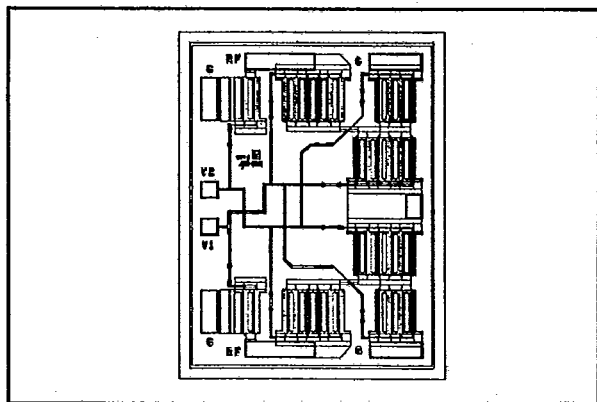


MA4GM303 SERIES

GaAs MMIC DC - 2 GHz Voltage Variable Absorptive Attenuator



Description

The MA4GM303 series of DC - 2 GHz GaAs FET MMIC absorptive bridge "T" attenuators will provide up to 32 dB of "matched" attenuation. The input and output SWR is less than 1.5 maximum under all attenuation values. The 0.1 dB compression point is 0 dBm. These attenuators are available as a bondable chip, in a TO-5 package and in three flat pack packages. The control voltage requirements are 0 to -5 volts and maximum control current (leakage) is 50 μ A.

This attenuator has two independent bias controls. By varying these two bias voltages, 32 dB of matched attenuation can be obtained.

The attenuator may be also used with "single bias control" by leaving V_1 at zero bias and controlling V_2 from 0 to -5 volts. Attenuation is reduced to 22 dBm maximum.*

These small attenuators have very flat attenuation from DC - 2 GHz. The electrical performance at both input and output is symmetrical.

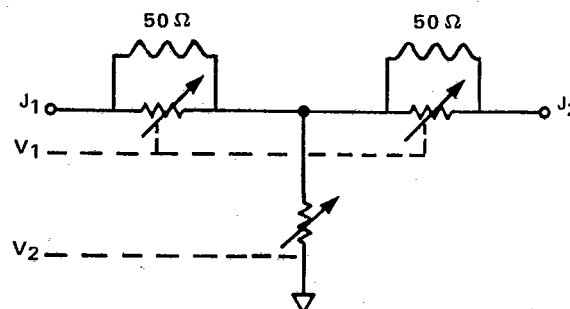
They are suggested as inexpensive, fast attenuators for AGC circuits in military systems, instrumentation, telecommunications and RF equipment or for control of signal levels in signal processing.

*In single bias mode of operation attenuator becomes reflective.

Features

- SINGLE* OR DUAL DC BIAS CONTROL
- EASILY CASCADABLE
- SMALL SIZE
- ATTENUATION FLATNESS
DC - 2 GHz $\pm$.2 dB
- LOW CONTROL CURRENT
CONSUMPTION (50 μ A)
- LOW PHASE SHIFT
- UP TO 32 dB MATCHED ATTENUATION

BRIDGE 'T' ATTENUATOR SCHEMATIC



ELECTRICAL SPECIFICATIONS @ 25°C¹

M/A-COM ADV SEMICONDUCTOR 27E D

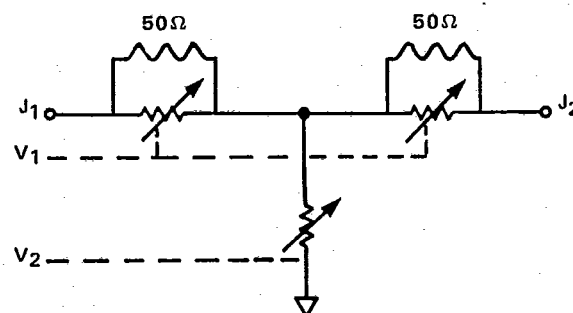
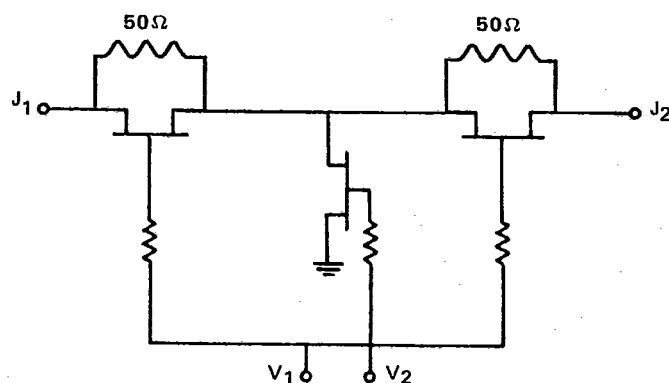
Parameters	Symbol	Test Conditions (T _A = 25°C)	Frequency	Min.	Nominal	Max.	Units
Insertion Loss ⁴	L	V ₁ = 0, V ₂ = -5	DC - 1.0 GHz 1.0 - 2.0 GHz	— —	1.3 1.4	1.5 1.7	dB
VSWR I/O ¹	SWR	All Attenuation Levels	DC - 1.0 GHz 1.0 - 2.0 GHz	— —	1.1 1.25	1.5 1.5	—
Relative Attenuation (Matched) ¹	—	Linear Attenuation	DC - 2.0 GHz	30	32	—	dB
Relative Attenuation (Single Bias) ²	—	Linear Attenuation	DC - 2.0 GHz	20	22	—	dB
Compression Point	P _{-1 dB}	(See Figure)	—	—	0	—	dB
Control Voltage ⁵	V _C	I _{GSL} < 50μA	—	—	0	-5	V
Phase Shift	Φ	10 dB Dynamic Range	1 GHz	—	3	—	Degrees
Leakage Current	I _{GSL}	@ -5V	—	—	—	50	μA

Notes:

- Two dc bias voltages required.
- One dc bias voltage required.
- All data in data sheet refer to dual dc bias control except for page 3 and line item referenced in note 2.
- Insertion loss is .2 dB lower for chip
- The control range for operation is 0 to -5 volts.

ABSOLUTE MAXIMUM RATINGS @ 25°C

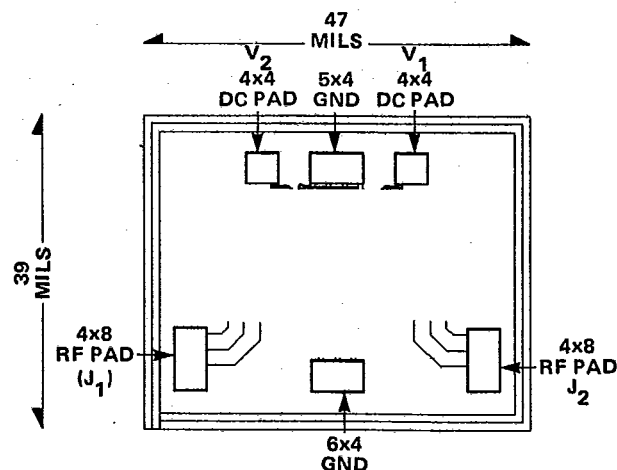
Symbol	Parameters	Units	Recommended Maximum
V _C	Control Voltage (V ₁ , V ₂)	V	-9
P _{IN}	Input Power: Operating Survival	dBm	see figures 27
T _{st}	Storage Temperature	°C	-55 to +150
T _{op}	Operating Temperature	°C	-55 to +125

ATTENUATOR EQUIVALENT CIRCUIT**ATTENUATOR SCHEMATIC DIAGRAM**

Note: All dc points have an impedance of at least 5K Ω

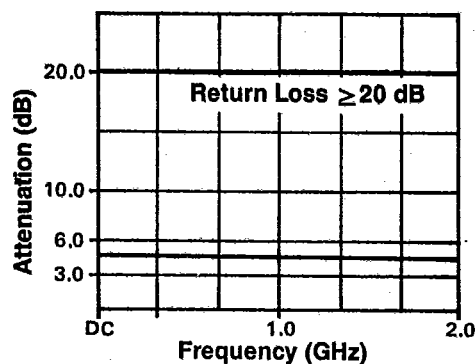
Attenuation Variation with Temperature for Dual Bias Mode with Return Loss > 20 dB.

Worst case variation of attenuation over the temperature range of -55°C to +125°C is ±0.5 dB or ±10% of the nominal value, whichever is greater. However, it is possible to minimize this tolerance by trading off return loss.

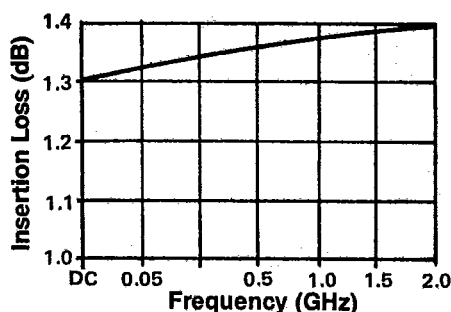
**BONDING DIAGRAM
MA4GM303-500**

M M/A-COM[®]

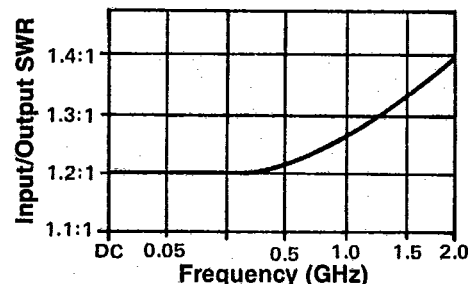
TYPICAL PERFORMANCE CURVES FOR DUAL BIAS CONDITION



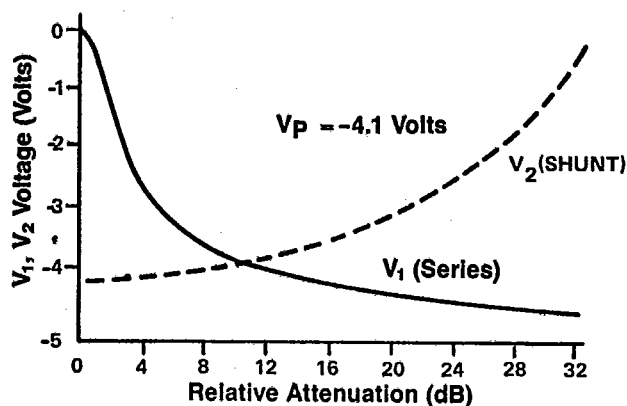
Attenuation vs. Frequency for Various Levels of Attenuation



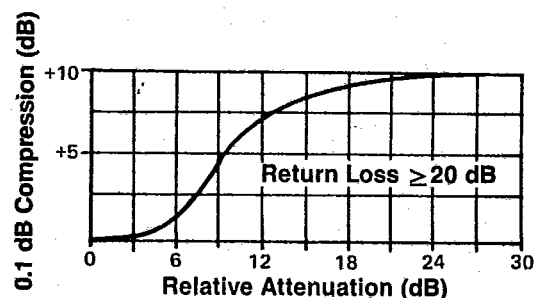
Insertion Loss vs. Frequency



(Insertion Loss Condition)
SWR vs. Frequency

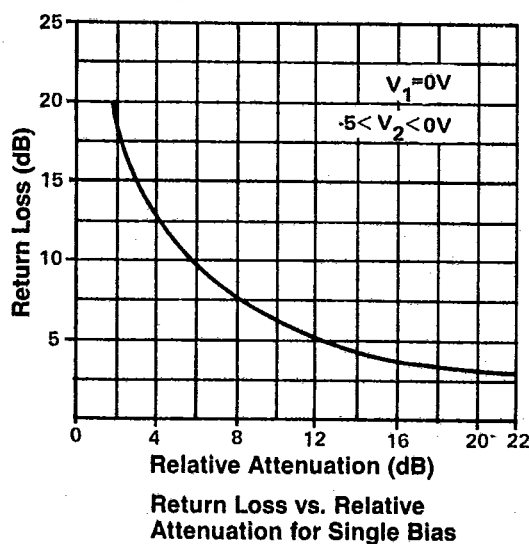


Attenuation under matched conditions vs. voltage bias for dual bias operation. All device types are specified with a .3 volt pinch off range.

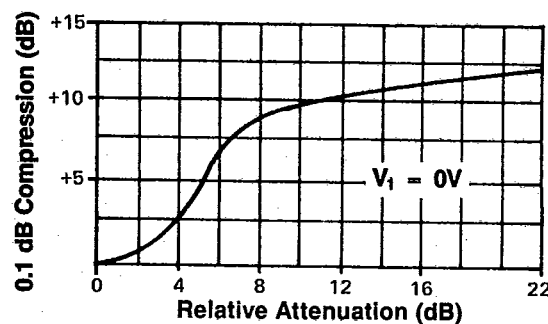
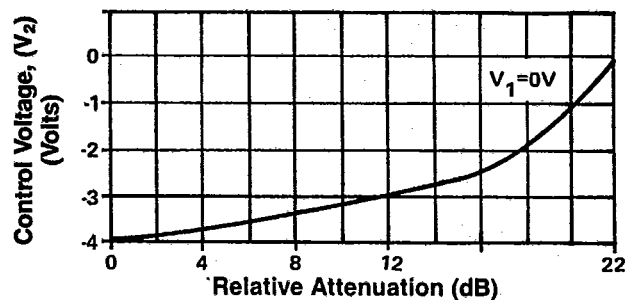


0.1 dB Compression vs. Relative Attenuation for Dual Bias

TYPICAL PERFORMANCE CURVES FOR SINGLE BIAS CONDITION ($V_1 = 0$ VOLTS)



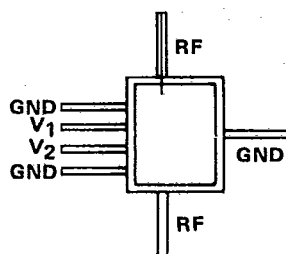
Return Loss vs. Relative Attenuation for Single Bias



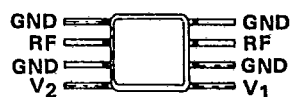
0.1 dB Compression vs. Relative Attenuation for Single Bias

PIN OUT DIAGRAMS — TOP VIEW (ALL PACKAGES)

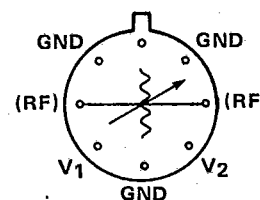
2000 AND 2100 PIN OUT



2012 PIN OUT



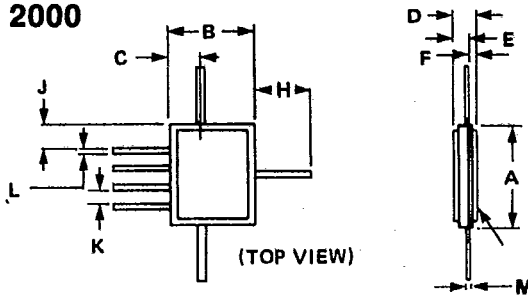
2010 PIN OUT



Note: Bottom surface of all packages and leads marked 'GND' are electrical ground for the circuit. Isolation specifications were measured with optimum condition (bottom surface grounded). This is important above 500 MHz.

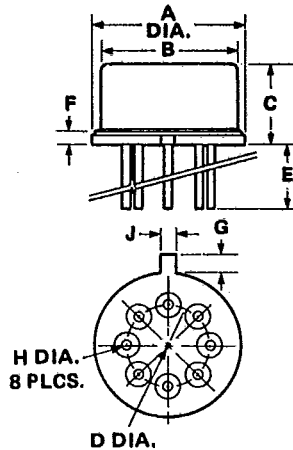
CASE STYLES M/A-COM ADV SEMICONDUCTOR 27E D 5642183 0000344 2

2000



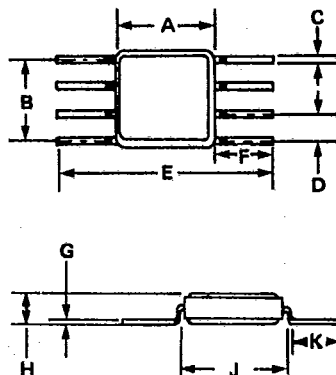
DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.252	.268	6.40	6.80
B	.207	.223	5.25	5.66
C	.075	.085	1.90	2.15
D	.050	.065	1.27	1.65
E	.027	.035	.685	.889
F	.020	.030	.508	.762
H	.120	.160	3.05	4.06
J	.053	.063	1.34	1.60
K	.032	.038	.812	.965
L	.008	.012	.203	.304
M	.004	.007	.101	.177

2010



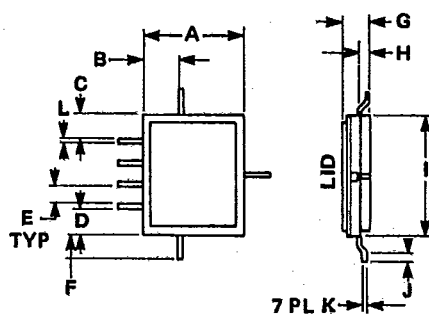
DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.335	.370	8.50	9.39
B	.305	.335	7.74	8.50
C	.180	.200	4.57	5.08
D	T.P.	.200	T.P.	5.08
E	.250	—	6.35	—
F	—	.040	—	1.02
G	.029	.045	0.737	1.14
H	.016	.019	0.41	0.48
J	.028	.034	0.68	0.86

2012



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.175	.185	4.44	4.69
B	.145	.155	3.68	3.93
C	.014	.016	0.35	0.40
D	.045	.055	1.14	1.40
E	—	.400	—	10.16
F	.090	.110	2.29	2.79
G	.004	.006	0.10	0.15
H	—	.075	—	1.90
J	.205	.215	5.20	5.46
K	.060	.080	1.52	2.03

2100



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.233	.207	5.64	5.25
B	.085	.075	2.15	1.90
C	.063	.053	1.60	1.34
D	.063	.053	1.60	1.34
E	.038	.032	0.94	0.81
F	.070	.050	1.77	1.27
G	.065	.050	1.65	1.27
H	.034	.024	0.91	0.61
I	.268	.252	6.80	6.40
J	.025	.015	0.43	0.34
K	.007	.004	0.17	0.10
L	.012	.006	0.30	0.20