National Semiconductor

NM95C12 Quad DataSwitch EEPROM (1K) (MICROWIRE™ Bus Inferface)

General Description

The NM95C12 is a 976-bit CMOS EEPROM configured as 16 bits x 61 addresses (registers) of EEPROM memory, integrated with four DataSwitch units. Each DataSwitch consists of two outputs that can be configured to a logic "0", logic '1', or as an analog DIP switch between the two. Therefore, this device can be programmed to form 4 pairs of SPST switches or 8 configurable outputs in addition to all standard EEPROM memory functions.

All DataSwitch functions are controlled by a 16-bit Switch Control Register (SCR) with the current switch setting stored in a Switch Readback Register (SRR) for switch status confirmation. In addition, DataSwitch power-up conditions are set by a standard EEPROM Switch Power-up Configuration Register (SPCR) dedicated for this purpose.

The NM95C12 memory is organized as follows:

Register	Function	Type
Registers 0–60	EEPROM array	Nonvolatile
Register 61	DataSwitch Power-up Configuration Register (SPCR)	Nonvolatile
Register 62	Switch Control Register (SCR)	Volatile
Register 63	Switch Readback Register (SRR)	Volatile

This device is fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. In addition, this device is available in an SO package for small space considerattions.

The EEPROM interfacing is MICROWIRE compatible for simple interface to standard microcontroller and microprocesors. There are 7 instructions that control the EEPROM memory: Read (READ), Write (WRITE), Write Enable (WEN), Write Disable (WDS) and Write all (WRALL). All programming is self-timed with the READY/BUSY status available on the DO pin during programming.

Features

- Four on-chip DataSwitch units
- Each DataSwitch can be configured as 2 programmable outputs or as an Analog switch
- DataSwitch power-up settings controlled by EEPROM register (SPCR)
- No erase required before write
- Sequential register read
- Reliable CMOS floating gate technology
- 4.5V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 year data retention
- Endurance: 10^6 data changes
- Packages availability: 14-pin DIP, 14-pin SO

Block Diagram

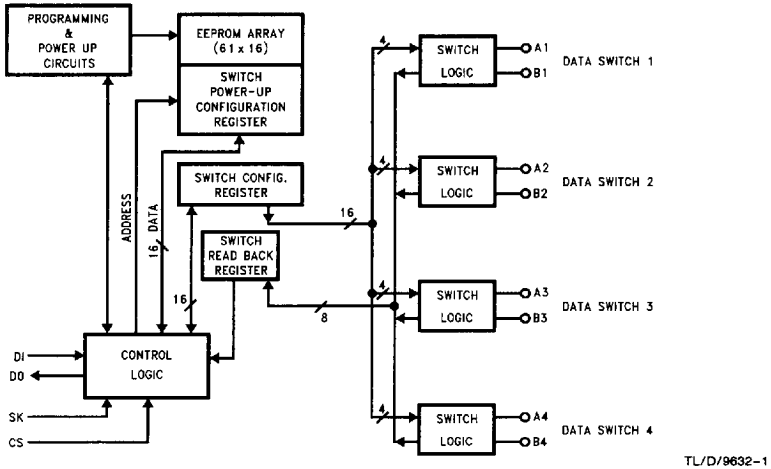
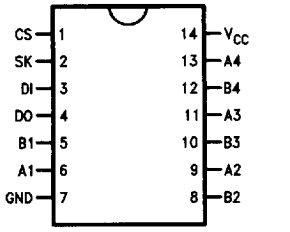


FIGURE 1. Block Diagram

Connection Diagrams

SO Package



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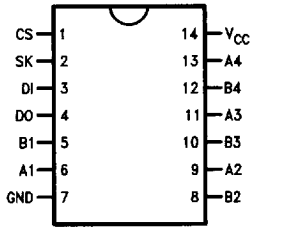
Top View
Order Number NM95C12M, NM95C12EM and NM95C12MM
See NS Package M14A

Dual-In-Line Package



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Top View
Order Number NM95C12N, NM95C12EN and NM95C12MN
See NS Package N14A

Pin Names

CS	Chip Select
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
A1–A4 B1–B4	Switch Terminals

Pin Descriptions

Pin Name	Description
CS	Chip Select, Input—This input must be high while communicating with the NM95C12. When this input is LOW, the chip is powered down into the standby mode. It should be noted that the CS does not control the A1 through A4 and B1 through B4 outputs and hence has no effect on them. The CS input must be made LOW after completing an instruction to prepare the control logic to accept the next instruction. If the CS input becomes LOW prematurely, the operation in progress is aborted. If programming the E^2 memory is in progress and the CS goes LOW, the programming is not aborted but will proceed to its normal completion.
SK	Serial Clock, Input—This input is used for clocking the serial I/O. The CS input must be high for clocking to have any effect. Information presented on the DI input will be shifted into the device on the LOW to HIGH transition of the clock. Information from the device will be available on the DO output serially, in response to the LOW to HIGH transition of the clock.
DI	Serial Data In, Input—All information needed for the operation of the device is entered serially from this input. HIGH represents logic '1' and LOW represents logic '0'. The entry order is most significant bit first and least significant bit last.
DO	Serial Data Out, Output, TRI-STATE®—When data is read, data from the addressed location will be available on this output serially, in sync with the LOW to HIGH transitions on the SK input. Normally the DO pin is in high impedance state. During a read instruction, when the last bit of the address is shifted in, the DO will go LOW indicating that data will follow. The data will follow in response to the clock transitions. The data will come out most significant bit first and least significant bit last. During E^2 programming operations, this output is also used as the status indicator. During programming operations, LOW indicates Busy (programming in progress) and HIGH indicates Ready. The DO output will be in the high impedance state if the CS input is LOW unconditionally.
A1–A4 B1–B4	Switch Terminals—These pins provide the simulated DIP switch features and hence are called terminals. The behavior of these pins is determined by the settings in the Switch Configuration Register and are independent of the CS input.
V_{CC}	Power Supply.
GND	Ground.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	6.5V
Voltage at Any Pin	−0.3 to +6.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation @25°C	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM95C12	0°C to +70°C
NM95C12E	−40°C to +85°C
NM95C12M*	−55°C to +125°C
Power Supply Voltage (V_{CC})	4.5V to 5.5V

*Contact factory for availability

DC Electrical Characteristics V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	$C_S = V_{IH}$, SK = 1 MHz		4	mA
I_{CC2}	Operating Current TTL Input Levels	$C_S = V_{IH}$, SK = 1 MHz		6	mA
I_{CC3}	Standby Current CMOS Input Levels on Switches	C_S = 0V		50	μA
I_{CC4}	Standby Current TTL Input Levels on Switches	C_S = 0V		800	μA
I_{iL} I_{oL}	Input Leakage (Note 4) Output Leakage	V_{IN} = 0V to V_{CC} (Note 4)		±1	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		−0.1 2.0	0.8 V_{CC} + 1	V V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage	I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V V
R_{ON}	Switch On Resistance			200	Ω
R_{OFF}	Switch Off Resistance		10		MΩ
V_S	Maximum Voltage Allowed on any Switch Terminal			V_{CC} + 1	V
I_S	Max Current Allowed through Switch Terminals			10	mA

AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
f_{SK}	SK Clock Frequency	NM95C12 NM95C12E NM95C12M	(Note 5)	0 0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM95C12 NM95C12E NM95C12M		250 300 500		ns
t_{SKL}	SK Low Time	NM95C12 NM95C12E NM95C12M		250 250 500		ns
t_{SKS}	SK Setup	NM95C12 NM95C12E NM95C12M		50 50 100		ns ns ns
t_{CS}	Minimum CS Low Time	NM95C12 NM95C12E NM95C12M	(Note 2)	250 250 500		ns
t_{CSS}	CS Setup Time	NM95C12 NM95C12E NM95C12M		50 50 100		ns

AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PUSR}	Power Up Slew Rate			1		ms
t_{DIS}	DI Setup Time	NM95C12 NM95C12E NM95C12M		100 100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"	NM95C12 NM95C12E NM95C12M			500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM95C12 NM95C12E NM95C12M			500 500 1000	ns
t_{SV}	CS to Status Valid	NM95C12 NM95C12E NM95C12M			500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE	NM95C12 NM95C12E NM95C12M	CS = V_{IL}		100 100 200	ns
t_{ISWD}	Switch Delay from Switch Input	NM95C12 NM95C12E NM95C12M			250 250 500	ns
t_{SWPD0}	Switch Delay to 0 from Config. Change	NM95C12 NM95C12E NM95C12M			500 500 1000	ns
t_{SWPD1}	Switch Delay to 1 from Config. Change	NM95C12 NM95C12E NM95C12M			500 500 1000	ns
t_{SWS}	A1–A4, B1–B4 Setup Time for SRR Read	NM95C12 NM95C12E NM95C12M		100 100 200		ns
t_{SWH}	A1–A4, B1–B4 Hold Time for SRR Read	NM95C12 NM95C12E NM95C12M		100 100 200		ns
t_{WP}	Write Cycle Time				10	ms
t_{DH}	DO Hold Time			10		ns

Capacitance (Note 3)

T_A = 25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages.)

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKH\ (minimum)} = t_{SKL\ (minimum)}$ for shorter SK cycle time operation.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Level	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/0.4 mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Functional Description

Per the **General Description,** the NM95C12 EEPROM array and switch control registers are organized into two main function blocks:

- EEPROM memory array: Addresses 0–60
- Switch Control Registers:
  - Switch Power-up Configuration Register (SPCR)
  - Switch Control Register (SCR)
  - Switch Readback Register (SRR)

ADDRESS SPACE

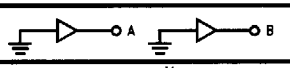
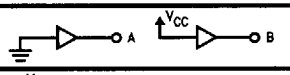
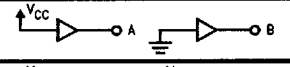
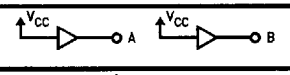
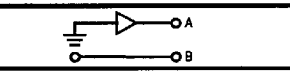
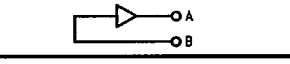
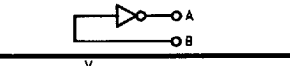
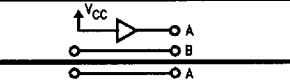
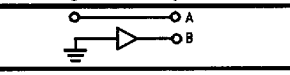
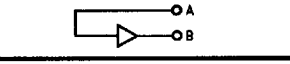
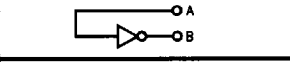
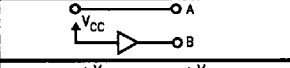
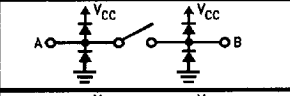
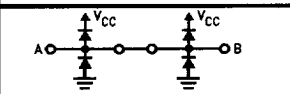
Registers 0–60 of the E²PROM are available to the user as general purpose non-volatile memory. Data may be read or programmed into this memory using the appropriate instructions. Address location 61 is an E² location which also can be read or programmed like any other E² location. However, address 61 is used in the NM95C12 to provide the initial switch configuration information automatically on power-up (SPCR).

The switch Control Register (SCR) is located at address 62. The SCR is not an E² location and hence is volatile. It does not have endurance limits or programming time requirements associated with it, allowing the switches to be reconfigured an unlimited number of times.

The SCR is automatically loaded from address 61 on power-up. The SCR controls the switch logic and hence the behavior of the terminals A1 through A4 and B1 through B4.

Located at address 63 is the Switch Readback Register (SRR). This is a read only register.

TABLE I. Switch Configurations

MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0 , B = 0
1	0	0	0	1		A = 0 , B = 1
2	0	0	1	0		A = 1 , B = 0
3	0	0	1	1		A = 1 , B = 1
4	0	1	0	0		A = 0 , B = TRI-STATE
5	0	1	0	1		A = B
6	0	1	1	0		A = $\overline{B}$
7	0	1	1	1		A = 1 , B = TRI-STATE
8	1	0	0	0		A = TRI-STATE , B = 0
9	1	0	0	1		B = A
10	1	0	1	0		B = $\overline{A}$
11	1	0	1	1		A = TRI-STATE , B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

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*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.

Functional Description (Continued)

SWITCH CONFIGURATIONS

The 16-bit SCR format is shown in *Figure 2*. It consists of four 4-bit fields. Each field controls its corresponding switch control logic. The individual bits in each field are labelled W, X, Y, and Z. Table I shows the relationship between these bit values and the resulting behavior of the terminals. It should be remembered that the CS input has no effect on the behavior of the terminals.

SWITCH READBACK REGISTER

The SRR allows the current logic level present at the switch terminals to be read back via the Microwire bus. The SRR is loaded by the rising edge of SK immediately after the last instruction bit is clocked in (The same clock edge that loads A0). The SRR is loaded on this clock edge only when register 63 (Switch Readback Register) is being read. In the case of switch mode 13 (Analog switch mode), the SRR will not report the actual levels present at the terminals due to this mode being analog levels. In mode 13, bits 15–8 of the SRR will be all 0's to indicate a closed analog switch. This is done to avoid ambiguous logic levels which could exist when the device is used in the analog switch mode.

The bit assignments and conceptual function of the SRR is shown in *Figure 3*. As shown, only bits 15 thru 8 are used, and bits 7 thru 0 are always read as logical 0. The SRR is a Read-Only register and if it is written, the device will not perform a write or generate a Ready/Busy status.

INSTRUCTION SET

The NM95C12 instruction set contains five instructions, and each instruction is ten bits long. The first 2 bits of the instruction are the start bits (SB) and are always a logical "01", followed by the op code (2 bits) and the address field (6 bits). The WRITE and WRALL instructions are followed by sixteen bits of data (D15–D0) which is written into the memory. Table II is a list of the instructions and their format.

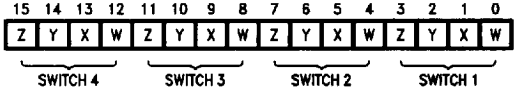

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FIGURE 2. Switch Configuration Register (SCR)

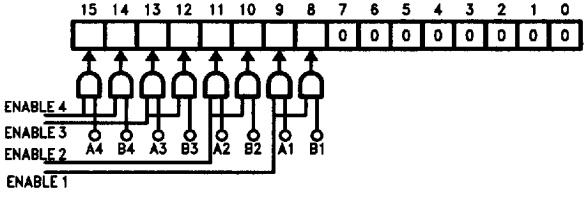

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FIGURE 3. Switch Readback Register (SRR)

TABLE II. NM95C12 Instructions

Instruction	SB	Op Code	Address	Data	Comments
READ	01	10	A5–A0		Reads data at selected address.
WEN	01	00	11XXXX		Enables all programming modes.
WRITE	01	01	A5–A0	D15–D0	Writes selected register.
WRALL	01	00	01XXXX	D15-D0	Writes all registers.
WDS	01	00	00XXXX		Disables all programming modes.

Functional Description (Continued)

WDS (Write Disable): When this instruction is issued, all programming modes are disabled. Any attempt to write into a disabled device is ignored. The NM95C12 powers up in the disabled state. The WEN is the only instruction that enables the device. The write disable operation has no effect on read operations.

WRALL (Write All): When this instruction is executed, the NM95C12 bulk-programs the same 16-bit data pattern into all of its E^2 memory locations (address 0 through 61). The SCR is unaffected since it is not an E^2 location. However, since the SPCR is included in the EEPROM array it will be programmed. The data pattern must follow immediately after the last bit of this instruction. The chip enters into the self-timed program mode after CS is brought low, before the next rising edge of SK.

WEN (Write Enable): This instruction is used to enable all programming modes. The circuits will remain enabled until the WDS instruction disables them. The NM95C12 powers up in the disabled state and hence WEN must be executed prior to any programming instructions.

WRITE (Write/Program): This instruction writes a 16-bit data word into the address location specified by the A_0–A_5 bits of the instruction. The 16 data bits must follow the last bit of the instruction. After loading the WRITE instruction and the 16-bit data, the chip enters into the self-timed program mode when CS is brought low before the next rising edge of the SK clock. If the addressed location is the SCR, then the chip does not enter into the self-timed E^2 programming mode (the SCR is not an E^2 location) but loads the switch configuration data into the SCR. The WRITE instruction can only be aborted by deselecting the chip (CS LOW) before entering all the instruction bits.

READ (Read): This instruction reads the data from the addressed location. As before, the instruction also contains the address. The data will come out serially on the D0 output on the rising edge of the clock. A logical '0' precedes the 16-bit data (dummy bit).

The NM95C12 has a convenient feature called sequential register read. Normally, the CS input is made LOW after the last data bit is shifted out. However, if the CS input is left HIGH and clocking continues, data from the next address location will be delivered on the D0 pin. This sequential read can continue indefinitely whereby the address is automatically incremented after delivering 16 bits of data. It should be noted that in the sequential register read mode, address wrap-around will occur from Amax–Amin.

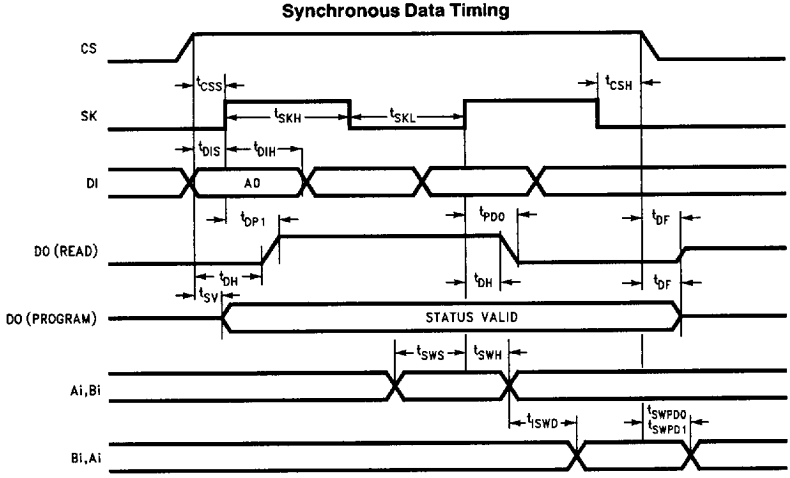
During a sequential register read there will be a dummy bit preceding the first word read, after which, the bit stream will be continuous without any dummy bits separating the data words.

Ready/Busy Indication

Programming an E^2 memory takes several milliseconds. Unlike some devices which require the user to keep track of the elapsed time to ensure completion of the programming cycle, the NM95C12 contains an on-chip timer. The timer starts when the CS input goes LOW after the last data bit is entered. After entering a programming cycle (CS forced LOW), the timer status may be observed by forcing the CS input back HIGH. The timer status is available on the D0 pin if the CS input is forced HIGH within one ms of starting the programming cycle. LOW on the D0 pin indicates that the programming is still in progress while HIGH indicates the device is READY for the next instruction. It should be noted that if the CS input is made HIGH for status observation, it must be made LOW when READY is indicated before loading the next instruction.

Timing Diagrams

Synchronous Data Timing



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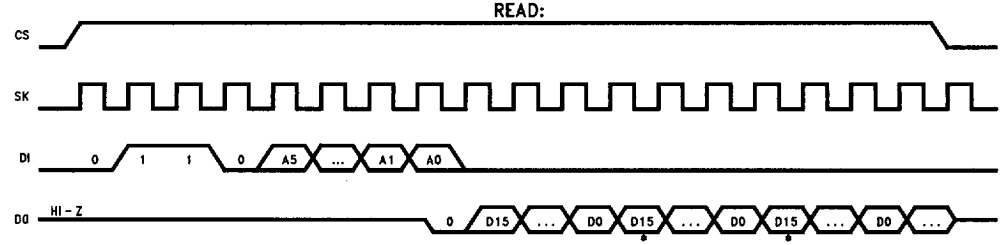
† t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

Timing Diagrams (Continued)

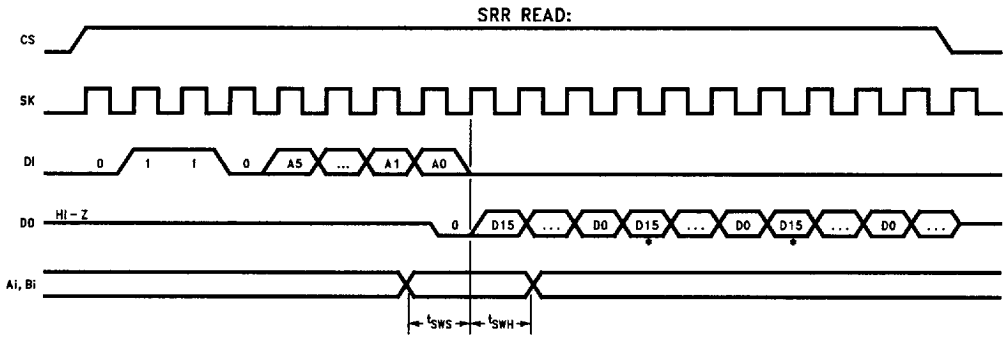
Instruction Sequence

READ:



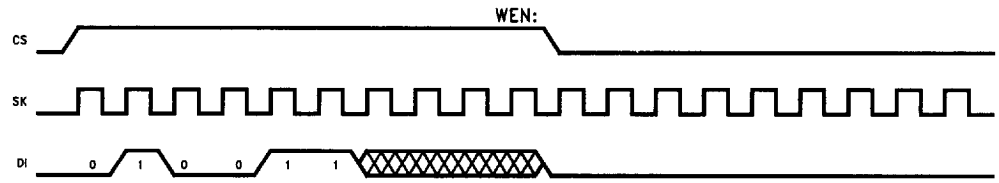
TL/D/9632-8

SRR READ:



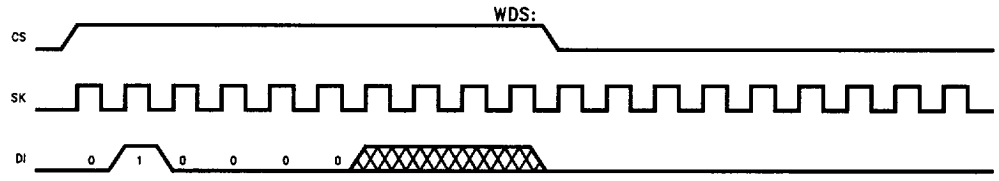
TL/D/9632-14

WEN:



TL/D/9632-9

WDS:

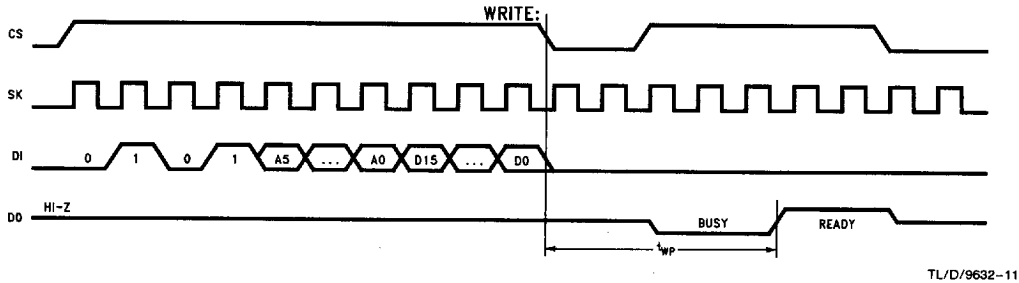


TL/D/9632-10

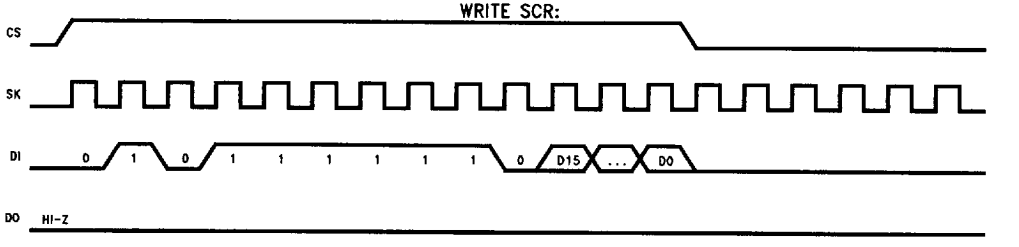
*The memory automatically cycles to the next register.

Timing Diagrams (Continued)

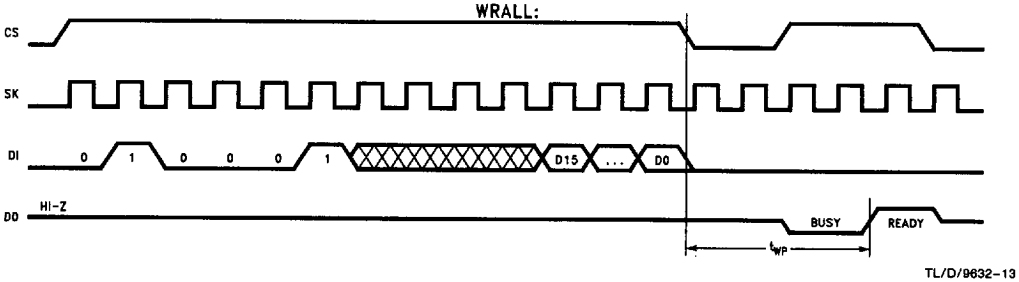
Instruction Sequence (Continued)



TL/D/9632–11



TL/D/9632–12



TL/D/9632–13