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SSI 32R1540R
+5V, -4.5V, 6-Channel MR Read/Write/Servo Read

Advance Information

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DESCRIPTION

The SSI 32R1540R is a BiCMOS monolithic integrated circuit designed for use with four-terminal Magneto-Resistive recording heads. It provides a write driver, MR read bias current, low noise read amplifiers for the MR head, and fault detection circuitry for up to six channels. The device requires +5V and -4.5V power supplies and comes in a 64-Lead TQFP package.

FEATURES

- **+5V, -4.5V ± 10% supply**
- **Designed for four-terminal MR heads with minimum external components**
- **Truly differential I-bias/V-sense MR read Amp**
- **MR head bias current range = 10 - 26 mA**
- **MR read gain = 250 V/V**
- **MR read input noise = 0.65 nV/√Hz (Nom)**
- **MR read input resistance = 900Ω (Nom)**
- **Differential PECL write data input with Flip-Flop**
- **Head voltage swing = 7.0 Vpp (Nom)**
- **Write current range = 5 - 30 mA**
- **Write unsafe detection**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**

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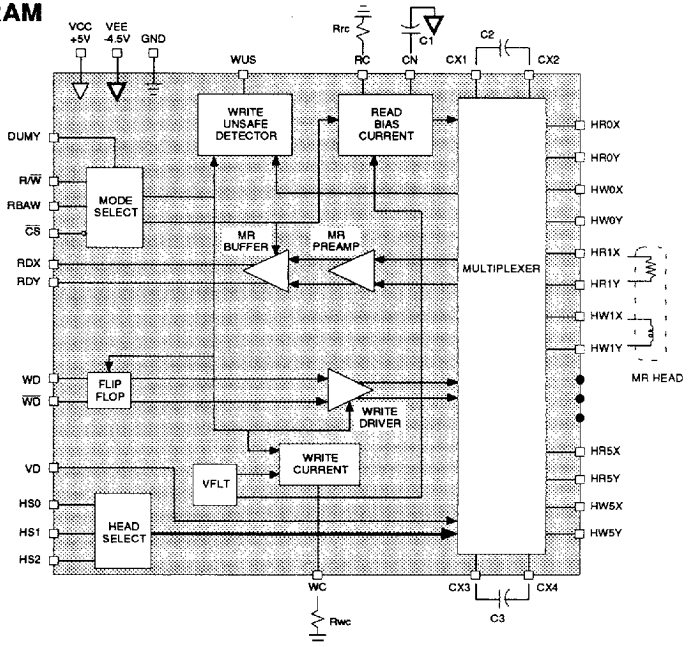
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

The SSI 32R1540R addresses up to 6 four-terminal MR heads providing write drive or read bias and amplification. The mode control and head selection are accomplished with TTL pins $\overline{CS}$, R/W, RBAW, DUMY, and HSn as shown in Tables 1 and 2. All the TTL inputs have internal pull-up resistor so that when left opened, it will default to the TTL High state.

TABLE 1: Mode Select

$\overline{CS}$	R/W	RBAW	DUMY	MODE
0	1	X	0	Read
0	0	0	0	Write, MR bias current off
0	0	1	0	Write, MR bias current on for fast Write to Read recovery
1	X	X	X	Idle, dummy head selected
X	X	X	1	Idle, dummy head selected

TABLE 2: Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	None
1	1	1	None

WRITE MODE

Taking both $\overline{CS}$ and R/W low selects Write mode which configures the 32R1540R as a current switch and activates the Write Unsafe (WUS) detect circuitry. Head current is toggled between the X (HWnX) and Y (HWnY) side of the selected head on each Low to High transition of the differential PECL signal WD - $\overline{WD}$. Changing from Read or Idle mode to Write mode initializes the Write Data Flip-Flop to pass write current into the "Y" pin, i.e., the X side of the head will be higher potential than the Y side.

The write current is externally programmed either by a resistor Rwc connected from pin WC to GND or by a current sink between pin WC and GND. The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{Aw \cdot Vwc}{Rwc} = \frac{Kw}{Rwc}$$

where Aw is 20 mA/mA and Vwc is 2.0 Volts.
Note that the actural head current $I_{x,y}$ is given by:

$$I_{x,y} = \frac{Iw}{1 + Rh/Rd}$$

where Rh is the head DC resistance and Rd is the damping resistance. In Write mode a 450Ω damping resistor is switched in across the selected HWnX, HWnY ports.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe (WUS) open collector output.

- WD/$\overline{WD}$ frequency too low
- Device in Read mode
- Device in Idle mode
- No head current
- Head opened
- Invalid head address decoded

Upon entering Write mode, WUS is valid after two Low to high transitions of WD - $\overline{WD}$ following the required Read - Write transition time (0.5 µs max).

READ MODE

Taking $\overline{CS}$ low and R/W high selects Read mode which activates the MR bias current generator, and low noise differential amplifier. The outputs of the MR amplifier RDX and RDY are emitter followers and are in phase with the resistivity change at the selected input ports HRnX and HRnY where the respective MR head is attached.

The DC current necessary for biasing the MR sensor is externally programmed either by a resistor Rrc connected from pin RC to GND or by a current sink between pin RC and GND. The magnitude of the bias current is given by:

$$Ir = \frac{Ar \cdot Vrc}{Rrc} = \frac{Kr}{Rrc}$$

where Ar is 20 mA/mA and Vrc is 2.0 Volts.

An external capacitor C1 connected from pin CN to VEE is used for reducing the shot noise from MR bias current source. A low inductance capacitor with a value of 0.1 µF is recommended. Two external floating capacitors C2 and C3, C2 connected between pins CX1, CX2 and C3 connected between CX3, CX4, for DC blocking of the MR sensors are required for all six channels. For the application that uses up to four MR heads, i.e., head 0 to head 3, only one floating capacitor connected between pins CX1 and CX2 is required. Care should be taken to use only the low-inductance high-frequency capacitors and to place all the external capacitors as close to the IC as possible as the stray inductance will degrade the MR amplifier's noise and frequency response performance. The value of the DC blocking capacitor C2/C3 will have direct effect on the Write to Read recovery time. For fast recovery time, the capacitor value should be kept as small as possible. The value of the capacitor C2/C3 also sets the low-frequency cutoff of the MR amplifier. The -3 dB low-frequency corner is given by:

$$f_L = 1/(2\pi \cdot 15\Omega \cdot C2)$$

For example, a 0.1 µF capacitor for C2/C3 will result in the -3 dB low-frequency of about 106 kHz.

To further improve the Write to Read recovery time, the MR bias current in the selected head can be left on during Write mode by taking RBAW pin high. With the MR bias current turned on, the voltage change across the DC blocking capacitor C2/C3 between Write and Read mode will be minimized which would then result in faster Write to Read recovery time. For best trade-off between power dissipation and Write to Read recovery time, the MR bias current doesn't have to be on for the whole Write period. A turn-on period in the range of tens of micro-seconds prior to the Write to Read transition usually would be sufficient.

In Read mode, the voltage at the midpoint of the selected MR head is forced to the same voltage as pin VD. VD is usually shorted to GND so that the voltage difference between the MR head and disks is minimized. For the unselected MR heads, the head ports become high impedance and thus will prevent the heads from conducting current in the event of head to disk contact.

FUNCTIONAL DESCRIPTION (continued)

IDLE MODE

Taking $\overline{CS}$ or DUMY high selects Idle mode which deactivates both the write current source and MR bias current. The voltage at pin RC remains active so that an internal dummy head can be switched on to provide proper voltage biasing for the DC blocking capacitor C2/C3. The pins RDX/RDY and WC are switched into high impedance state to facilitate multiple device applications where these pins could be wire OR'ed.

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disability the write current generator and MR bias current during a voltage fault or power startup regardless of mode.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HW0X - HW5X	I/O	Inductive write head X connection
HW0Y - HW5Y	I/O	Inductive write head Y connection
HR0Y - HR5X	I/O	MR read head X connection
HR0Y - HR5Y	I/O	MR read head Y connection
CN	I	Noise filter Cap C1; X side; Y side of C1 should be connected to VEE
CX1,CX2	I	Floating DC blocking Cap C2; for head 0 to head 3
CX3, CX4	I	Floating DC blocking Cap C3; for head 4 and head 5
WD, $\overline{WD}$	I	Differential PECL Write Data input, a positive transition of (WD-$\overline{WD}$) toggles the direction of the head current
RDX, RDY	O	Differential MR head Read Data output
WC	I	Write Current set: used to set the magnitude of the write current
RC	I	Read Current set: used to set the magnitude of the MR bias current
WUS	O	Write Unsafe; open collector; a high level indicates an unsafe writing condition
HS0,HS1,HS2	I	Head Select: select one of six heads; TTL
CS/	I	Chip Select: a high inhibits the chip; TTL
R/W	I	Read/Write: a high level selects Read mode; TTL
DUMY	I	A high level inhibits the chip; TTL
RBAW	I	A high level activates the MR bias current in Write mode; TTL
VD	I	Analog Reference for MR head voltage
VCC	I	+5V Supply
VEE	I	-4.5V Supply
GND	I	Ground

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may result in permanent damage to the device.

PARAMETER		RATING
DC Supply Voltage	VCC	+6 VDC
	VEE	-6 VDC
Logic Input voltage	TTL	-0.3 to VCC + 0.3 VDC
Logic Input Voltage	PECL	0 to VCC VDC
Write Current	Iw	50 mA
MR Bias Current	Ir	40 mA
Output Current	WUS	+8 mA
	RDX/RDY	-5 mA
Operating Junction Temperature	T_j	+135°C
Storage Temperature	T_{stg}	-65 to +150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING
DC Supply Voltage	VCC	+5V, ±10%
	VEE	-4.5V, ±10%
Operating Ambient Temperature	T_A	0 to 70°C

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCC Supply Current	Read Mode		28 + 1.1 Ir		mA
	Write Mode, RBAW = Low		24 + 1.15 Iw + 0.15 Ir		mA
	Write Mode, RBAW = High		24 + 1.15 Iw + 1.1Ir		mA
	Idle Mode		6 + 0.15 Ir		mA
VEE Supply Current	Read Mode		18 + 1.05 Ir		mA
	Write Mode, RBAW = Low		21 + 1.1 Iw + 0.1 Ir		mA
	Write Mode, RBAW = High		21 + 1.1 Iw + 1.05 Ir		mA
	Idle Mode		5 + 0.1 Ir		mA

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Power Dissipation	Ir = 18 mA, Iw = 30 mA				
	Read Mode		405		mW
	Write Mode, RBAW = Low		550		mW
	Write Mode, RBAW = High		715		mW
	Idle Mode		70		mW
VCC Fault Voltage	Iw < 0.2 mA, Ir < 0.2 mA	3.75	4.0	4.25	VDC
VEE Fault Voltage	Iw < 0.2 mA, Ir < 0.2 mA	-3.75	-3.5	-3.25	VDC

DIGITAL INPUTS AND OUTPUTS

Input Low Voltage	VIL	TTL			0.8	VDC
Input High Voltage	VIH	TTL	2.0			VDC
Input Low Current	LIL	Vil = 0.8V	-0.4	-0.2		mA
Input High Current	LIH	Vih = 2.0V			100	µA
Input Low Voltage	VIL2	WD, $\overline{WD}$	Vcc -1.9		Vcc - 1.5	VDC
Input High Voltage	VIH2	WD, $\overline{WD}$	Vcc - 1.2		Vcc - 0.7	VDC
Input Low Current	LIL2	Vil2 = Vcc - 1.7V		3	50	µA
Input High Current	LIH2	Vih2 = Vcc - 0.9V		3	50	µA
Output High Current	IOH	WUS			50	µA
Output Low Current	LOL	WUS			4	mA
Output Low Voltage	VOL	WUS, Iol = 4 mA			0.5	VDC

READ CHARACTERISTICS, MR HEAD AMPLIFIER

Recommended operating conditions apply unless otherwise specified.
VD = 0 V; Rmr = 13Ω; Rrc = 2.22 kΩ; Rwc = 2.0 kΩ
CL (RDX, RDY) < 20 pF; RL (RDX, RDY) > 1 kΩ

MR Head Resistance				13		Ω
MR Current Range			10	18	26	mA
MR Current Gain	AR	Read Mode		20		A/A
MR Current Setting Voltage	VRC	All Modes		2		V
"KR" Factor		Kr = Ar • Vrc	37	40	43	V
MR Head Potential		Selected Head	-250		250	mV
Unselected MR Current					0.1	mA
Differential Voltage Gain		Vin = 1 mVpp @ 5 MHz	190	250	280	V/V
Voltage BW	-1dB	Rmr = 13Ω, Lmr = 20 nH		40		MHz
	-3 dB	Vin = 1 mVpp	60			MHz

READ CHARACTERISTICS, MR HEAD AMPLIFIER (continued)
Recommended operating conditions apply unless otherwise specified.
VD = 0 V; Rmr = 13Ω; Rrc = 2.22 kΩ; Rwc = 2.0 kΩ
CL (RDX, RDY) < 20 pF; RL (RDX, RDY) > 1 kΩ

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input Noise Voltage	Exclude head noise		0.65		nV/√Hz
Differential Input Resistance	Vin = 1 mVpp @ 5 MHz C2 = C3 = 0.1 µF		900		Ω
Differential Input Capacitance	Vin = 1 mVpp @ 5 MHz C2 = C3 = 0.1 µF		12		pF
Input Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	4			mVpp
CMRR	Vin = 1 mVpp @ 5 MHz	55			dB
PSRR	100 mVpp @ 5 MHz on VCC or VEE	50			dB
Channel Separation	Unselected channels driven with 100 mVpp @ 5 MHz	45			dB
Output Offset Voltage		-250		250	mV
Single Ended Output Resistance			35	70	Ω
Output Current		1.5	2.2		mA
RDX, RDY Common Mode Output Voltage		Vcc - 2.9	Vcc - 2.6	Vcc - 2.3	V

WRITE CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified.
Iw = 20 mA, Lh = 550 nH, Rh = 40Ω

Write Current Range			5	20	30	mA
Write Current Gain	Aw	Write Mode		20		A/A
Write Current Setting Voltage	Vwc	Write Mode		2		V
"Kw" Factor		Kw = Aw • Vwc	37	40	43	V
Differential Head Voltage Swing		Open Head Iw = 20 mA	6	7		Vpp
Unselected Head Current		DC			0.1	mA
		AC			1	mApk
Head Differential Damping Resistance	Rd	Write Mode		450		Ω
		Read or Idle mode		3000		Ω
Head Differential Load Capacitance					15	pF

SWITCHING CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified.
VD = 0V; Rmr = 13Ω; Rrc = 2.22 kΩ; Rwc = 2.0 kΩ
CL (RDX, RDY) < 20 pF; RL (RDX, RDY) > 1 kΩ
Lh = 550 nH, Rh = 40Ω, f(WD/$\overline{WD}$) = 5 MHz

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
R/W	Read to Write	To 90% of write current			0.5	µs
	Write to MR Read	To 90% of 100 mV read signal envelope; RBAW = 1			1	µs
$\overline{CS}$	Idle to MR Read	To 90% of 100 mV 5 MHz read signal envelope			5	µs
	Read/Write to Idle				0.5	µs
HSO, 1, 2,	to any MR head	To 90% of 100 mV 5 MHz read signal envelope			5	µs
WUS	Safe to Unsafe TD1	Write mode, from loss of (WD-$\overline{WD}$) transition	0.6	0.95	2.4	µs
	Unsafe to Safe TD2	Fault cleared, from first positive (WD-$\overline{WD}$) transition			0.5	µs
Head Current						
	WD/$\overline{WD}$ to I_{x-y} TD3	From 50% point		6	20	ns
	Asymmetry	Lh = 0, Rh = 0; (WD-$\overline{WD}$) has 1 ns rise/fall time			0.5	ns
	Rise/Fall Time	With head		4.5	6	ns

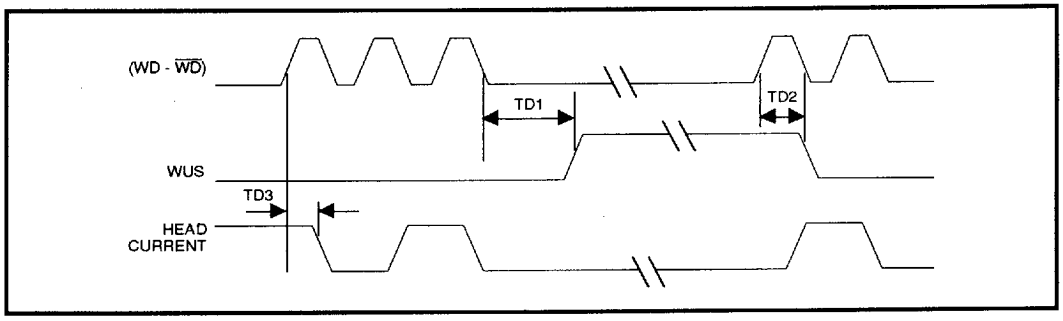
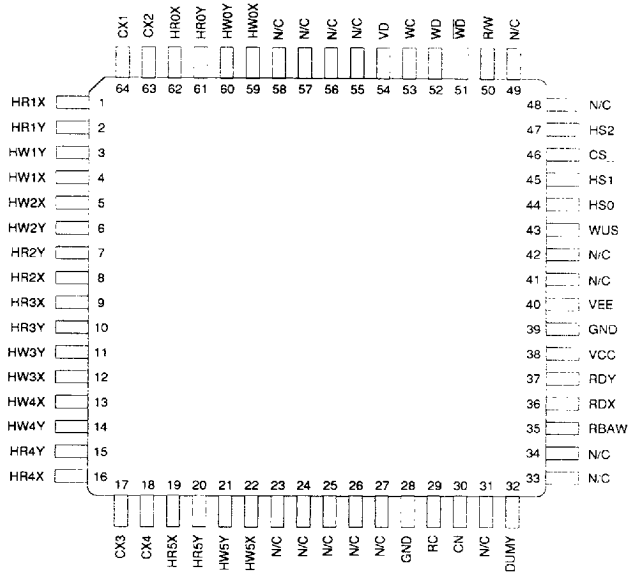


FIGURE 1: Write Mode Timing

PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: θjA

64-Lead TQFP	84°C/W



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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