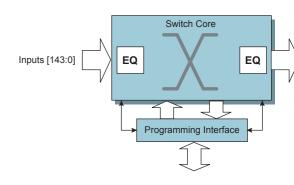


## **BLOCK DIAGRAM:**



FEATURES:	BENEFITS:
▶ 11 Gbps 144 × 144 strictly nonblocking switch matrix with multicast and output striping programming modes	1.584 Tbps aggregate bandwidth in a single chip for network switching and video systems
Input signal equalization (ISE) with programmable control globally or on a per-channel basis	<ul> <li>Addresses system-level and board-level signal integ intersymbol interface (ISI) jitter issues</li> </ul>
▶ Adjustable output pre-emphasis EQ	▶ EQ and drive flexibility for driving boards, backplane
▶ Differential current mode logic (CML) data output driver	▶ Convenient I/O flexibility for interfacing with multiple
▶ Protocol-independent switching and data transmission	▶ Can be used with latest storage, Ethernet, and netw
▶ 45 mm × 45 mm, 1.27 mm pin pitch, 1072-pin BGA package	▶ Layout-friendly package and pinout for easier PCB of
▶ Parallel and serial programming modes for configuration and monitoring	▶ Programming and control convenience
➤ Software control to optimize power dissipation	▶ Control and lower overall power when ports are not

## APPLICATIONS:

- ▶ High-definition digital broadcast video systems
- ▶ Multi-service provisioning platforms (MSPPs)
- ▶ Mixed TDM/packet switching systems
- ▶ High-speed storage, Ethernet, and networking equipment
- ▶ DWDM switching systems
- ▶ High-speed automated test equipment



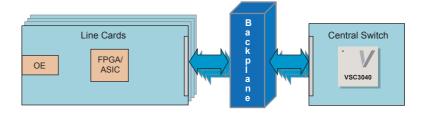
port bandwidth and 144 × 144 switch matrix enables a breakthrough 1.5 Tbps capacity in a single device.

The VSC3040 fully non-blocking switch core is programmed using a multimode port interface that allows random access programming of each I/O port. Each VSC3040 data output can be programmed to connect to any of its inputs. The signal path through the device is fully asynchronous, eliminating restrictions on the phase, frequency, or signal pattern of any input

terminated on-die, using 100  $\Omega$  resistors betwinputs with a common connection to an interaction and interact

Core programming for the VSC3040 device port-by-port basis, or multiple program assignn issued simultaneously. The entire device straight-through, multicast, or other configuration be powered down to allow efficient use of the require only a subset of the available I/O of enabled in the software by programming individe power-down code.

## **BACKPLANE APPLICATION:**



#### SPECIFICATIONS:

- ▶ 11 Gbps NRZ per-channel data rate
- ▶ 2.5 V power supply (2.5 V or 3.3 V program port power supply)
- ▶ 2.5 V or 3.3 V CMOS TTL-compatible I/O
- ▶ Differential CML I/O with integrated termination impedance

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