

# VSC3139

**VITESSE**

## 4.2 Gbps 72 x 72 Asynchronous Crosspoint Switch

**FEATURES:**

- ▶ 4.2 Gbps, 72x72 Strictly Nonblocking Switch Matrix with Dual User Configuration Registers and Multicast and Address Striping Programming Modes
- ▶ 3rd Generation Input Signal Equalization (ISE) 'Eye Opener' Technology with Global and Per Channel Multilevel Programmable Control
- ▶ At-Speed Built-in Self-Test (BIST) Capability with Auxiliary DRIVE and SENSE I/O, on Board PRBS Generator/Detector, and Programmable Temperature Alarm/Sensor
- ▶ Global and Per Channel Programmable CML Output Level Control with Integrated Back Termination
- ▶ Parallel and Serial Programming Modes with Secondary Serial Access Port for Configuration and Monitoring
- ▶ Software Control to Optimize Power Dissipation

**BENEFITS:**

- ▶ 4.2 Gbps NRZ performance provides protocol transparency with exceptional performance and margin for 2.5 Gbps and 3.125 Gbps switching applications.
- ▶ Advanced ISE ('Eye Opener') capabilities to reduce Inter Symbol Interference (ISI) due to PCB losses and/or copper cable losses to enable longer back planes or shelf to shelf interconnects.
- ▶ BIST (System) features Enable Simplified Design, Verification, Production Testing at the Board or System Level, and in Application Signal Monitoring.
- ▶ Enhanced Signal Integrity and Package Design for Ease of PCB Design

**APPLICATIONS:**

- ▶ Large 3 Stage CLOS Fabrics of up to 2,880x2,880 I/O Ports with up to 10Tb/s of Data Throughput
- ▶ DWDM Switches
- ▶ Wavelength Routers
- ▶ Storage Area Network (SAN) Switch Fabrics
- ▶ Packet Switching Fabrics

**MARKETS:**

- ▶ Core and Metro Transport
- ▶ Enterprise
- ▶ High-Speed Automated Test Equipment
- ▶ Broadcast Video

**SPECIFICATIONS:**

- ▶ 3.6 Gbps NRZ Data Rate
- ▶ 2.5V Power Supply [2.5V/3.3V Program Port Power Supply]
- ▶ 2.5V/3.3V CMOS TTL Compatible I/O
- ▶ Differential CML I/O with Integrated Termination Impedance
- ▶ 4.4W Typical Power Dissipation with Output Levels
- ▶ 33x33mm, 1.27mm Pitch, 613 BGA Package
- ▶ 0°C to +85°C Operating Temperature Range

# VSC3139

## 4.2 Gbps 72 x 72 Asynchronous Crosspoint Switch

### GENERAL DESCRIPTION:



The VSC3139 is a 72x72 asynchronous crosspoint switch, designed to carry broadband data streams. The fully non-blocking switch core is programmed through a multi-mode port interface that allows random access programming of each input/output port. A high degree of signal integrity is maintained throughout the chip by fully differential signal paths.

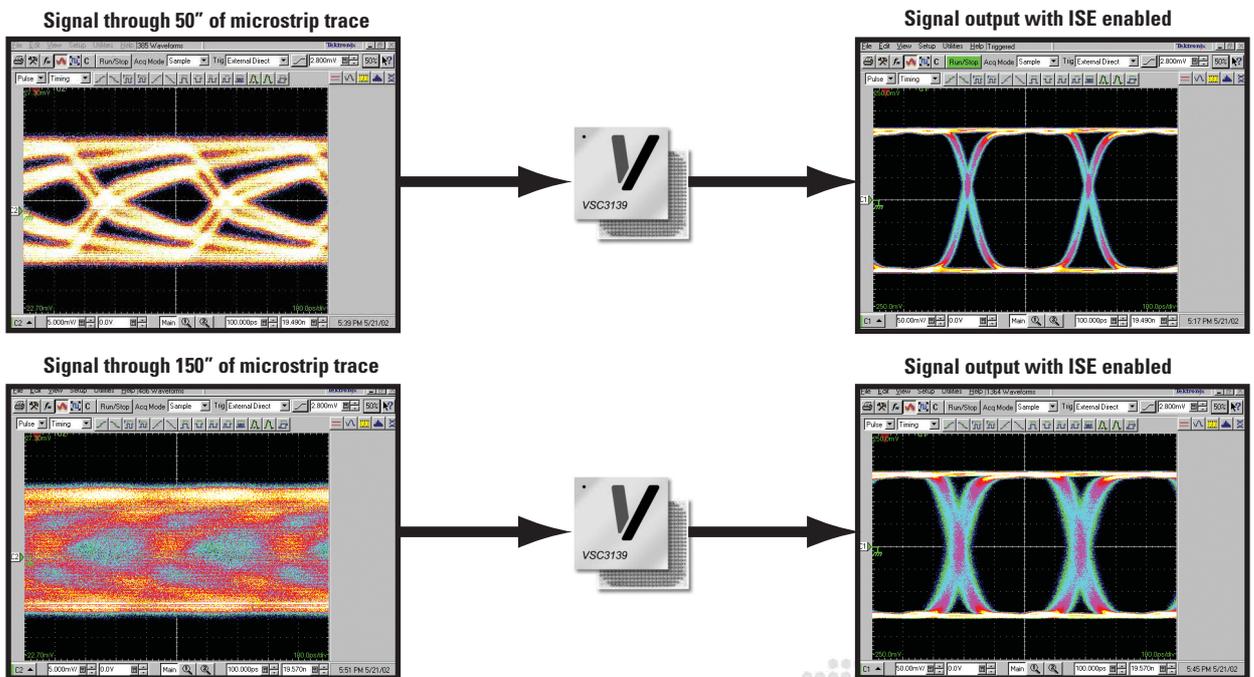
Each data output can be programmed to connect to one of the 72 inputs. The signal path is unregistered and fully asynchronous, so there are not any restrictions on the phase, frequency, or signal pattern on any input. Each high-speed output is a fully differential switched current driver with on-die terminations for maximum signal integrity. Data inputs are terminated on die through 100Ω resistors between true and complement inputs with a common connection to an internal bias source, facilitating AC-coupling to the switch inputs.

A multi-mode, programming interface is provided that allows commands to be sent as serial data or multiplexed parallel

data. Core programming can be sequential on a port by port basis, or multiple program assignments can be queued and issued simultaneously using the CONFIG bit. The INIT feature will reset the entire switch into a "straight-through" configuration (A0 to Y0, A1 to Y1, etc.) or it can be programmed by the user to initialize to any other configuration. Programming of the VSC3139 is via an 11-bit multiplexed ADDR/DATA bus in conjunction with the ALE, RD, WR, CONFIG and INIT pins. Additionally, the CONFIG and INIT signals can be set via an internal control register to reduce the number of signals required to interface with the switch. To lock-in programming of switch connections, INIT, and CONFIG can be disabled through software.

Unused channels may be powered down to allow efficient use of the switch in applications that require only a subset of the channels. Power-down is enabled in software by programming individual unused outputs with a power-down code. A secondary access port allows asynchronous readback and configuration control to take place while the primary programming port is in use.

### EYE OPENER INPUT SIGNAL EQUALIZATION PERFORMANCE:



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