



32K X 8 SRAM

FEATURES

- Access times of 12,15,20 ns
- Fast output enable (t_{DOE}) for cache applications
- Low active power: 400 mW (Typical)
- Low standby power
- Fully static operation, no clock or refresh required
- TTL Compatible Inputs and Outputs
- TSOP (only) offered in "reverse" TSOP package for easy 2-sided board assembly
- Single +5V power supply
- Industrial and military temperature range

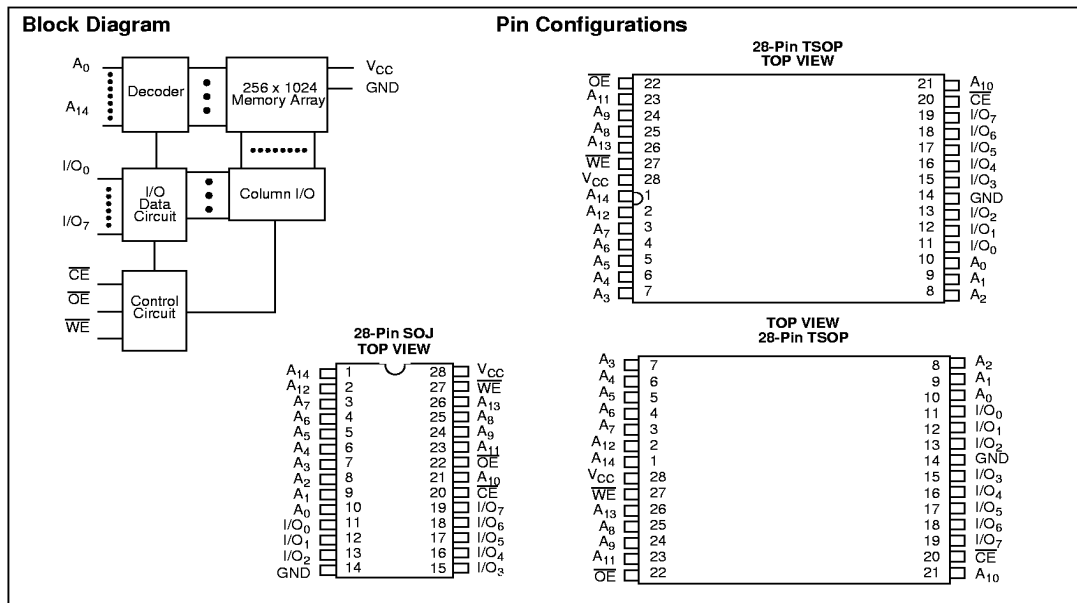
FUNCTIONAL DESCRIPTION

The ASSI AS5C2568DJ is a high speed, low power, 32,768 word by 8-bit CMOS static RAM. It is fabricated using ASI's high performance CMOS, double metal technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 12 ns (Max).

When Chip Enable (\overline{CE}) is HIGH, the device assumes a standby mode at which the power dissipation can be reduced down to 10 μ W (typical) at CMOS input levels.

Easy memory expansion is provided by using asserted LOW \overline{CE} and asserted LOW output enable inputs (\overline{OE}). The asserted LOW write enable (\overline{WE}) controls both writing and reading of the memory.

The AS5C2568DJ is pin-compatible with other 32K X 8 SRAM's in the SOJ, and TSOP package.



**ABSOLUTE MAXIMUM RATINGS**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....-65°C to +150°C

Ambient Temperature

with Power Applied.....-55°C to +125°C

V_{CC} Supply Relative to GND.....-1.0V to +7.0V
Voltage on Any

Pin Relative to GND.....-0.5V to V_{CC} +0.5V

Short Circuit Output Current².....±50mA

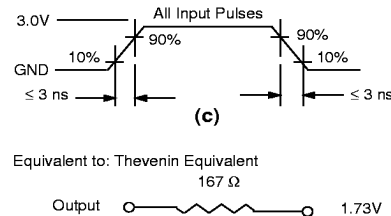
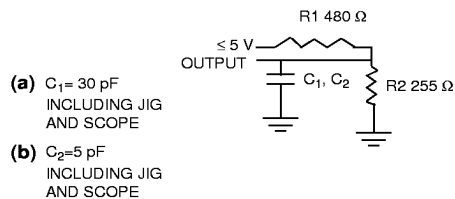
Power Dissipation.....1.0 W

ELECTRICAL CHARACTERISTICS Over the operating Range (-40°C ≤ T ≤ 85°C; V_{CC} = 5V ± 10%)-Industrial Temps.

Symbol	Parameter	Test Conditions	AS5C2568DJ-15		AS5C2568DJ-20		Unit
			Min.	Max.	Min.	Max.	
I _{CC1}	Dynamic Operating Current	V _{CC} = MAX, I _{OUT} = mA, CE = V _{IL} , f = f _{max}		150		140	mA
I _{CC2}	Operating Current	V _{CC} = MAX, I _{OUT} = mA, CE = V _{IL} , f = 0		100		100	mA
I _{SB1}	TTL Standby Current -TTL Inputs	V _{CC} = MAX, V _{IN} = V _{IH} or V _{IL} , CE V _{IH} , f = f _{max}		30		30	mA
I _{SB2}	CMOS Standby Current -CMOS Inputs	V _{CC} = MAX, CE ≤ V _{CC} -0.2V, V _{IN} ≤ V _{CC} -0.2V or V _{IN} ≤ 0.2V f = 0		15		15	mA
I _{LI}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-1	1	-1	1	μA
I _{LO}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} Output Disabled	-1	1	-1	1	μA
V _{OH}	Output High Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output Low Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input High Voltage		2.2	V _{CC} +0.5	2.2	V _{CC} +0.5	V
V _{IL}	Input Low Voltage		-0.5	0.8	-0.5	0.8	V

Capacitance⁴

Symbol	Description	Max.	Unit
C _{IN}	Input Capacitance	5	pF
C _{IO}	I/O Capacitance	5	pF

AC Test Loads and Waveforms**Notes:**

1. No more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

2. Tested initially and after any design or process changes that may effect these parameters.

3. V_{IL} = -3.0 V for pulse width less than 3 ns.

**Electrical Characteristics** Over the operating Range ($-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$; $V_{CC} = 5V \pm 10\%$)-Military Temps.

Symbol	Parameter	Test Conditions	AS5C2568DJ-20		Unit
			Min.	Max.	
ICC1	Dynamic Operating Current	$V_{CC} = \text{Max.}, I_{OUT} = \text{mA}, \overline{CE} = V_{IL}, f = f_{\text{max}}$		145	mA
ICC2	Operating Current	$V_{CC} = \text{Max.}, I_{OUT} = \text{mA}, \overline{CE} = V_{IL}, f = 0$		105	mA
ISB1	TTL Standby Current -TTL Inputs	$V_{CC} = \text{Max.}, V_{IN} = V_{IH} \text{ or } V_{IL}, \overline{CE} \geq V_{IH}, f=f_{\text{max}}$		60	mA
ISB2	CMOS Standby Current -CMOS Inputs	$V_{CC} = \text{Max.}, \overline{CE} \geq V_{CC} - 0.2V, V_{IN} \geq V_{CC} - 0.2V \text{ or } V_{IN} \leq 0.2V, f = 0$		30	mA
ILI	Input Leakage Current	$GND \leq V_{IN} \leq V_{CC}$	-1	1	mA
ILO	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ Output Disabled	-1	1	mA
VOH	Output High Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		V
VOL	Output Low Voltate	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4	V
VIH	Input High Voltage		2.2	$V_{CC} + 0.5$	V
VIL	Input Low Voltage		-0.5	0.8	V

**Switching Characteristics** Over the operating Range (-12 and -15, -40°C To +85°C) (-20, -55°C To +125°C)

Parameter	Description	AS5C2568DJ-12		AS5C2568DJ-15		AS5C2568DJ-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t _{RC}	Read Cycle Time	12		15		20		ns
t _{AA}	Address Access Time		12		15		20	ns
t _{OHA}	Output Hold Time	3		3		3		ns
t _{ACE1} , t _{ACE2}	\overline{CE} Access Time		12		15		20	ns
t _{DOE}	\overline{OE} Access Time		5		7		8	ns
t _{LZOE}	\overline{OE} to Low-Z Output	0		0		0		ns
t _{HZOE} ²	\overline{OE} to High-Z Output		5		6		7	ns
t _{LZCE1} , t _{LZCE2}	\overline{CE} to Low-Z Output	3		3		3		ns
t _{HZCE1} , t _{HZCE2}	\overline{CE} to High-Z Output		6		8		9	ns
t _{PU}	\overline{CE} to Power Up	0		0		0		ns
t _{PD}	\overline{CE} to Power Down		12		15		20	ns
Write Cycle ³								
t _{w c}	Write Cycle Time	12		15		20		ns
t _{SCE1} , t _{SCE2}	\overline{CE} to Write End	8		10		12		ns
t _{AW}	Address to Set-up Time to Write End	8		10		12		ns
t _{HA}	Address Hold to Write End	0		0		0		ns
t _{SA}	Address Set-up Time	0		0		0		ns
t _{pw e1} ⁴	\overline{WE} Pulse Width (\overline{OE} = HIGH)	8		10		12		ns
t _{pw e2}	\overline{WE} Pulse Width (\overline{OE} = LOW)	12		12		15		ns
t _{SD}	Data Set-up to Write End	6		7		10		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{HZWE} ²	\overline{WE} LOW to High-Z Output		7		7		9	ns
t _{LZWE}	\overline{WE} HIGH to Low-Z Output	2		2		2		ns

Notes:

- Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 - 3.0 V and output loading specified in AC Test Loads and Waveforms *Figure (a)*.
- Tested with the load in AC Test Loads and Waveforms *Figure (b)*.
- The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a write, but any signal can be deasserted to terminate the write. The Data Input Set-up

- and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
- Tested with \overline{OE} HIGH.
- \overline{WE} is HIGH for a Read Cycle.
- The device is continuously selected. $\overline{OE}, \overline{CE}_1 = V_{IL}$.
- Address is valid prior to or coincident with \overline{CE} LOW transitions.
- I/O will assume the High-Z state if $\overline{OE} = V_{IH}$.



PIN DESCRIPTION

A_0 - A_{14} : Address Inputs

These 15 address inputs select one of the 32,768 8-bit words in the RAM.

\overline{CE} : Chip Enable Input

\overline{CE} is asserted LOW. The Chip Enable is asserted LOW to read from or write to the device. If Chip Enable is deasserted, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

\overline{OE} : Output Enable Input

The Output Enable Input is asserted LOW. If the Output Enable

is asserted LOW while \overline{CE} is asserted (LOW) and \overline{WE} is deasserted (HIGH), data from the SRAM will be present on the I/O pins. The I/O pins will be in the high-impedance state when \overline{OE} is deasserted.

\overline{WE} : Write Enable Input

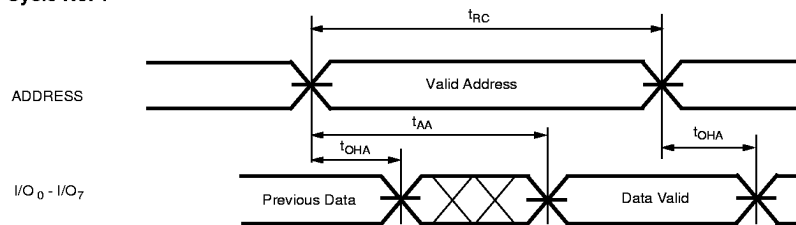
The Write Enable Input is asserted LOW and controls read and write operations. When \overline{CE} and \overline{WE} are both asserted (LOW) input data present on the I/O pins will be written into the selected memory location.

I/O_0 - I/O_7 : Common Input/Output Pins

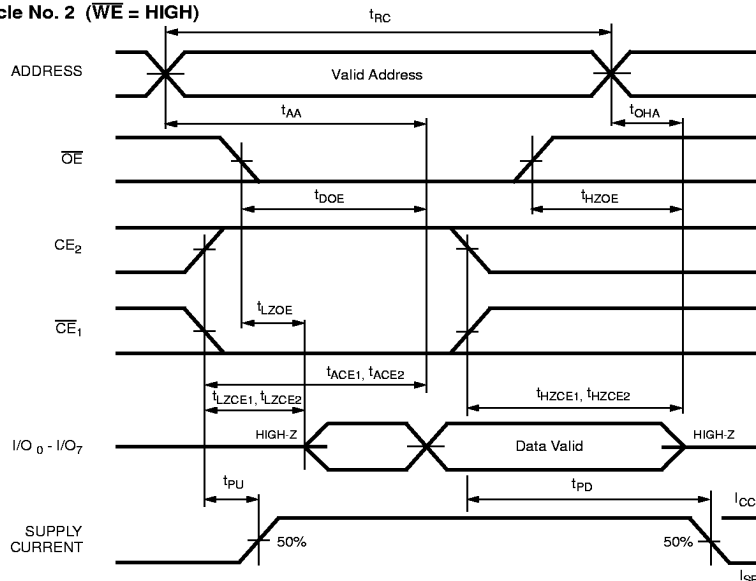
GND: Ground

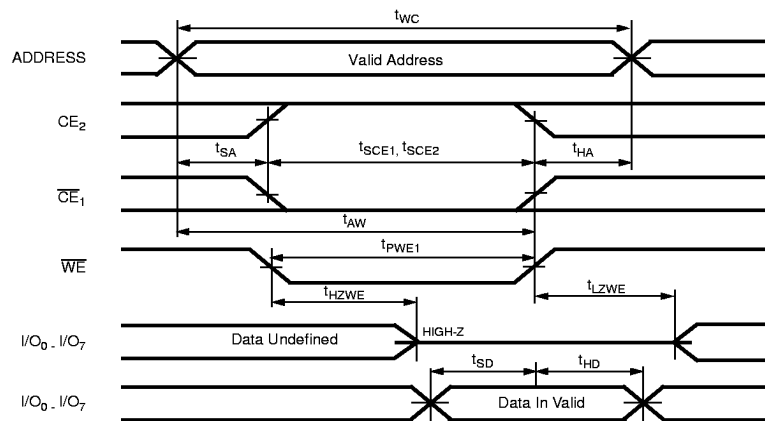
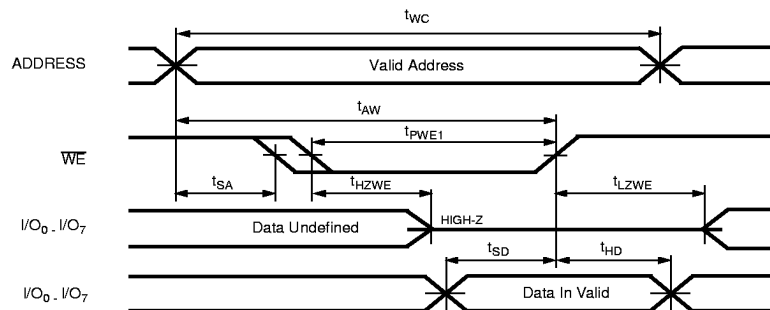
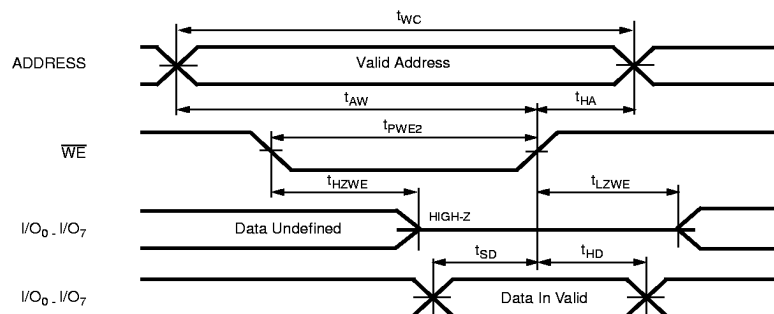
Switching Waveforms

Read Cycle No. 1



Read Cycle No. 2 ($\overline{WE} = \text{HIGH}$)



**Switching Waveforms** (continued)Write Cycle No.1 (\overline{CE}_1 , or CE_2 controlled, \overline{OE} is HIGH or LOW: \overline{CE}_1 or CE_2 Terminates Write)Write Cycle No.2 (\overline{WE} controlled, \overline{OE} is HIGH, \overline{CE}_1 is LOW, and CE_2 is HIGH: \overline{WE} Terminates Write)Write Cycle No.3 (\overline{WE} controlled, \overline{OE} is LOW, CE_2 is HIGH, \overline{CE}_1 is LOW: \overline{WE} Terminates Write)

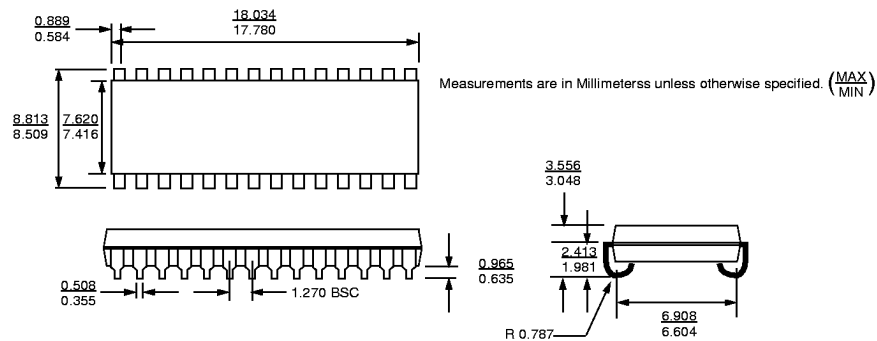


Truth Table

Mode	\overline{WE}	\overline{CE}	\overline{OE}	I/O	I_{CC}
Standby	X	H	X	High-Z	I_{SB1} , I_{SB2}
Standby	X	X	X	High-Z	I_{SB1} , I_{SB2}
Selected/Output Disabled	H	L	H	High-Z	I_{CC1} , I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1} , I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1} , I_{CC2}

Package Diagrams

28-Pin Small Outline J-Bend (SOJ)



28-Pin Thin Small Outline Package (TSOP)

