

DATA SHEET

BUK107-50DS PowerMOS transistor Logic level TOPFET

Product specification
Supersedes data of September 1994
File under Discrete Semiconductors, SC13a

March 1997

PowerMOS transistor
Logic level TOPFET

BUK107-50DS

DESCRIPTION

Monolithic overload protected logic level power MOSFET in a surface mount plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

- General controller for driving
- lamps
 - small motors
 - solenoids

FEATURES

- Vertical power DMOS output stage
- Overload protected up to 85°C ambient
- Overload protection by current limiting and overtemperature sensing
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	0.7	A
P_D	Total power dissipation	1.8	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	200	mΩ

FUNCTIONAL BLOCK DIAGRAM

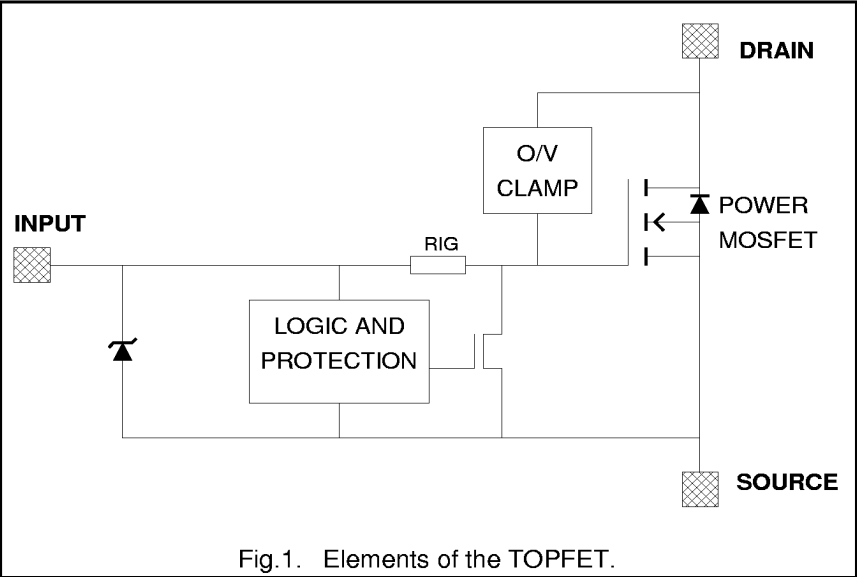
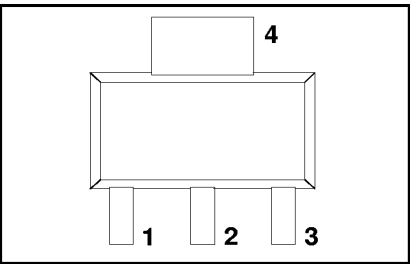


Fig.1. Elements of the TOPFET.

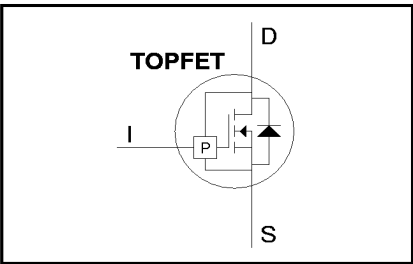
PINNING - SOT223

PIN	DESCRIPTION
1	input
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



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LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage ¹	-	-	50	V
I_D	Continuous drain current ²	-	-	self limiting	A
I_I	Continuous input current	clamping	-	3	mA
I_{IRM}	Non-repetitive peak input current	$t_p \leq 1$ ms	-	10	mA
P_D	Total power dissipation	$T_{amb} = 25$ °C	-	1.8	W
T_{stg}	Storage temperature	-	-55	150	°C
T_J	Continuous junction temperature	normal operation ³	-	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; $C = 250$ pF; $R = 1.5$ k Ω	-	2	kV

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{DSM}	Non-repetitive clamping energy	$T_b \leq 25$ °C; $I_{DM} < I_{D(lim)}$; inductive load	-	100	mJ
E_{DRM}	Repetitive clamping energy	$T_b \leq 75$ °C; $I_{DM} = 50$ mA; $f = 250$ Hz	-	4	mJ

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from short circuit loads.
Overload protection operates by means of drain current limiting and activating the overtemperature protection.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDP}	Protected drain source supply voltage	$V_{IS} = 5$ V	-	35	V
		$V_{IS} = 4$ V	-	16	V

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off to protect itself when there is an overload fault condition.
It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Overload protection					
$I_{D(lim)}$	Drain current limiting	$V_{IS} = 5$ V	0.7	1.1	1.5	A
$T_{J(TO)}$	Overtemperature protection Threshold junction temperature	only in drain current limiting $V_{IS} = 5$ V	100	130	160	°C

¹ Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

² Refer to OVERLOAD PROTECTION CHARACTERISTICS.

³ Not in an overload condition with drain current limiting.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance Junction to solder point		-	12	18	K/W
$R_{th\ j-b}$	Junction to board ¹	Mounted on any PCB	-	40	-	K/W
$R_{th\ j-a}$	Junction to ambient	Mounted on PCB of fig. 19	-	-	70	K/W

STATIC CHARACTERISTICS

$T_b = 25\ ^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	$V_{IS} = 0\ \text{V}$; $I_D = 10\ \text{mA}$	50	55	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	$V_{IS} = 0\ \text{V}$; $I_{DM} = 200\ \text{mA}$; $t_p \leq 300\ \mu\text{s}$; $\delta \leq 0.01$	-	56	70	V
I_{DSS}	Off-state drain current	$V_{DS} = 45\ \text{V}$; $V_{IS} = 0\ \text{V}$	-	0.5	2	μA
I_{DSS}	Off-state drain current	$V_{DS} = 50\ \text{V}$; $V_{IS} = 0\ \text{V}$	-	1	20	μA
I_{DSS}	Off-state drain current	$V_{DS} = 40\ \text{V}$; $V_{IS} = 0\ \text{V}$; $T_j = 100\ ^\circ\text{C}$	-	10	100	μA
$R_{DS(ON)}$	Drain-source on-state resistance ²	$V_{IS} = 5\ \text{V}$; $I_{DM} = 100\ \text{mA}$; $t_p \leq 300\ \mu\text{s}$; $\delta \leq 0.01$	-	150	200	m Ω

INPUT CHARACTERISTICS

$T_b = 25\ ^\circ\text{C}$ unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	$V_{DS} = 5\ \text{V}$; $I_D = 1\ \text{mA}$	1.7	2.2	2.7	V
I_{IS}	Input supply current	normal operation; $V_{IS} = 5\ \text{V}$	-	330	450	μA
		$V_{IS} = 4\ \text{V}$	-	170	270	μA
I_{ISL}	Input supply current	protection latched; $V_{IS} = 5\ \text{V}$	-	500	650	μA
		$V_{IS} = 3.5\ \text{V}$	-	250	400	μA
V_{ISR}	Protection latch reset voltage ³		1	2.2	3.5	V
$V_{(CL)IS}$	Input clamping voltage	$I_l = 1.5\ \text{mA}$	6	7.5	-	V
R_{IG}	Input series resistance	to gate of power MOSFET	-	33	-	k Ω

SWITCHING CHARACTERISTICS

$T_{amb} = 25\ ^\circ\text{C}$; resistive load $R_L = 50\ \Omega$; adjust V_{DD} to obtain $I_D = 250\ \text{mA}$; refer to test circuit and waveforms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{don}	Turn-on delay time	$V_{IS} = 0\ \text{V}$ to $V_{IS} = 5\ \text{V}$	-	8	-	μs
t_r	Rise time		-	30	-	μs
t_{doff}	Turn-off delay time	$V_{IS} = 5\ \text{V}$ to $V_{IS} = 0\ \text{V}$	-	3	-	μs
t_f	Fall time		-	6	-	μs

¹ Temperature measured 1.3 mm from tab.

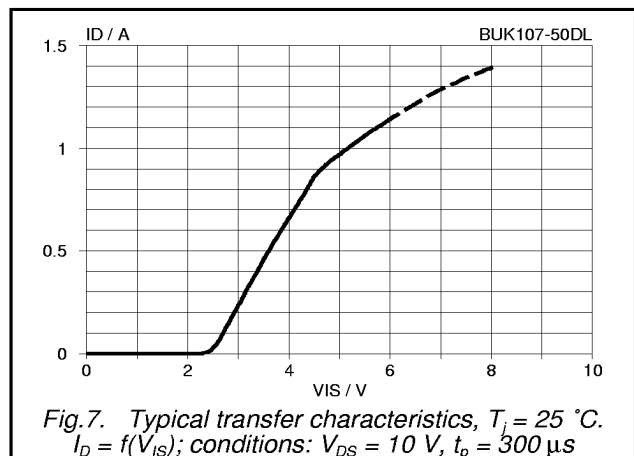
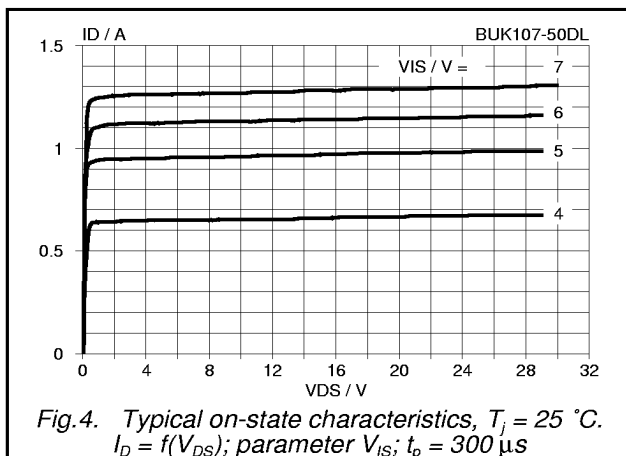
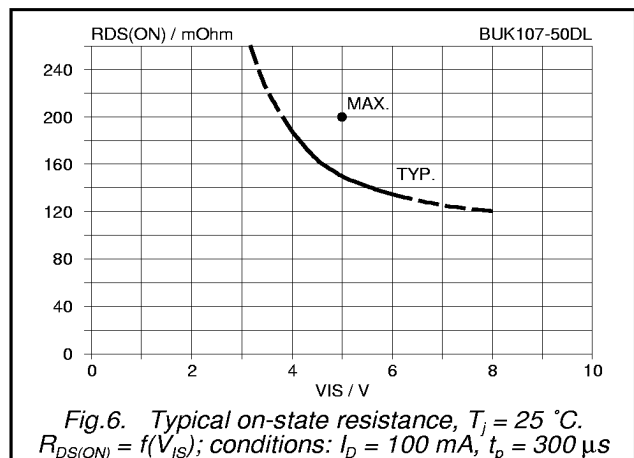
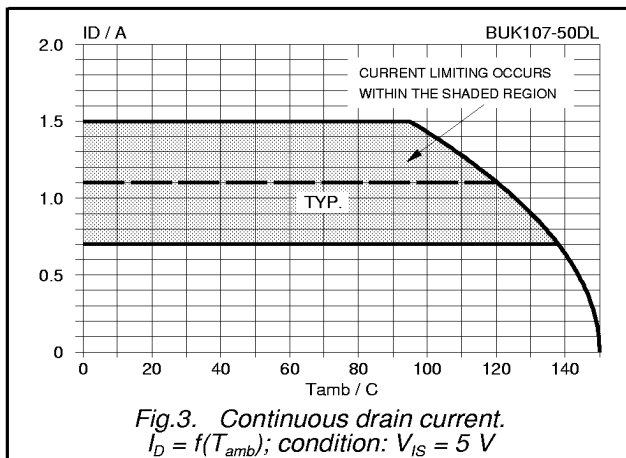
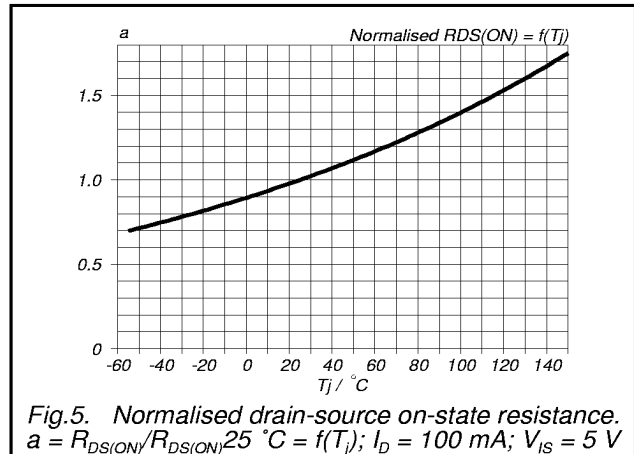
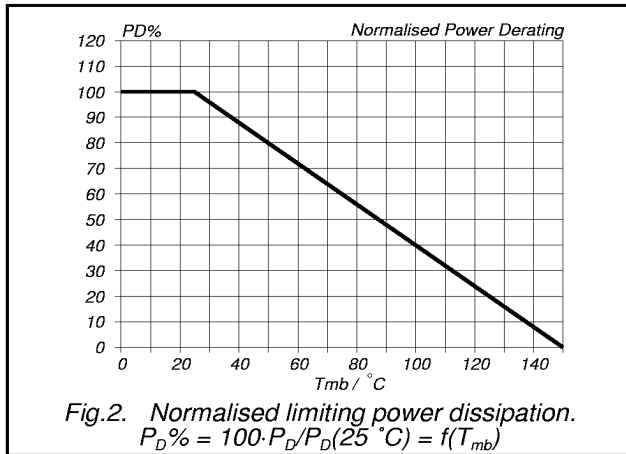
² Continuous input voltage. The specified pulse width is for the drain current.

³ The input voltage below which the overload protection circuits will be reset.

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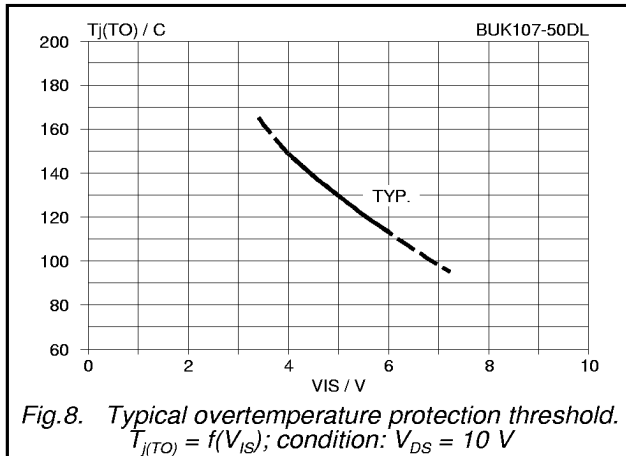


Fig. 8. Typical overtemperature protection threshold.
 $T_{j(TO)} = f(V_{IS})$; condition: $V_{DS} = 10\text{ V}$

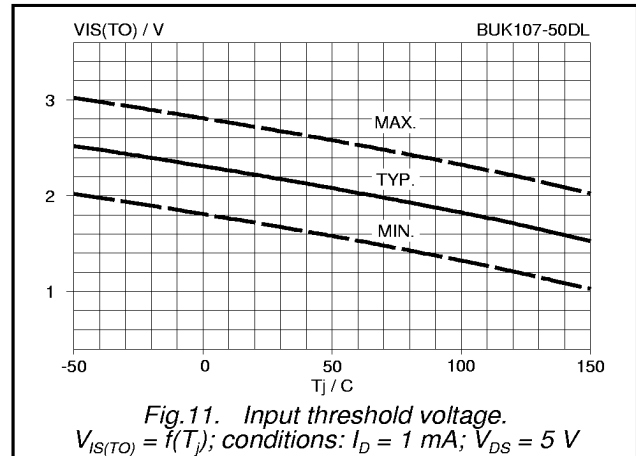


Fig. 11. Input threshold voltage.
 $V_{IS(TO)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = 5\text{ V}$

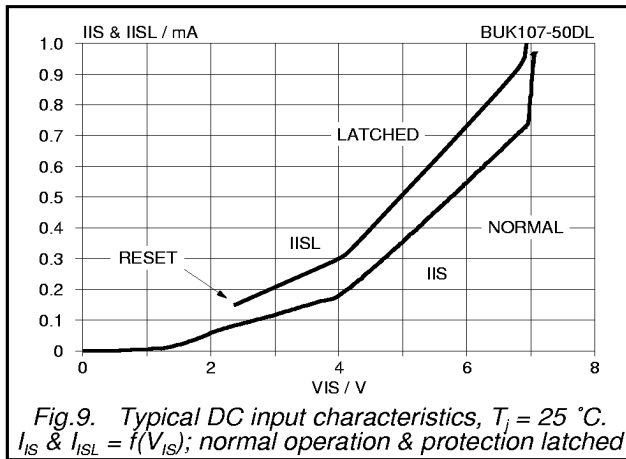


Fig. 9. Typical DC input characteristics, $T_j = 25^\circ\text{C}$.
 I_{IS} & $I_{ISL} = f(V_{IS})$; normal operation & protection latched

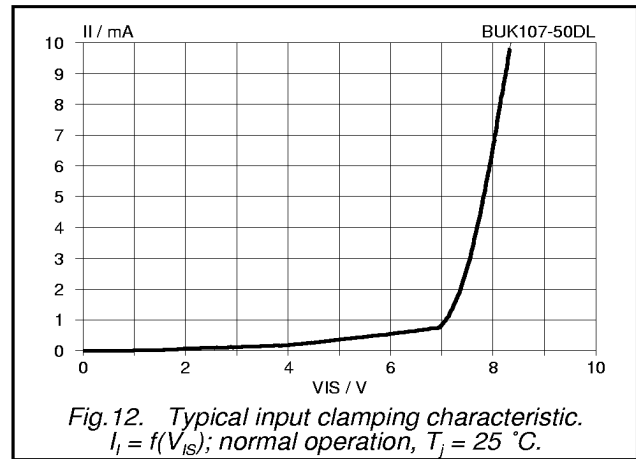


Fig. 12. Typical input clamping characteristic.
 $I_i = f(V_{IS})$; normal operation, $T_j = 25^\circ\text{C}$.

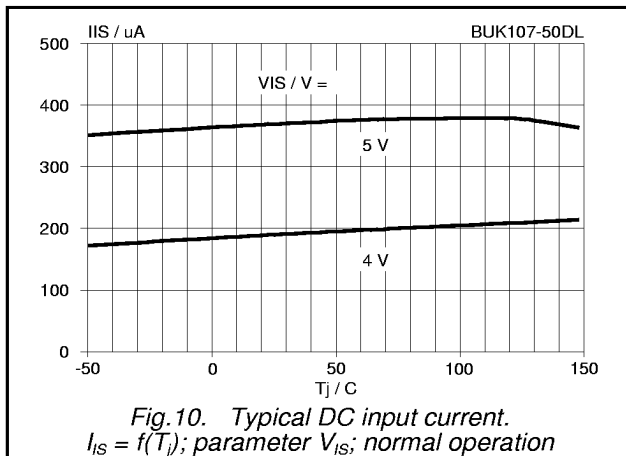


Fig. 10. Typical DC input current.
 $I_{IS} = f(T_j)$; parameter V_{IS} ; normal operation

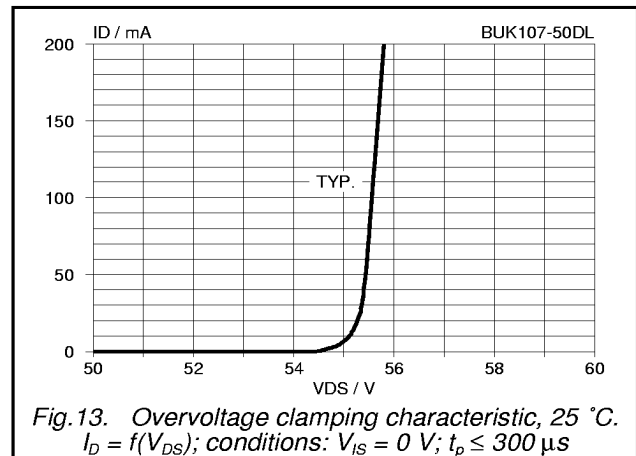
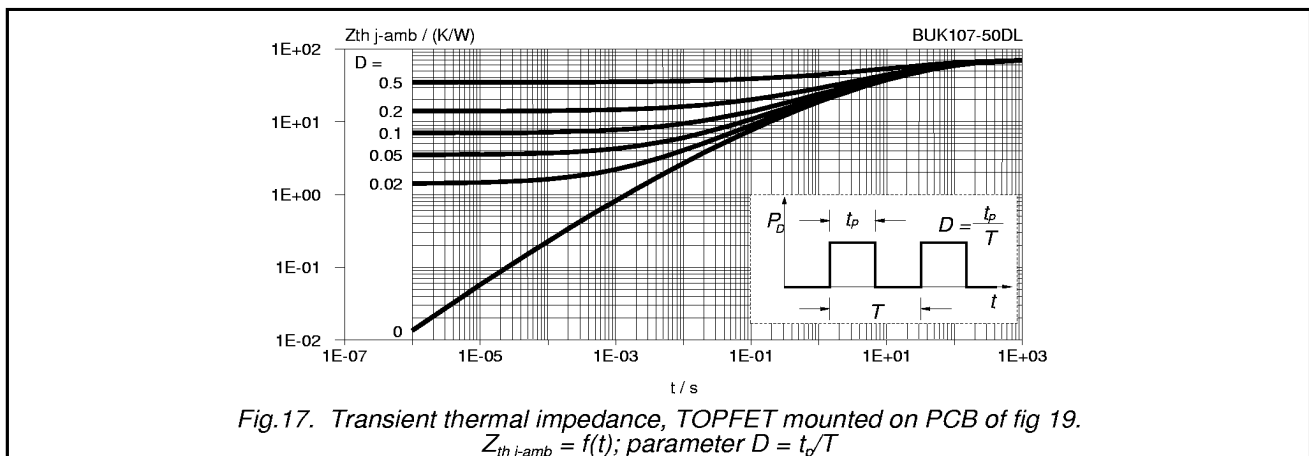
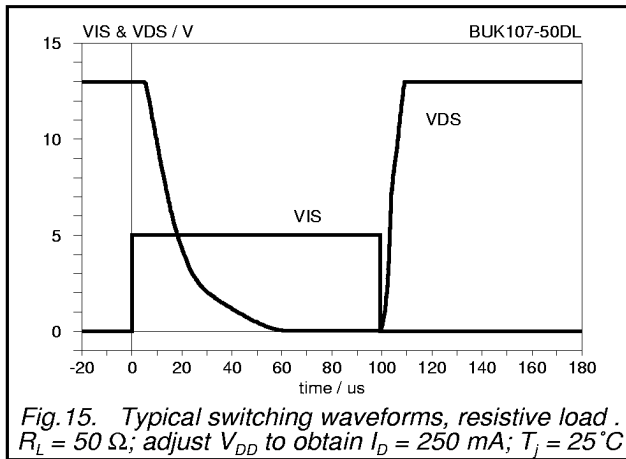
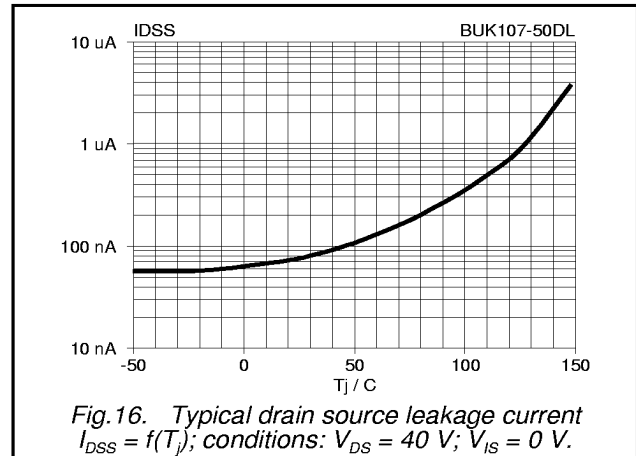
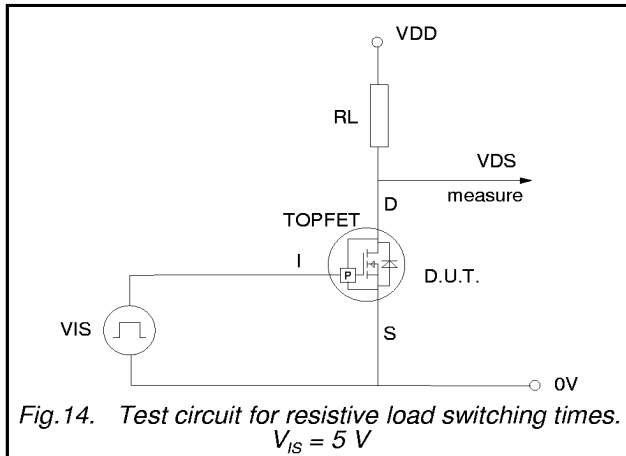


Fig. 13. Overvoltage clamping characteristic, 25°C .
 $I_D = f(V_{DS})$; conditions: $V_{IS} = 0\text{ V}$; $t_p \leq 300\text{ }\mu\text{s}$

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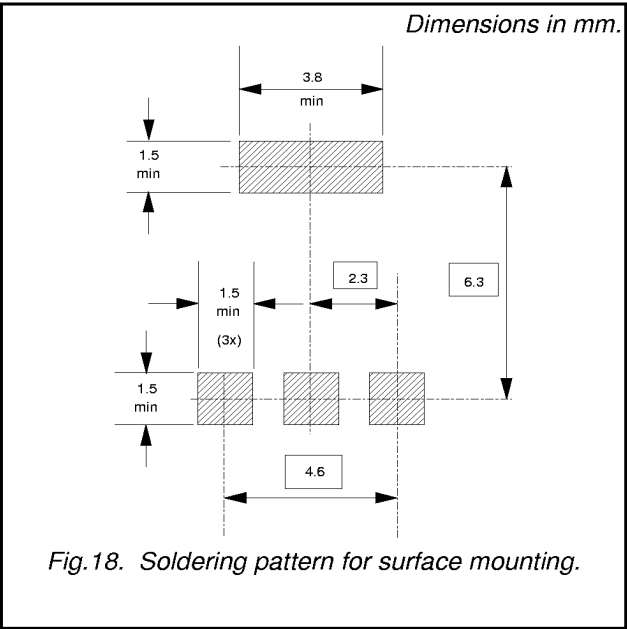
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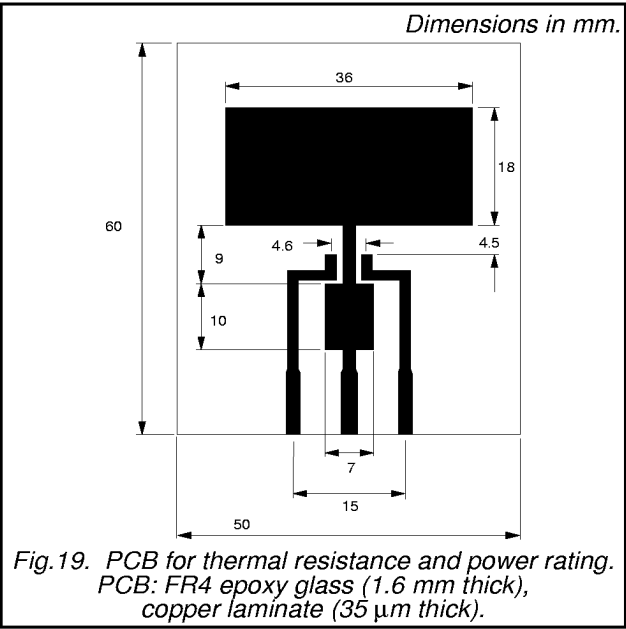
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MOUNTING INSTRUCTIONS



PRINTED CIRCUIT BOARD



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MECHANICAL DATA

Dimensions in mm

Net Mass: 0.11 g

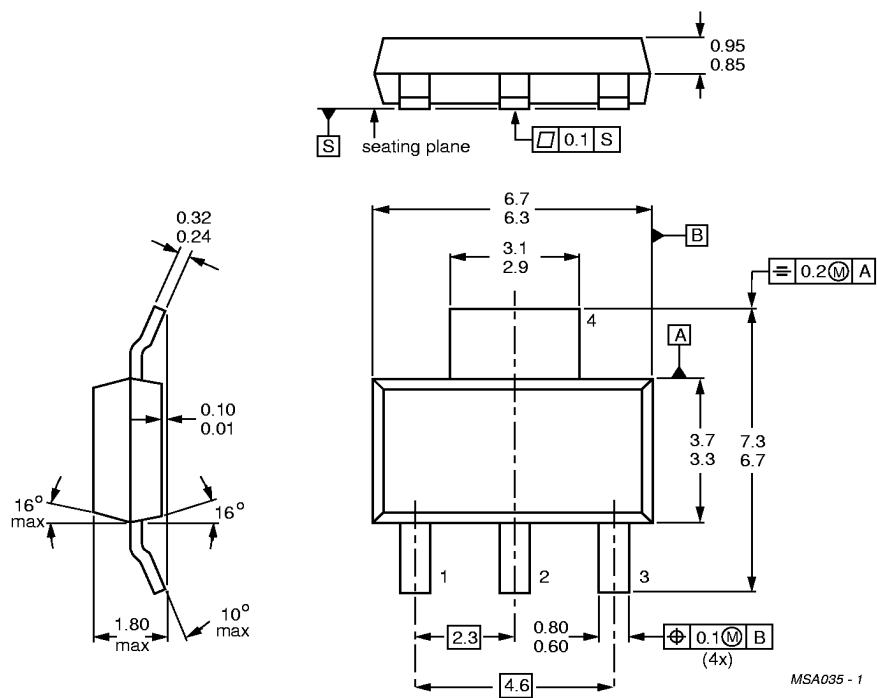


Fig.20. SOT223 surface mounting package¹.

1 For further information, refer to surface mounting instructions for SOT223 envelope. Epoxy meets UL94 V0 at 1/8".