T-52-33-05

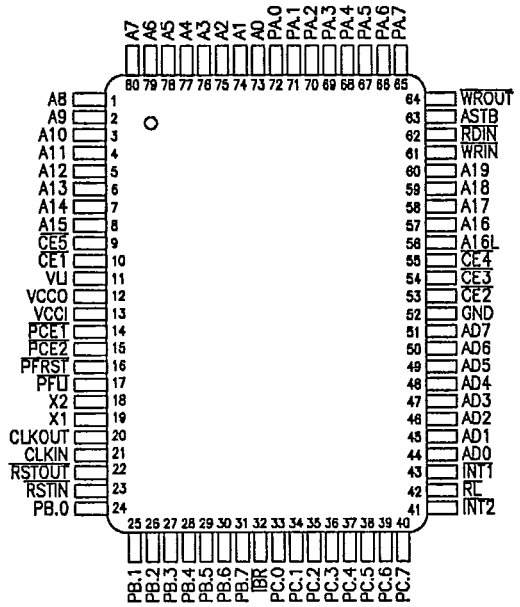
DALLAS SEMICONDUCTOR

DS5340
V40 Softener Chip

FEATURES

- Provides softness for V40-based systems
- Adapts to task-at-hand:
  - -Converts up to 672K bytes of CMOS SRAM into lithium-backed NV program/data storage
  - -Serial bootstrap loading
  - -Code can be changed in end use
- Crashproof operation during transient conditions
- Provides 3 enhanced 8-bit parallel I/O ports

PIN DESCRIPTION



80-Pin Quad Flat Pack

DESCRIPTION

The DS5340 V40 Softener Chip provides the benefits of adaptability, crashproof operation, and enhanced parallel I/O capabilities, as discussed in the DS53xx Micro Softener Chips family data sheet, for systems based on the popular NEC V40 microprocessor. The DS5340 interfaces directly to the V40's address/data bus and control signals and converts up to 672K bytes of CMOS SRAM into nonvolatile read/write storage.

An embedded control system with the above attributes can be implemented using only the V40, DS5340 V40 Softener Chip, CMOS static RAM, and a lithium cell. Additional peripheral functions, such as a permanently powered clock/calendar function (using the DS1283 Watchdog Timekeeper Chip) can be added to the system without the need for additional glue logic. Because the V40 is code-compatible with the 8086, application code can be developed on

a PC in its native instruction set. As a result, a multitude of high-level language compilers, assemblers, and debugging packages are available to support development of a V40/DS5340-based embedded control system.

Also available from Dallas Semiconductor is the DS2340 Soft V40 Flip Stik, which is a complete implementation of the embedded control system described above. The DS2340 is implemented as a small daughterboard that plugs into an industry-standard 72-pin SIMM connector scheme that supports redundant contacts, simple insertion/extraction, and low overall height profiles. The DS2340 can be used as a high-level building block in a system design resulting in a quick time to market for a Softener-based V40 system. Alternatively, it can be used for fast prototyping of a system which will ultimately incorporate the DS5340 V40 Softener Chip itself. Consult the DS2340 data sheet for information on this application of the DS5340.

PIN DESCRIPTION

The table shown below summarizes the pin functions of the DS5340 by function type.

DS5340 PIN DESCRIPTION Table 1

NAME	DESCRIPTION
V_{CCI}	+5V Power Supply Input
GND	Ground
V_{LI}	+3V Lithium Supply Input
V_{CCO}	Lithium-Backed Power Supply Output
PFRST\	Power Fail Reset Output
PFLI\	Power Fail Lithium Output
X1	Crystal Oscillator Input
X2	Crystal Oscillator Output
RL\	Reload Input
CLKIN	Clock Input from V40
CLKOUT	Clock Output
A19-A8	Address Bus Inputs from V40
A16L	Latched A16 Line; Output
AD7-AD0	Mux. Address/Data Bus to/from V40; bidirectional
ASTB	Address Strobe Input from V40

NAME	DESCRIPTION
MRDIN\	Memory Read Input from V40
MWRIN\	Memory Write Input from V40
A7-A0	Demux. Address Bus; Outputs
CE1\-CE5\	Chip Enable Outputs
PCE1\-PCE2\	Peripheral Chip Enable Outputs
WROUT\	Write Output
RSTIN\	Reset Input
RSTOUT\	Reset Output to V40
INT1\	Interrupt Output 1 to V40
INT2\	Interrupt Output 2 to V40
PA.7-PA.0	Port A; Bidirectional
PB.7-PB.0	Port B; Bidirectional
PC.7-PC.0	Port C; Bidirectional
IBR\	Input Buffer Ready Status Output

BLOCK DIAGRAM

A conceptual block diagram of the DS5340 is shown in Figure 1. Consult the DS53xx Micro Softener Chip family data sheet for complete operational details which are common to all of the versions of the Micro Softener. Features unique to the DS5340 are described below.

MEMORY MAP

The DS5340 interfaces directly to the NEC V40's multiplexed address/data bus. All 20 address lines as well as the ASTB, MRD\, and MWR\ control signals are monitored so that all memory accesses performed by the V40 are interpreted by the DS5340. The V40 Softener Chip decodes incoming addresses and controls access to its internal registers, to external CMOS SRAMs, and to external peripherals such as the DS1283 Watchdog Timekeeper Chip.

CE1\-CE5\ are the chip enable signals used to control the external CMOS SRAMs. The decoding of the chip enable signals is controlled by programming mode control bits within the DS5340 during system initialization via the bootstrap loader. Through selection of these modes, the chip enable outputs can be assigned to control various combinations of 32K x 8 and/or 128K x 8 CMOS SRAMs. This allows a minimum of 64K bytes of program/data storage up to a maximum of 672K bytes of program/data storage. This operating mode information is retained in the absence of V_{CC}.

As illustrated in Figure 2, five different system memory maps can be selected via the mode control bits. Mode 0 implements a contiguous 64K byte memory map for minimal system designs. Address bits A19-A16 are ignored when this mode is in effect. Both CE1\ and CE5\ are intended to be connected to the chip enable inputs of 32K x 8 CMOS SRAMs. CE2\,CE3\, and CE4\ are disabled when mode 0 is in effect. CE1\ is activated for all memory accesses from X0000H to X7FFFH, and CE5\ is activated for all memory accesses from X8000H to XFFFFH. The application program can be written to occupy the contiguous 64K byte area complete with interrupt vector information in the lowest portion of the map and with the reset information at the top portion of the map.

Modes 1-4 all decode the total 1M byte system memory map. As can be seen from the figure, Modes 1-3 select various combinations of 32K x 8 and/or 128K x 8 CMOS SRAMs under control of each of the chip enable signals CE1\-CE5\. When Mode 4 is selected, CE1\ and CE5\ select a 128K x 8 and a 32K x 8 CMOS SRAM, respectively, while CE2\ selects a 512K x 8 CMOS SRAM array. CE3\ and CE4\ are disabled in Mode 4.

As described in the DS53xx Micro Softener Chip family data sheet, the PCE1\ and PCE2\ lines are available for the interface of peripheral devices.

PARALLEL I/O

The DS5340 incorporates a total of three additional 8-bit parallel I/O ports which are easily accessed by the microprocessor. The ports are designated as A, B, and C. These ports function as described in the DS53xx data sheet.

BOOTSTRAP LOADER COMMANDS

The general function of the serial bootstrap loader is described in the DS53xx data sheet. In addition to the standard method of communication to a local PC via the V40's on-chip serial I/O port, the DS5340's serial bootstrap loader can be configured to communicate to a host PC at a remote location via a DS2245 Soft Modem Stik in the embedded system.

Extended Intel Hex representation is the format used to load program/data information into the nonvolatile SRAM of a V40/DS5340-based system. Extended Intel Hex is the typical format which is generated by existing 6803 assemblers.

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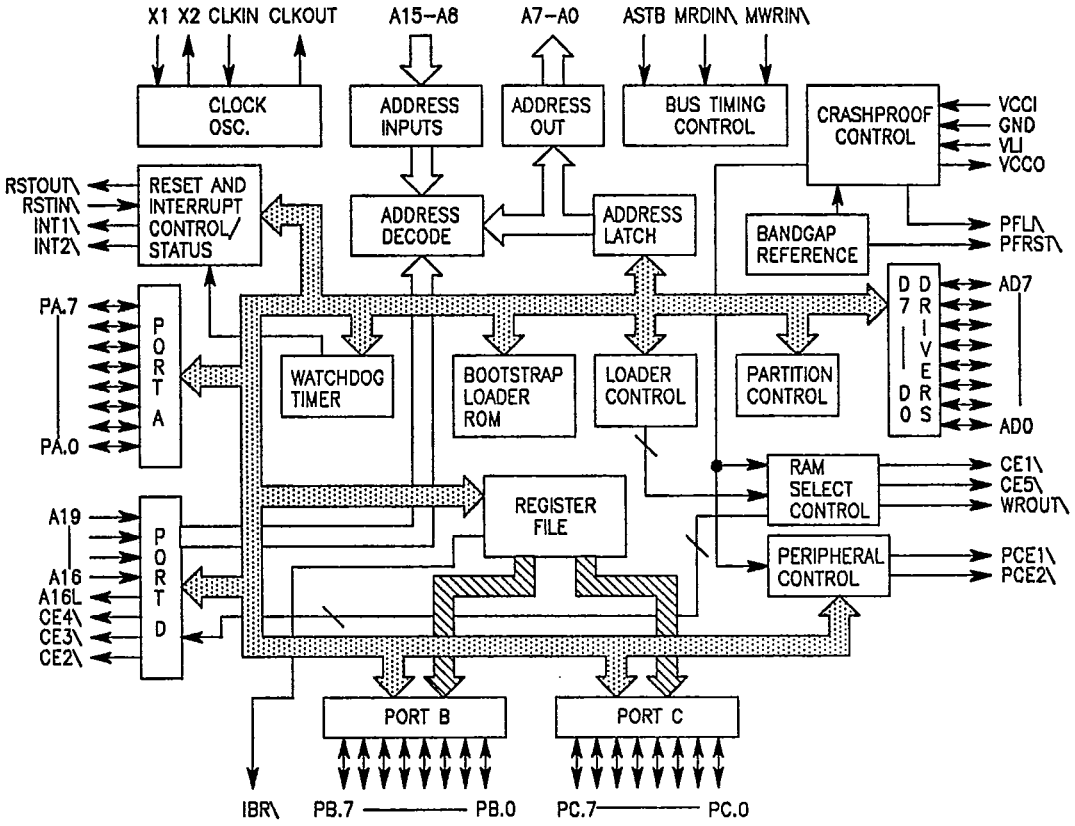
DS5340 V40 SOFTENER BLOCK DIAGRAM Figure 1



DS5340 SERIAL BOOTSTRAP LOADER Table 2

COMMAND	FUNCTION
C [range]	Calculate, store and report CRC-16 value
D [range]	Dump Extended Intel Hex
E	Exit Serial Bootstrap Loader
F val [range]	Fill NV SRAM with Constant
K	Clear CRC values
L	Load Extended Intel Hex
M	Enable/Disable Modem Communication
N	Set Freshness Seal
R	Read DS5340 Registers
V [range]	Verify Extended Intel Hex
W	Write DS5340 Register

A command summary specifically for the DS5340 serial bootstrap loader is given on the preceeding page (Table 2).

ORDERING INFORMATION

The following versions of the DS5340 are available as standard products from Dallas Semiconductor.

PART #	CLOCK	PACKAGE
DS5340FP	8 MHz	80-pin QFP
DS5340FP-A	10 MHz	80-pin QFP

FOR FURTHER INFORMATION

Complete technical specifications for the DS5340 as well as other versions of the Micro Softener and Soft Stik products are available on request from Dallas Semiconductor.

DS5340 MEMORY MAP MODES Figure 2