National Semiconductor

DS55325/DS75325 Memory Drivers

General Description

The DS55325 and DS75325 are monolithic memory drivers which feature high current outputs as well as internal decoding of logic inputs. These circuits are designed for use with magnetic memories.

The circuit contains two 600 mA sink-switch pairs and two 600 mA source-switch pairs. Inputs A and B determine source selection while the source strobe (S1) allows the selected source turn on. In the same manner, inputs C and D determine sink selection while the sink strobe (S2) allows the selected sink turn on.

Sink-output collectors feature an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This protects the outputs from voltage surges associated with switching inductive loads.

The source stage features Node R which allows extreme flexibility in source current selection by controlling the amount of base drive to each source transistor. This method of setting the base drive brings the power associated with the resistor outside the package thereby allowing the circuit to operate at higher source currents for a given junction temperature. If this method of source current setting is not desired, then Nodes R and R_{INT} can be shorted externally, activating an internal resistor connected from V_{CC2} to Node R. This provides adequate base drive for source currents up to 375 mA with V_{CC2} = 15V or 600 mA with V_{CC2} = 24V.

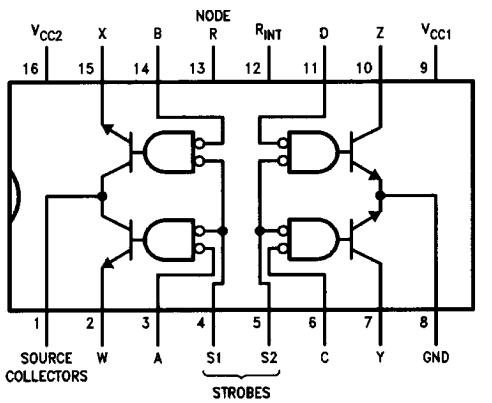
The DS55325 operates over the fully military temperature range of −55°C to +125°C, while the DS75325 operates from 0°C to +70°C.

Features

- 600 mA output capability
- 24V output capability
- Dual sink and dual source outputs
- Fast switching times
- Source base drive externally adjustable
- Input clamping diodes
- TTL compatible

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS55325J, DS75325J or DS75325N
See NS Package Number J14A or N14A

Truth Table

Address Inputs				Strobe Inputs		Outputs			
Source		Sink		Source	Sink	Source		Sink	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = High Level, L = Low Level, X = Irrelevant

Note: Not more than one output is to be on at any one time.

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC1} (Note 5)	7V
Supply Voltage V_{CC2} (Note 5)	25V
Input Voltage (Any Address or Strobe Input)	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate Cavity Package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Temperature (T_A)			
DS55325	−55	+125	°C
DS75325	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	*(Figures 1 and 2)*			2			V
V_{IL}	Low Level Input Voltage	*(Figures 3 and 4)*					0.8	V
V_I	Input Clamp Voltage	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{IN} = −12 mA, T_A = 25°C *(Figure 5)*				−1.3	−1.7	V
I_{OFF}	Source Collectors Terminal "Off" State Current	V_{CC1} = 4.5V, V_{CC2} = 24V *(Figure 1)*	Full Range	DS55325			500	μA
				DS75325			200	μA
			T_A = 25°C	DS55325		3	150	μA
				DS75325		3	200	μA
V_{OH}	High Level Sink Output Voltage	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{OUT} = 0 mA *(Figure 2)*			19	23		V
V_{SAT}	Saturation Voltage Source Outputs	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SOURCE} ≈ −600 mA *(Figure 3)* (Notes 4 and 6)	Full Range				0.9	V
			T_A = 25°C	DS55325		0.43	0.7	V
				DS75325		0.43	0.75	V
V_{SAT}	Saturation Voltage Sink Outputs	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SINK} ≈ 600 mA *(Figure 4)* (Notes 4 and 6)	Full Range				0.9	V
			T_A = 25°C	DS55325		0.43	0.7	V
				DS75325		0.43	0.75	V
I_I	Input Current at Maximum Input Voltage	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 5.5V *(Figure 5)*	Address Inputs				1	mA
			Strobe Inputs				2	mA
I_{IH}	High Level Input Current	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 2.4V *(Figure 5)*	Address Inputs			3	40	μA
			Strobe Inputs			6	80	μA
I_{IL}	Low Level Input Current	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 0.4V *(Figure 5)*	Address Inputs			−1	−1.6	mA
			Strobe Inputs			−2	−3.2	mA
$I_{CC\ OFF}$	Supply Current, All Sources and Sinks "Off"	V_{CC1} 5.5V, V_{CC2} = 24V, T_A = 25°C *(Figure 6)*	V_{CC1}			14	22	mA
			V_{CC2}			7.5	20	mA
I_{CC1}	Supply Current from V_{CC1}, Either Sink "On"	V_{CC1} = 5.5V, V_{CC2} = 24V, I_{SINK} = 50 mA, T_A = 25°C *(Figure 7)*				55	70	mA
I_{CC2}	Supply Current from V_{CC2}, Either Source "On"	V_{CC1} = 5.5V, V_{CC2} = 24V, I_{SOURCE} = −50 mA, T_A = 25°C *(Figure 8)*				32	50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55325 and across the 0°C to +70°C range for the DS75325. All typical values are at T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

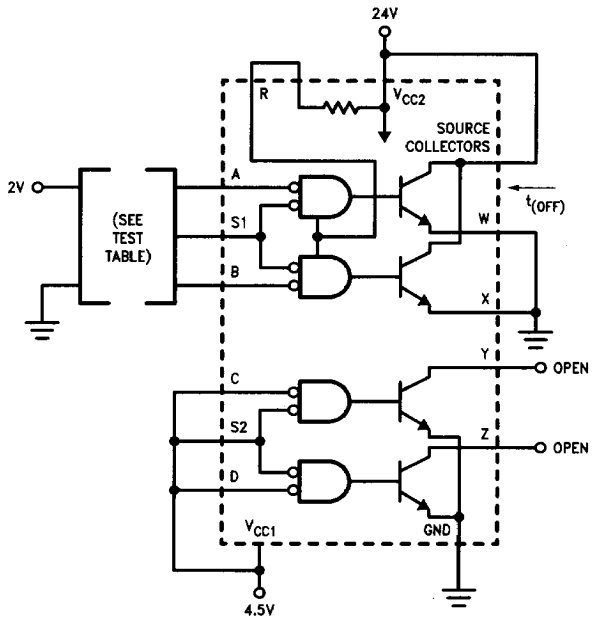
Note 5: Voltage values are with respect to network ground terminal.

Note 6: These parameters must be measured using pulse techniques. t_W = 200 μs, duty cycle ≤2%.

Switching Characteristics $V_{CC1} = 5V, T_A = 25°C$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$V_{CC2} = 15V, R_L = 24\Omega, C_L = 25$ pF *(Figure 9)*	Source Collectors		25	50	ns
			Sink Outputs		20	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$V_{CC2} = 15V, R_L = 24\Omega, C_L = 25$ pF *(Figure 9)*	Source Collectors		25	50	ns
			Sink Outputs		20	45	ns
t_{TLH}	Transition Time, Low-to-High Level Output	$C_L = 25$ pF	Source Outputs, $V_{CC2} = 20V$, $R_L = 1$ kΩ *(Figure 10)*		55		ns
			Sink Outputs, $V_{CC2} = 15V$, $R_L = 24\Omega$ *(Figure 9)*		7	15	ns
t_{THL}	Transition Time, High-to-Low Level Output	$C_L = 25$ pF	Source Outputs, $V_{CC2} = 20V$, $R_L = 1$ kΩ *(Figure 10)*		7		ns
			Sink Outputs, $V_{CC2} = 15V$, $R_L = 24\Omega$ *(Figure 9)*		9	20	ns
t_S	Storage Time, Sink Outputs	$V_{CC2} = 15V, R_L = 24\Omega, C_L = 25$ pF *(Figure 9)*			15	30	ns

DC Test Circuits



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Test Table

A	B	S1
GND	GND	2V
2V	2V	GND

FIGURE 1. I_{OFF}

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DC Test Circuits (Continued)

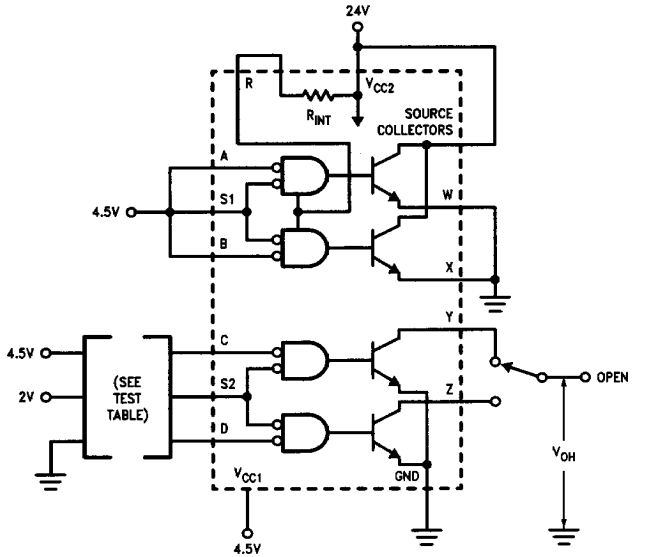

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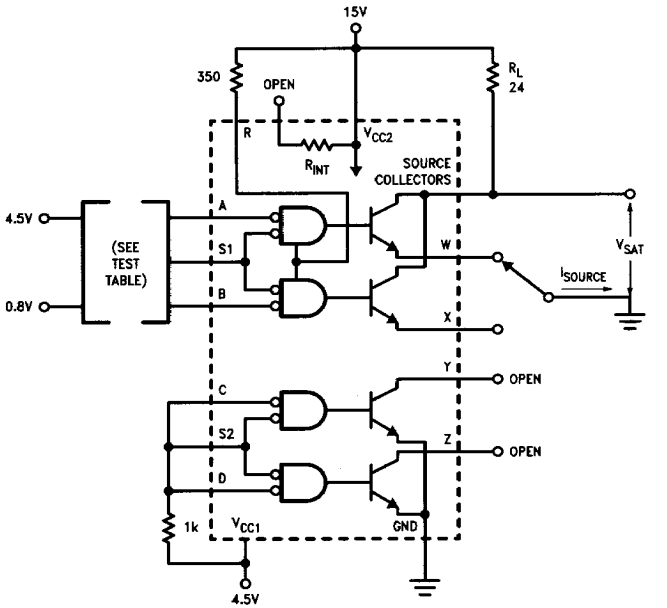
FIGURE 2. V_{IH} and V_{OH}

Test Table

C	D	S2	Y	Z
2V	4.5V	GND	V_{OH}	OPEN
GND	4.5V	2V	V_{OH}	OPEN
4.5V	2V	GND	OPEN	V_{OH}
4.5V	GND	2V	OPEN	V_{OH}



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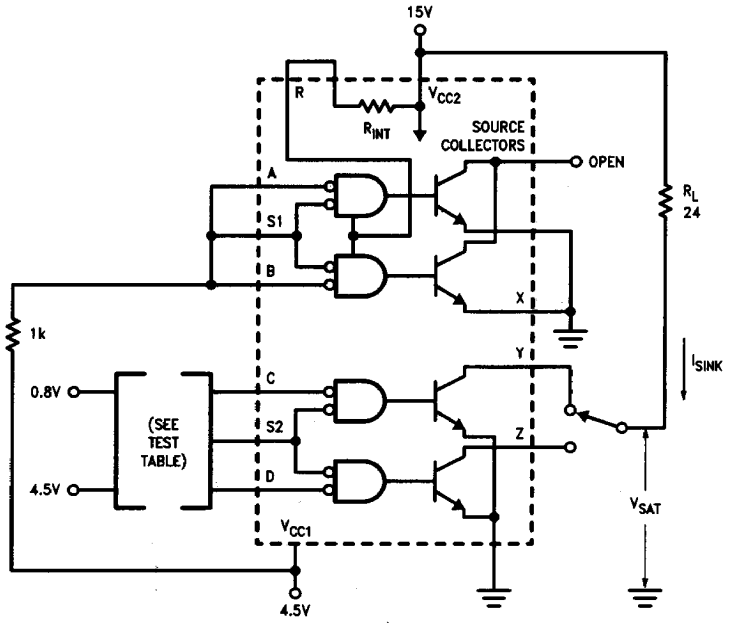
Test Table

A	B	S1	W	X
0.8V	4.5V	0.8V	GND	OPEN
4.5V	0.8V	0.8V	OPEN	GND

Note 1: *Figure 3* and *4* parameters must be measured using pulse techniques, t_W = 200 μs, duty cycle ≤ 2%.

FIGURE 3. V_{IL} and Source V_{SAT}

DC Test Circuits (Continued)



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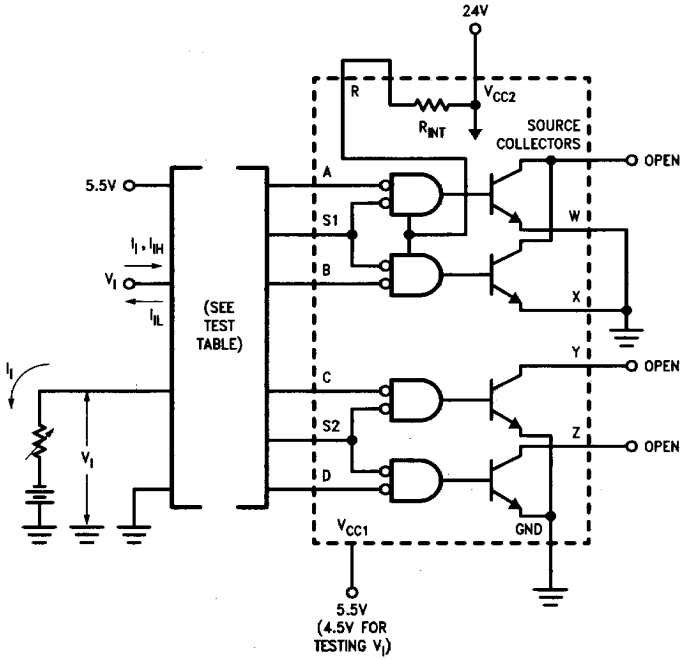
Note 1: *Figure 3* and *4* parameters must be measured using pulse techniques, t_W = 200 μs, duty cycle ≤2%.

Test Table

C	D	S2	Y	Z
0.8V	4.5V	0.8V	R_L	OPEN
4.5V	0.8V	0.8V	OPEN	R_L

FIGURE 4. V_{IL} and Sink V_{SAT}

DC Test Circuits (Continued)



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Test Tables

I_I, I_{IH}

Apply V_I = 5.5V Measure I_I Apply V_I = 2.4V Measure I_{IH}	Ground	Apply 5.5V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

Apply V_I = 0.4V Measure I_{IL} Apply I_I = −10 mA Measure V_I	Apply 5.5V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5. V_I, I_I, I_{IH} and I_{IL}

DC Test Circuits (Continued)

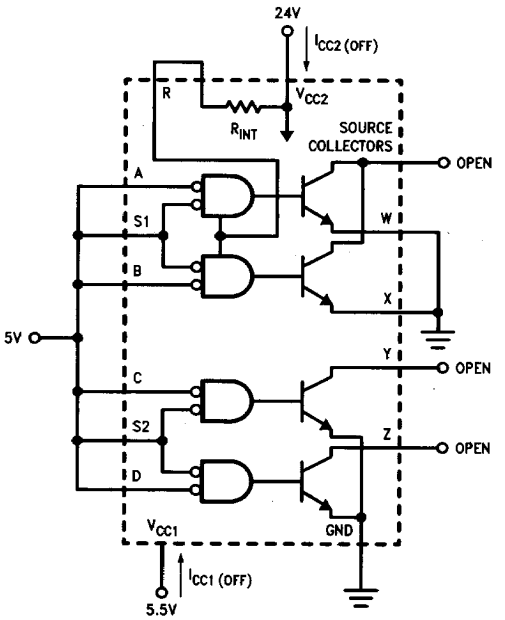

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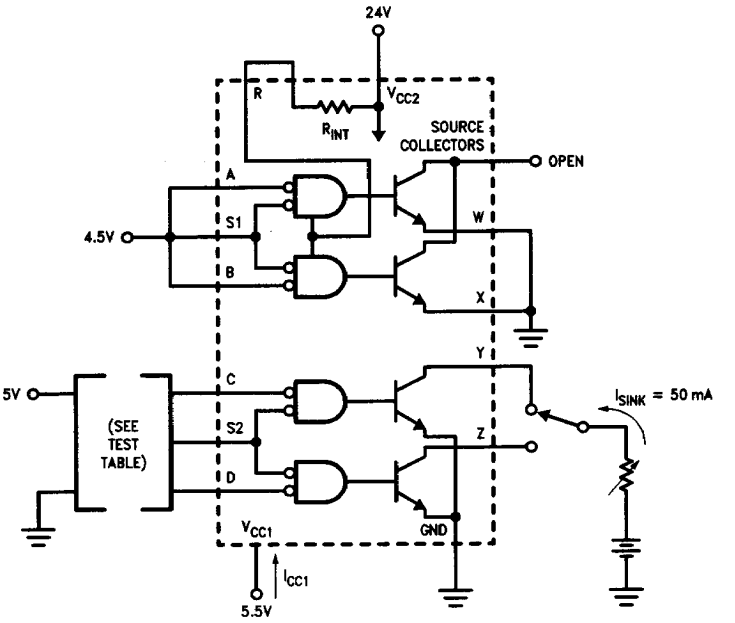
FIGURE 6. $I_{CC1\ (OFF)}$ and $I_{CC2\ (OFF)}$

DC Test Circuits (Continued)



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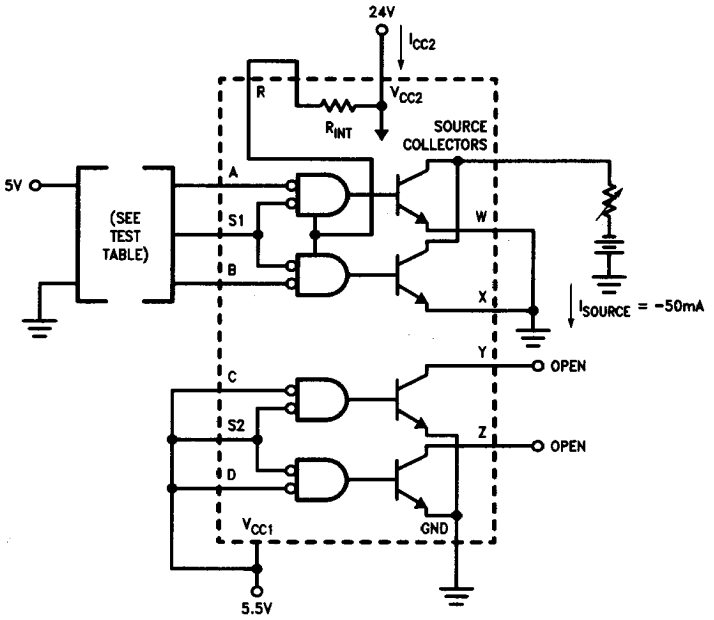
Test Table

C	D	S2	Y	Z
GND	5V	GND	I_{SINK}	OPEN
5V	GND	GND	OPEN	I_{SINK}

FIGURE 7. I_{CC1}, Either Sink On

DC Test Circuits (Continued)



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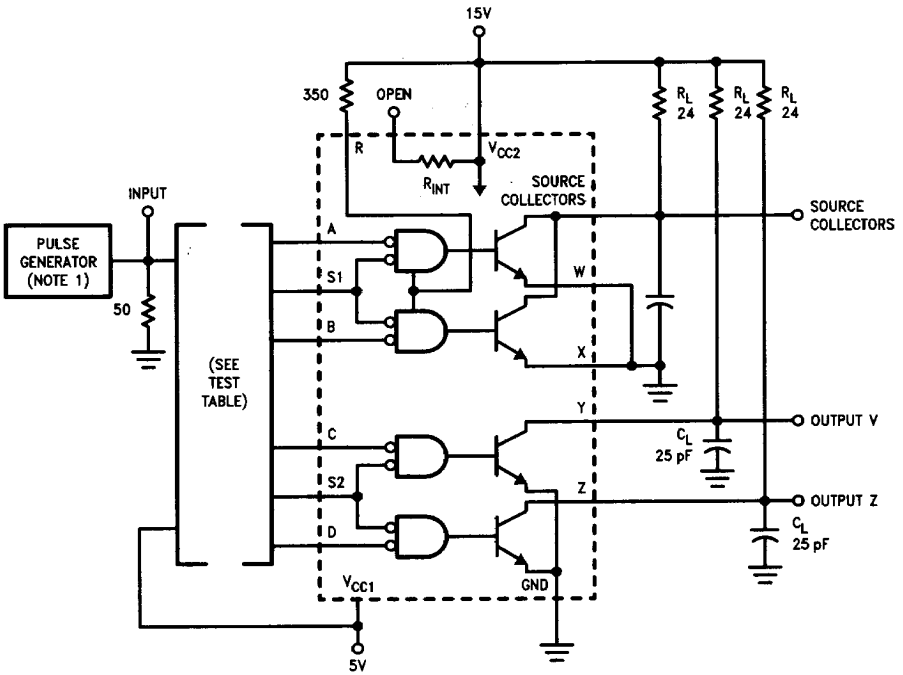
Test Table

A	B	S1
GND	5V	GND
5V	GND	GND

FIGURE 8. I_{CC2}, Either Source On

DC Test Circuits (Continued)



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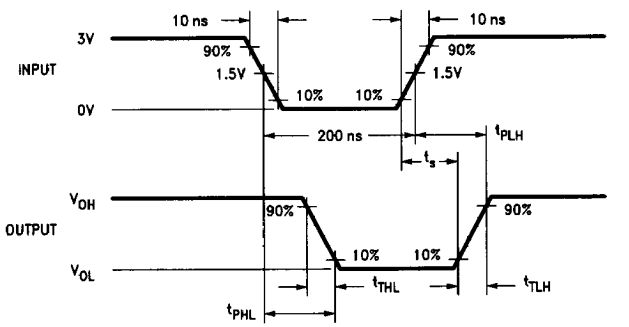
Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, duty cycle ≤ 1%.

Note 2: C_L includes probe and jig capacitance.

Voltage Waveforms



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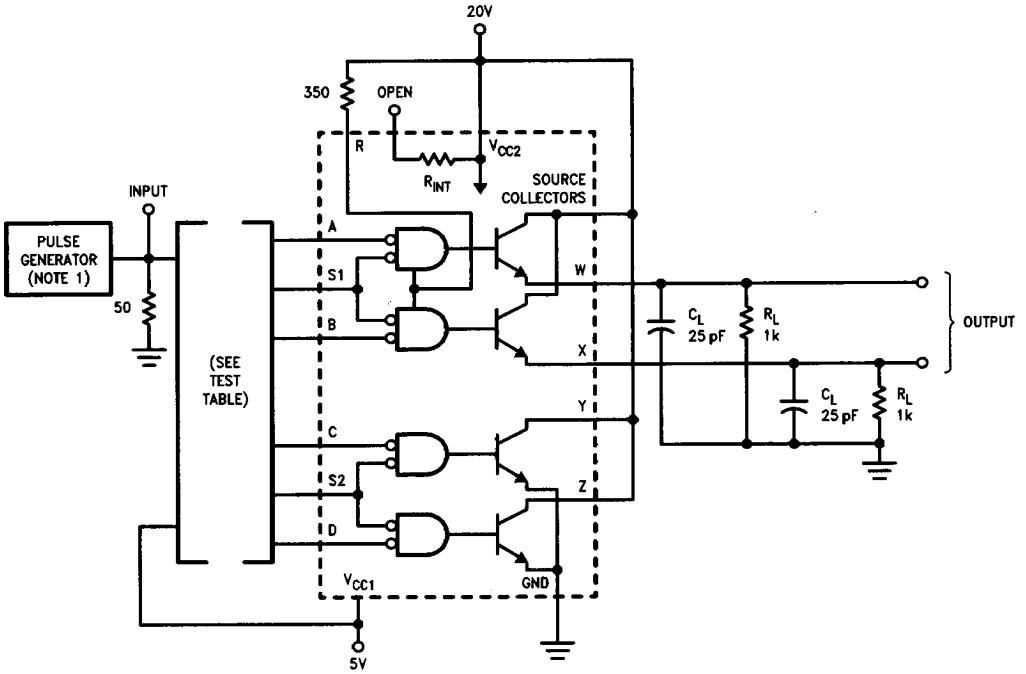
Test Table

Parameter	Output Under Test	Input	Connect to 5V
t_{PLH} and t_{PHL}	Source Collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} and t_S	Sink Output Y	C and S2	A, B, D and S1
	Sink Output Z	D and S2	A, B, C and S1

FIGURE 9. Switching Times

DC Test Circuits (Continued)



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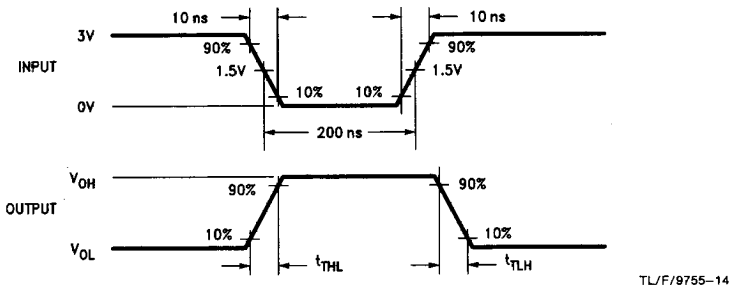
Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, duty cycle ≤ 1%.

Note 2: C_L includes probe and jig capacitance.

Voltage Waveforms



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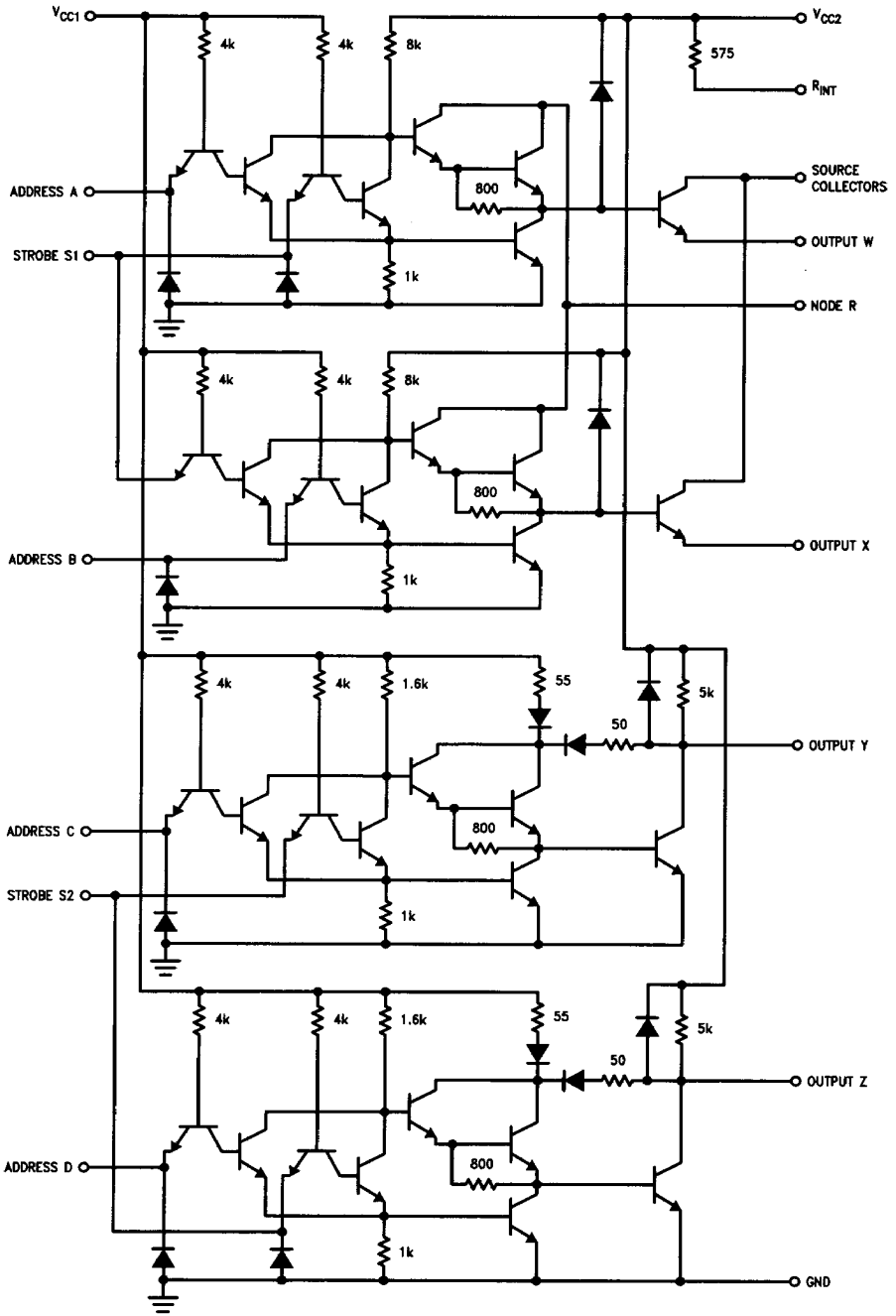
Test Table

Parameter	Output Under Test	Input	Connect to 5V
t_{TLH} and t_{THL}	Source Output W	A and S1	B, C, D and S2
	Source Output X	B and S1	A, C, D and S2

FIGURE 10. Transition Times of Source Outputs

Schematic Diagram



Applications

EXTERNAL RESISTOR CALCULATION

A typical magnetic-memory word drive requirement is shown in *Figure 11*. A source-output transistor of one DS75325 delivers load current (I_L). The sink-output transistor of another DS75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(Min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(Min)} - V_S - 2.9]} \quad (1)$$

where: R_{ext} is in kΩ,

$V_{CC2(Min)}$ is the lowest expected value of V_{CC2} in volts, V_S is the source output voltage in volts with respect to ground, I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2.

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(Min)} - V_S - 2] \quad (2)$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3.

$$I_{CS} \approx 0.94\,I_L \quad (3)$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(Min)} = 20V$ and $V_L = 3V$ while I_L of 500 mA flows. Using Equation 1:

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5\ k\Omega$$

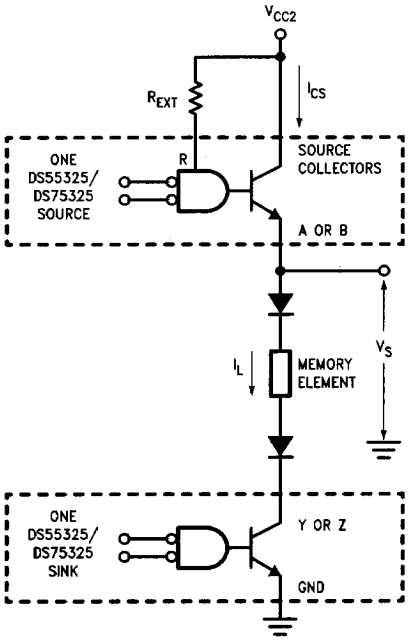
and from Equation 2:

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\,(500) \approx 470\ mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.



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Note 1: For clarity, partial logic diagrams of two DS55325s are shown.

Note 2: Source and sink shown are in different packages.

FIGURE 11. Typical Application Data

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