Ordering number : ENN4212A

CMOS IC

LC86P6032

8-Bit Single Chip Microcontroller with One-Time PROM

Overview

The LC86P6032 microcontroller, a new addition to the LC866000 series, is a 8-bit single chip CMOS microcontroller with one-time PROM. This microcontroller has the same function and pin assignment as for the LC866000 series mask ROM version, and a 32K-byte PROM.

Features

(1) Option switching using PROM data

The optional functions of the LC866000 series can be specified using PROM data.
The functions of the trial products can be evaluated using a mass production board.

(2) Internal one-time PROM capacity : 32768 bytes

(3) Internal RAM capacity : 512 bytes

Mask ROM version	PROM capacity	RAM capacity
LC866032	32512 bytes	512 bytes
LC866028	28672 bytes	512 bytes
LC866024	24576 bytes	512 bytes
LC866020	20480 bytes	384 bytes
LC866016	16384 bytes	384 bytes
LC866012	12288 bytes	384 bytes
LC866008	8192 bytes	384 bytes

(4) Operating supply voltage : 4.5V to 6.0V

(5) Instruction cycle time : 0.98µs to 400µs

(6) Operating temperature range : -30°C to +70°C

(7) Pin and package compatible with the mask ROM version

(8) Applicable mask ROM version : LC866032/LC866028/LC866024/LC866020/LC866016/LC866012 /LC866008

(9) Factory shipment : DIP64S
: QFP64E

Programming service

We offer various services at nominal charges. These include ROM writing, ROM reading, and package stamping and screening. Contact our local representatives for further information.

SANYO Electric Co.,Ltd. Semiconductor Company
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Notice for use

When using, please take note of the following.

(1) Differences between the LC86P6032 and the LC866000 series

Item	LC86P6032	LC866032/28/24/20/16/12/08
Port status at reset	Please refer to “Port status at reset” on the next page.	
Operation after releasing reset	The option is specified by degrees within 3ms after applying a ‘H’ level to the reset pin. The program located at 00H is executed.	The program located at 00H is executed immediately after applying a ‘H’ level to the reset pin.
Output form of segment •S0/T0 to S6/T6 •S7/T7 to S15/T15 •S16 to S23 •S24 to S29	Pulldown resistor Not provided Provided(fixed) Provided(fixed) Not provided	Pulldown resistor : Provided/Not provided Specified by the option Provided(fixed) Specified by the option Specified by the option
Operating supply voltage range (VDD)	4.5V to 6.0V	2.5V to 6.0V
Power dissipation	Refer to “electrical characteristics” on the semiconductor news.	

LC86P6032 uses 256 bytes that is addressed on 7F00H to 7FFFH in the program memory as the option configuration data area. This option configuration cannot execute all options which LC866000 series have. Next tables show the options that correspond and not correspond to LC86P6032.

• LC86P6032 Options

Option	Pins, Circuits	Option Settings
Configuration of input/output ports	Port 0 (Can be specified for each bit.)	1. Input : No pull-up MOS transistor Output : N-channel open drain 2. Input : Pull-up MOS transistor Output : CMOS
	Port 1 (Can be specified for each bit.)	1. Input : Programmable pull-up MOS transistor Output : N-channel open drain 2. Input : Programmable Pull-up MOS transistor Output : CMOS
Port 7 pull-up MOS transistor	Port 7 (Can be specified for each bit.)	1. Pull-up MOS transistor not provided. 2. Pull-up MOS transistor provided.

• A kind of option not corresponding LC86P6032

Option	Pins, Circuits	LC86P6032	LC866032/28/24/20/16/12/08
Pull-down resistor of high voltage withstand output terminal	·S0/T0 to S6/T6 ·S16 to S23 ·S24 to S29 (specified in a bit)	Not provided Provided(fixed) Not provided	Specified by the option Specified by the option Specified by the option

The port operation related to the option is different at reset. Please refer to the next table.

• Port configuration at reset

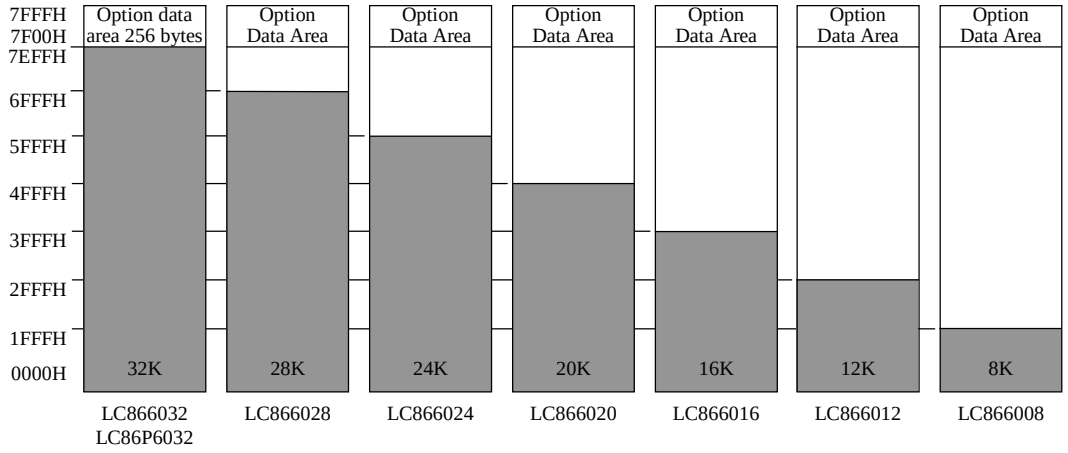
Pin	Option settings	LC86P6032	LC866032/28/24/20/16/12/08
P0	Input : No pull-up MOS transistor Output : N-channel open drain	(Same as for the mask version)	Input mode without pull-up MOS transistor (Output is OFF)
	Input : Pull-up MOS transistor Output : CMOS	Input mode •The Pull-up MOS transistor is not present during reset or several hundred microseconds after releasing reset. After that, the pull-up MOS transistor is present. (Output is OFF)	Input mode with pull-up MOS transistor (Output is OFF)
P1	Input : Programmable pull-up MOS transistor Output : N-channel open drain	(Same as for the mask version)	Input mode without pull-up MOS transistor (Output is OFF)
	Input : Programmable pull-up MOS transistor Output : CMOS	(Same as for the mask version)	Input mode without pull-up MOS transistor (Output is OFF)
P7	Pull-up MOS transistor not provided	(Same as for the mask version)	Input mode without pull-up MOS transistor
	Pull-up MOS transistor provided	Input mode •The Pull-up MOS transistor is not present during reset or several hundred microseconds after releasing reset. After that, the pull-up MOS transistor is present.	Input mode with pull-up MOS transistor

(2) Option

The option data is created by the option specified program “SU866000.EXE”. The created option data is linked to the program area by the linkage loader “L866000.EXE”.

(3) ROM space

LC86P6032 and LC866000 series use 256 bytes that is addressed on 07F00H to 07FFFH in the program memory as the option specified data area. These program memory capacity are 32512 bytes that is addressed on 0000H to 7EFFH.



(4) Ordering information

1.When ordering identical mask ROM and PROM devices simultaneously.

Provide an EPROM containing the target memory contents together with separate order forms for each of the mask ROM and PROM versions.

2. When ordering a PROM device.

Provide an EPROM containing the target memory contents together with an order form.

How to use

(1) Specification of option

LC86P6032 is programmed after specifying option data. The option is specified by the SU866000.EXE. The specified option file and the file created by our macro assembler (M866000.EXE) are linked by our linker (L866000.EXE) which creates HEX file, then the option code is put in the option specified area (07F00H to 07FFFH) of its HEX file.

(2) How to program for the EPROM

The LC86P6032 can be programmed by an EPROM programmer with attachments W86EP6032D and W86EP6032Q.

- Recommended EPROM programmer

Supplier	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electronics	MODEL 1890A

- "27512 (Vpp=12.5V) Intel high-speed programming" mode available. The address must be set to "0000H to 07FFFH" and the jumper (DASEC) must be set 'OFF' at programming.

(3) How to use the data security function

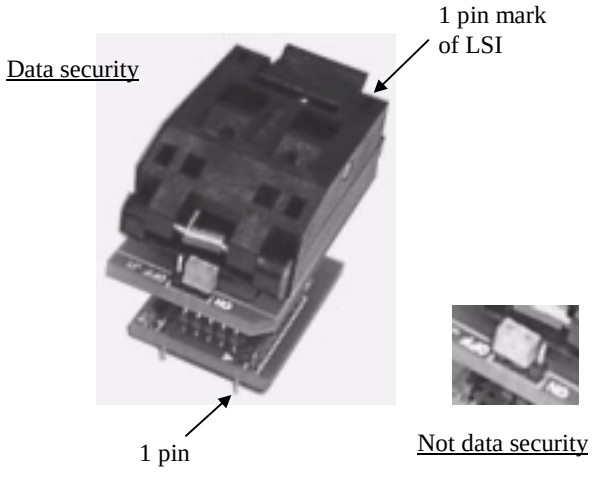
"Data security" is a function to prevent EPROM data from being read.

Instructions on using the data security function :

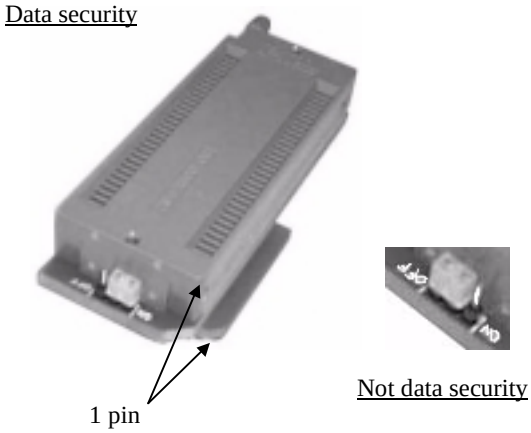
1. Set the jumper of attachment "ON".
2. Attempt to program the EPROM. The EPROM programmer will display an error. The error indication is a result of normal activity of the data security feature. This is not a problem with the EPROM programmer chip.

(Notes)

• The data security function is not carried out when the data of all addresses contain "FF" at step 2 above.
• Data security cannot be executed when the sequential operation "BLANK=>PROGRAM=>VERIFY" is used at step 2 above.
• Set the jumper "OFF" after execution of data security.

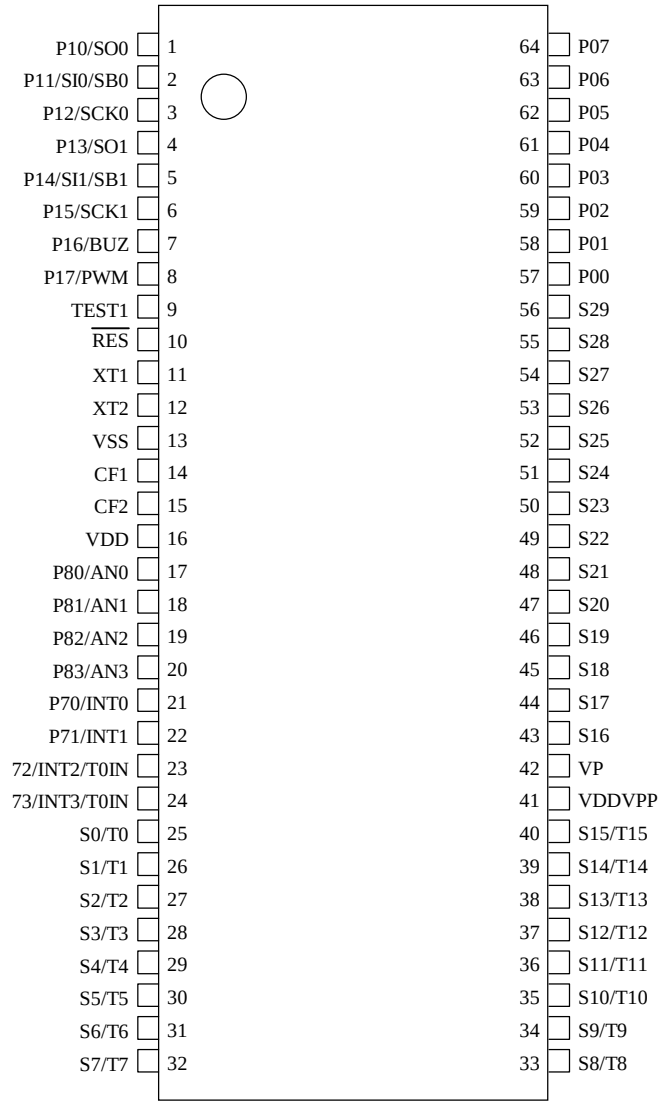


W86EP6032Q



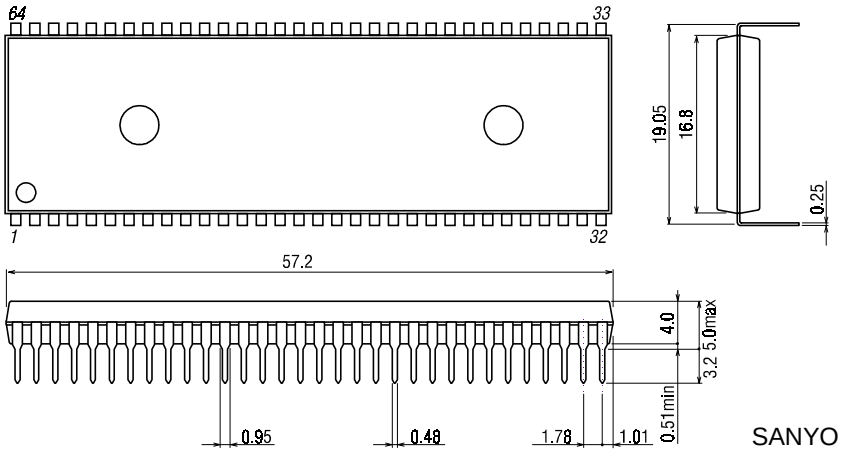
W86EP6032D

Pin Assignment



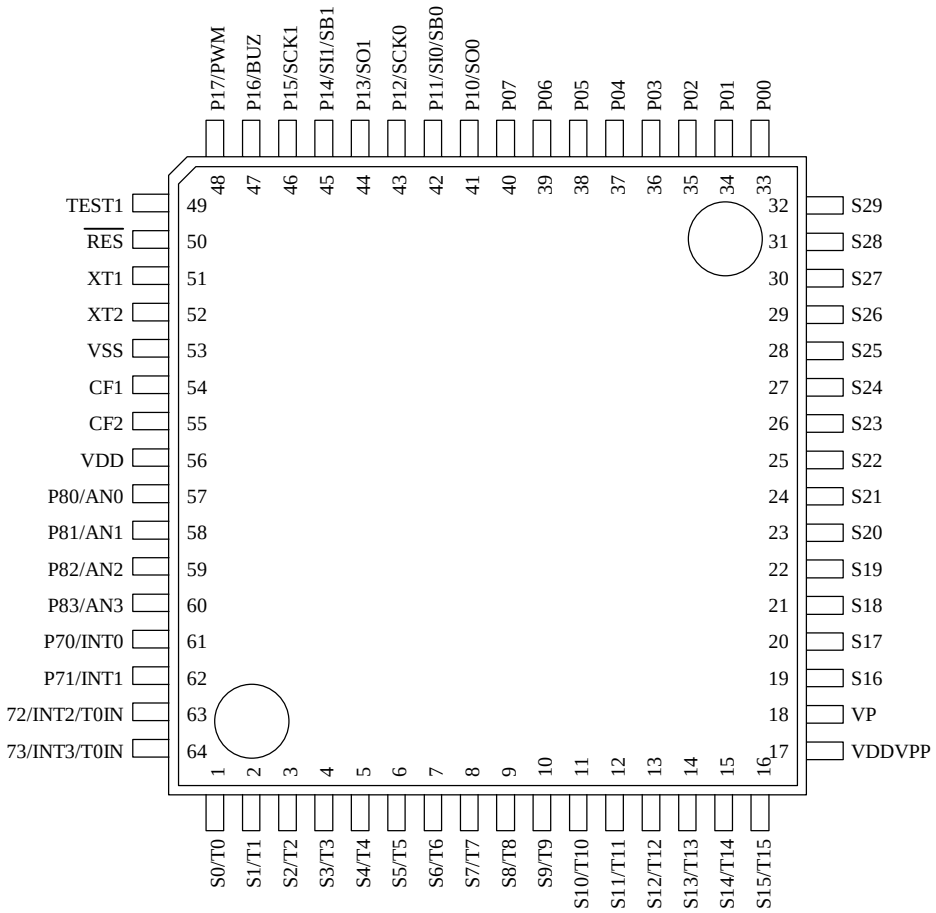
Package Dimension

(unit : mm)
3071



SANYO : DIP-64S(750mil)

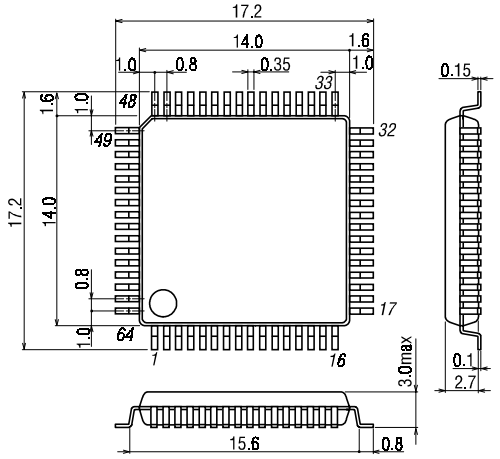
Pin Assignment



Package Dimension

(unit : mm)

3159

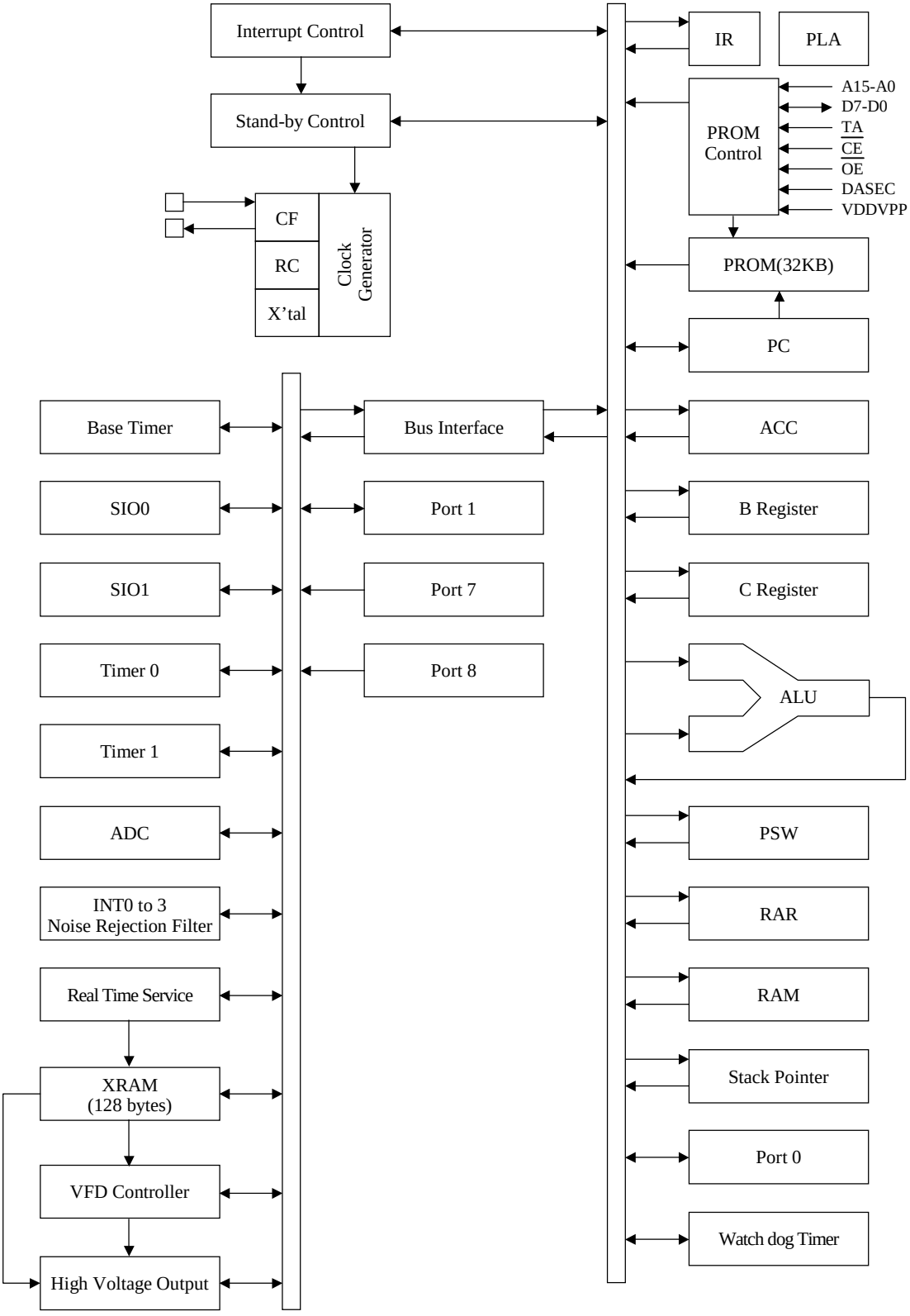


SANYO : QIP-64E

Notes

- The QFP packages should be heat-soaked for 24 hours at 125°C immediately prior to mounting (This baking is called pre-baking).
- After pre-baking, a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less. Please solder within 8 hours.

System Block Diagram



Pin Description

Pin Description Table

Pin name	I/O	Function Description	Option	Function in PROM mode
VSS	-	Power supply pin (-)		
VDD	-	Power supply pin (+)		
VP	-	Power supply pin (-) for the VFD output pull-down resist		
VDDVPP	-	Power supply pin (+) *6		Power for programming
PORT0 P00 to P07	I/O	•8-bit Input / output port •Input for port 0 interrupt •Input/output in nibble units •Input for HOLD release	•Pull-up resistor : Present/Not present •Output form : CMOS/N-channel open drain	
PORT1 P10 to P17	I/O	•8-bit input/output port •Data direction can be specified for each bit. •Other pin functions P10 : SIO0 data output P11 : SIO0 data input/bus input/output P12 : SIO0 clock input/output P13 : SIO1 : data output P14 : SIO1 : data input/bus input/output P15 : SIO1 clock input/output P16 : Buzzer output P17 : Timer 1 output (PWM output)	Output form : CMOS/N-channel open drain	Data input/output D0 to D7
PORT7 P70 P71 to P73	 I/O I	•4-bit input port •Other pin functions P70 : INT0 input/HOLD release/N-channel Tr. output for watchdog timer P71 : INT1 input/HOLD release P72 : INT2 input/timer 0 event input P73 : INT3 input with noise filter/timer 0 event input •Interrupt received format, vector address	•Pull-up resistor : Present/Not present	 Input of PROM control signal •DASEC (*1) • $\overline{OE}$ (*2) • $\overline{CE}$ (*3)

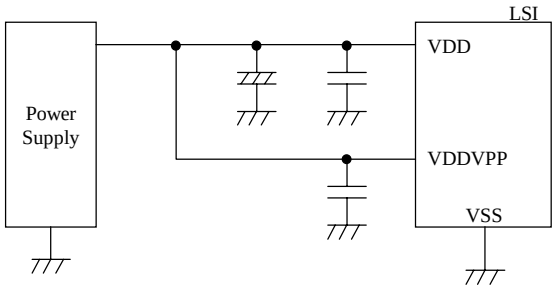
	Rising	Falling	Rising /falling	H level	L level	Vector
INT0	Enable	Enable	Disable	Enable	Enable	03H
INT1	Enable	Enable	Disable	Enable	Enable	0BH
INT2	Enable	Enable	Enable	Disable	Disable	13H
INT3	Enable	Enable	Enable	Disable	Disable	1BH

PORT8 P80 to P83	I	•4-bit input port •Other pin functions AD input port (4 port pins)		
S0/T0 to S6/T6 *7	O	Output for VFD display controller segment/timing in common		
S7/T7 to S15/T15 *8	O	•Output for VFD display controller segment/timing in common •Internal pull-down resistor output		•S14/T14 : TA (*4) •S15/T15 : A14 (*5)
S16 to S23 *9	O	•Output for VFD display controller segment •Internal pull-down resistor output		Address input A13 to A0
S24 to S29 *10	O	•Output for VFD display controller segment		
$\overline{RES}$	I	Reset pin		

Pin name	I/O	Function Description	Option	Function in PROM mode
TEST1	O	Test pin Should be left open		
XT1	I	Input pin for 32.768kHz crystal oscillation When not used, connect to VDD		
XT2	O	Output pin for 32.768kHz crystal oscillation When not used, should be left open		
CF1	I	Input pin for ceramic resonator oscillation		
CF2	O	Output pin for ceramic resonator oscillation		

• All port options can be specified in bit units.

*1 Memory select input for data security
*2 Output enable input
*3 Chip enable input
*4 TA → PROM control signal input
*5 A14 → Address input
*6 Connect as shown in the following figure to reduce noise into VDD pin.
• Short-circuit the VDD pin to the VDDVPP pin.



*7 S0/T0 to S6/T6 : not provided the pull-down resistor
*8 S7/T7 to S15/T15 : provided the pull-down resistor (fixed)
*9 S16 to S23 : provided the pull-down resistor (fixed)
*10 S24 to S29 : not provided the pull-down resistor

1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings min.	typ.	max.	unit
Supply voltage		VDDMAX	VDD,VDDVPP			-0.3		+7.0	V
Input voltage		VI(1)	•Ports 71,72,3,8 • $\overline{RES}$			-0.3		VDD+0.3	
		VI(2)	VP			VDD-4.5		VDD+0.3	
Output voltage		VO	•S0/T0 to S15/T15 •S16 to S29			VDD-4.5		VDD+0.3	
Input/Output voltage		VIO	•Ports 0, 1 •Port 70			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1	•CMOS output •At each pin		-4			mA
		IOPH(2)	S0/T0 to S15/T15	•At each pin		-30			
		IOPH(3)	S16 to S29	•At each pin		-15			
	Total output current	∑IOAH(1)	Port 0	Total of all pins		-10			
		∑IOAH(2)	Port 1	Total of all pins		-10			
		∑IOAH(3)	•S0/T0 to S15/T15 •S16 to S29	Total of all pins		-130			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1	At each pin				20	
		IOPL(2)	Port 70	At each pin				15	
	Total output current	∑IOAL(1)	Port 0	Total of all pins				40	
		∑IOAL(2)	Ports 1, 70	Total of all pins				40	
Power dissipation (max.)		Pdmax(1)	DIP64S	Ta=-30 to+70°C				760	mW
		Pdmax(2)	QFP64E	Ta=-30 to+70°C				430	
Operating temperature range		Topr				-30		+70	°C
Storage temperature range		Tstg				-65		+150	

Notes

- The QFP packages should be heat-soaked for 24 hours at 125°C immediately prior to mounting (This baking is called pre-baking).
- After pre-baking, a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less. Please solder within 8 hours.

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Operating supply voltage range	VDD	VDD	0.98μs ≤ tCYC ≤ 400μs		4.5		6.0	V
Hold voltage	VHD	VDD	RAM and registers retain their pre-HOLD mode values		2.0		6.0	
Pull-down voltage	VP	VP		4.5 to 6.0	-35		VDD	
Input high voltage	VIH(1)	Port 0 (Schmitt)	Output disable	4.5 to 6.0	0.4VDD +0.9		VDD	
	VIH(2)	•Port 1 •Ports 72,73 (Schmitt)	Output disable	4.5 to 6.0	0.75VDD		VDD	
	VIH(3)	•Port 70 port input/interrupt •Port 71 • $\overline{\text{RES}}$ (Schmitt)	Output N-channel Tr. OFF	4.5 to 6.0	0.75VDD		VDD	
	VIH(4)	Port 70 Watchdog timer	Output N-channel Tr. OFF	4.5 to 6.0	0.9VDD		VDD	
	VIH(5)	Port 8		4.5 to 6.0	0.75VDD		VDD	
Input low voltage	VIL(1)	Port 0 (Schmitt)	Output disable	4.5 to 6.0	VSS		0.2VDD	
	VIL(2)	•Port 1 •Ports 72,73 (Schmitt)	Output disable	4.5 to 6.0	VSS		0.25VDD	
	VIL(3)	•Port 70 port input/interrupt •Port 71 • $\overline{\text{RES}}$ (Schmitt)	N-channel Tr. OFF	4.5 to 6.0	VSS		0.25VDD	
	VIL(4)	Port 70 Watchdog timer	N-channel Tr. OFF	4.5 to 6.0	VSS		0.8VDD -1.0	
	VIL(5)	Port 8		4.5 to 6.0	VSS		0.25VDD	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	μs

continue

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Oscillation frequency range (Note 1)	FmCF(1)	CF1,CF2	•12MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0	11.76	12	12.24	MHz
	FmCF(2)	CF1,CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0	2.94	3	3.06	
	FmRC		RC oscillation	4.5 to 6.0	0.4	0.8	2.0	
	FsXtal	XT1,XT2	•32.768kHz (crystal resonator oscillation) •Refer to figure 2	4.5 to 6.0		32.768		kHz
Oscillation stable time period (Note 1)	tmsCF(1)	CF1,CF2	•12MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0		0.02	0.2	ms
	tmsCF(2)	CF1,CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0		0.1	1	
	tssXtal	XT1,XT2	•32.768kHz (crystal resonator oscillation) •Refer to figure 3	4.5 to 6.0		1	1.5	s

(Note 1) The oscillation constants are shown on Table 1 and Table 2.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	typ.	max.	unit
Input high current	IIH(1)	•Port 1 •Port 0 without pull-up MOS Tr.	•Output disabled •Pull-up MOS Tr. OFF •VIN=VDD (including off-state leak current of output Tr.)	4.5 to 6.0			1	μA
	IIH(2)	•Port 7 without pull-up MOS Tr. •Port 8	VIN=VDD	4.5 to 6.0			1	
	IIH(3)	$\overline{RES}$	VIN=VDD	4.5 to 6.0			1	
Input low current	IIL(1)	•Port 1 •Port 0 without pull-up MOS Tr.	•Output disabled •Pull-up MOS Tr. OFF •VIN=VSS (including off-state leak current of output Tr.)	4.5 to 6.0	-1			
	IIL(2)	•Port 7 without pull-up MOS Tr. •Port 8	VIN=VSS	4.5 to 6.0	-1			
	IIL(3)	$\overline{RES}$	VIN=VSS	4.5 to 6.0	-1			
Output high voltage	VOH(1)	Ports 0, 1 at CMOS output	IOH=-1.0mA	4.5 to 6.0	VDD-1			V
	VOH(2)		IOH=-0.1mA	4.5 to 6.0	VDD-0.5			
	VOH(3)	S0/T0 to S15/T15	IOH=-20mA	4.5 to 6.0	VDD-1.8			
	VOH(4)		•IOH=-1mA •The current IOH at each pin should be between 0 and -1mA.	4.5 to 6.0	VDD-1			
	VOH(5)	S16 to S29	IOH=-5mA	4.5 to 6.0	VDD-1.8			
	VOH(6)		•IOH=-1mA •The current IOH at each pin should be between 0 and -1mA.	4.5 to 6.0	VDD-1			
Output low voltage	VOL(1)	Ports 0, 1	IOL=10mA	4.5 to 6.0			1.5	
	VOL(2)		•IOL=1.6mA •When the total current of the ports 0, 1 is not over 40mA.	4.5 to 6.0			0.4	
	VOL(3)	Port 70	IOL=1mA	4.5 to 6.0			0.4	
Pull-up MOS Tr. resistance	Rpu	•Ports 0, 1 •Port 7	VOH=0.9VDD	4.5 to 6.0	15	40	70	KΩ

continue

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Output off-leakage current	IOFF(1)	S0/T0 to S6/T6, S24 to S29 without pull-down resistor	•Output P-ch Tr. OFF •VOUT=VSS	4.5 to 6.0	-1			μA
	IOFF(2)		•Output P-ch Tr. OFF •VOUT=VDD-40V	4.5 to 6.0	-30			
Pull-down resistor	Rpd	S7/T7 to S15/T15, S16 to S23 with pull-down resistor	•Output P-ch Tr. OFF •VOUT=3V •Vp=-30V	5.0	60	100	200	KΩ
Hysteresis voltage	VHIS	•Ports 0, 1 •Port 7 • $\overline{RES}$	Output disable	4.5 to 6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •Unmeasured input pins are set to VSS level •Ta=25°C	4.5 to 6.0		10		pF

4. Serial Input/Output Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5.	4.5 to 6.0	2			tCYC
		Low-level pulse width	tCKL(1)			4.5 to 6.0	1			
		High-level pulse width	tCKH(1)			4.5 to 6.0	1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	•Use pull-up resistor (1kΩ) when set to open-drain output. •Refer to figure 5.	4.5 to 6.0	2			
		Low-level pulse width	tCKL(2)			4.5 to 6.0		1/2 tCKCY		
		High-level pulse width	tCKH(2)			4.5 to 6.0		1/2 tCKCY		
Serial input	Data set up time		tICK	•SI0,SI1 •SB0,SB1	•Data set-up to SCK0,1 •Data hold from SCK0,1 •Refer to figure 5.	4.5 to 6.0	0.1			μs
	Data hold time		tCKI			4.5 to 6.0	0.1			
Serial output	Output delay time (Serial clock is external clock)		tCKO(1)	•SO0,SO1 •SB0,SB1	•Use pull-up resistor (1kΩ) when set to open-drain output. •Data hold from SCK0,1 •Refer to figure 5.	4.5 to 6.0			7/12 tCYC +0.2	
	Output delay time (Serial clock is internal clock)		tCKO(2)			4.5 to 6.0			1/3 tCYC +0.2	

5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0 pulse countable	4.5 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock selected to 1/1.)	•Interrupt acceptable •Timer0 pulse countable	4.5 to 6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock selected to 1/64.)	•Interrupt acceptable •Timer0 pulse countable	4.5 to 6.0	128			
	tPIL(4)	$\overline{\text{RES}}$	Reset acceptable	4.5 to 6.0	200			μs

6. AD Converter Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Resolution	N			4.5 to 6.0		8		bit
Absolute precision	ET		(Note 2)	4.5 to 6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time = 16 × tCYC (ADCR2=0) (Note 3)	4.5 to 6.0	15.68 (tCYC= 0.98μs)		65.28 (tCYC= 4.08μs)	μs
			AD conversion time = 32 × tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98μs)		130.56 (tCYC= 4.08μs)	
Analog input voltage range	VAIN	AN0 to AN3		4.5 to 6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 to 6.0			1	μA
	IAINL		VAIN=VSS	4.5 to 6.0	-1			

(Note 2) Quantizing error (±1/2 LSB) is ignored.

(Note 3) The conversion time is the period from execution of the instruction to start conversion to the completion of shifting the A/D converted value to the register.

7. Current Drain Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current drain during basic operation (Note 4)	IDDOP(1)	VDD	•FmCF=12MHz for Ceramic resonator oscillation •FsXtal=32.768kHz for crystal oscillator •System clock : CF oscillator •Internal RC oscillator stopped	4.5 to 6.0		13	26	mA
	IDDOP(2)		•FmCF=3MHz for Ceramic resonator oscillation •FsXtal=32.768kHz for crystal oscillator •System clock : CF oscillator •Internal RC oscillator stopped	4.5 to 6.0		6.5	14	
	IDDOP(3)		•FmCF=0Hz (when oscillator stops) •FsXtal=32.768kHz for crystal oscillator •System clock : RC oscillator	4.5 to 6.0		4	10	
	IDDOP(4)		•FmCF=0Hz (when oscillator stops) •FsXtal=32.768kHz for crystal oscillator •System clock : crystal oscillator •Internal RC oscillator stopped	4.5 to 6.0		3.5	9	

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current drain at HALT mode (Note 4)	IDDHALT(1)	VDD	•HALT mode •FmCF=12MHz for Ceramic resonator oscillation •FsXtal=32.768kHz for crystal oscillator •System clock : CF oscillator •Internal RC oscillator stopped	4.5 to 6.0		5	10	mA
	IDDHALT(2)		•HALT mode •FmCF=3MHz for Ceramic resonator oscillation •FsXtal=32.768kHz for crystal oscillator •System clock : CF oscillator •Internal RC oscillator stopped	4.5 to 6.0		1.8	4.6	
	IDDHALT(3)		•HALT mode •FmCF=0Hz (when oscillator stops) •FsXtal=32.768kHz crystal oscillator •System clock : RC oscillator	4.5 to 6.0		400	800	μA
	IDDHALT(4)		•HALT mode •FmCF=0Hz (when oscillator stops) •FsXtal=32.768kHz for crystal oscillator •System clock : crystal oscillator •Internal RC oscillator stopped	4.5 to 6.0		20	60	
Current drain at HOLD mode (Note 4)	IDDHOLD(1)	VDD	HOLD mode	4.5 to 6.0		0.05	30	
	IDDHOLD(2)			2.5 to 4.5		0.02	20	

(Note 4) The currents of output transistors and pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation circuit recommended constants (main-clock)

Oscillation type	Supplier	Oscillator	C1	C2
12MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33pF	33pF
		CSA12.0MT	33pF	33pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	33pF	33pF
3MHz ceramic resonator oscillation	Murata	CSA3.00MG	33pF	33pF
		CST3.00MGW	on chip	
	Kyocera	KBR-3.0MS	47pF	47pF

* For both C1 and C2, the K rank (±10%) and SL characteristics must be used.

Table 2. Crystal oscillation circuit recommended constants (sub-clock)

Oscillation type	Supplier	Oscillator	C3	C4
32.768kHz crystal oscillation	Daishinku	DT-38(1TA252E00)	18pF	18pF
	Kyocera	KF-38G-13P0200	18pF	18pF

(Notes) •Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
•If you use other oscillators herein, we provide no guarantee for the characteristics.

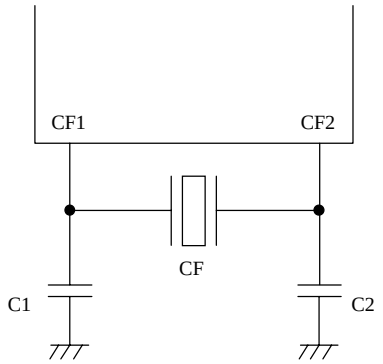


Figure 1 Ceramic resonator oscillation

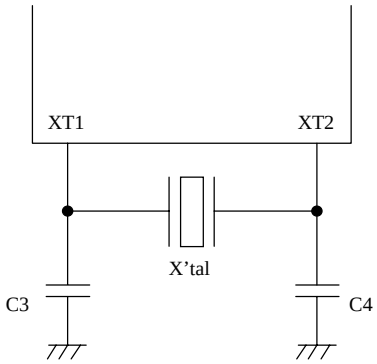


Figure 2 Crystal oscillation

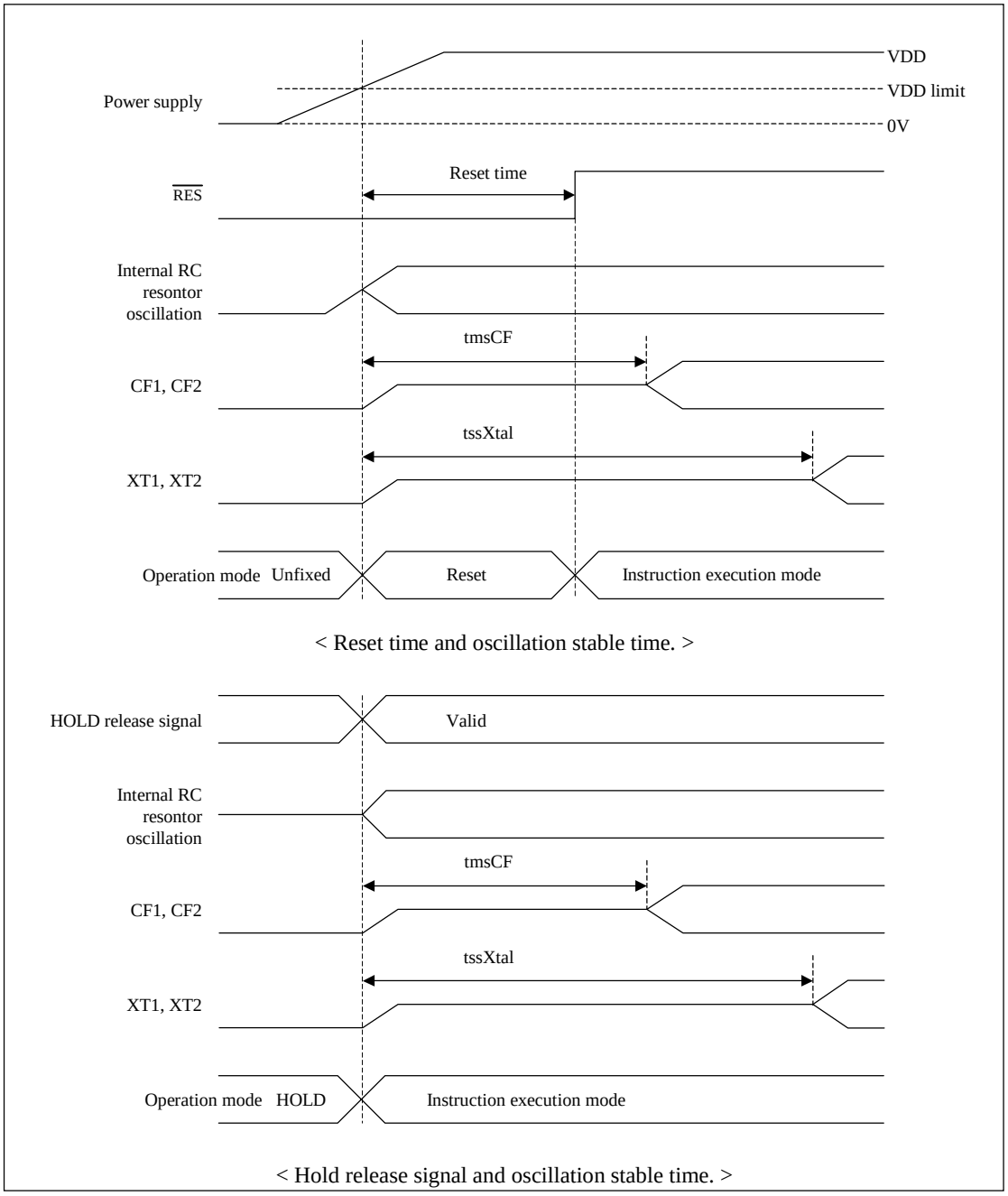
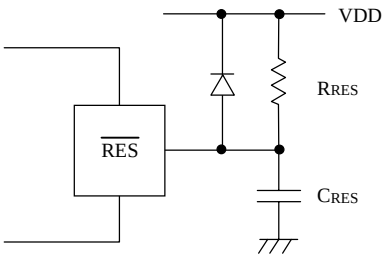
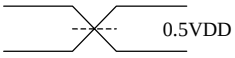


Figure 3 Oscillation stable time

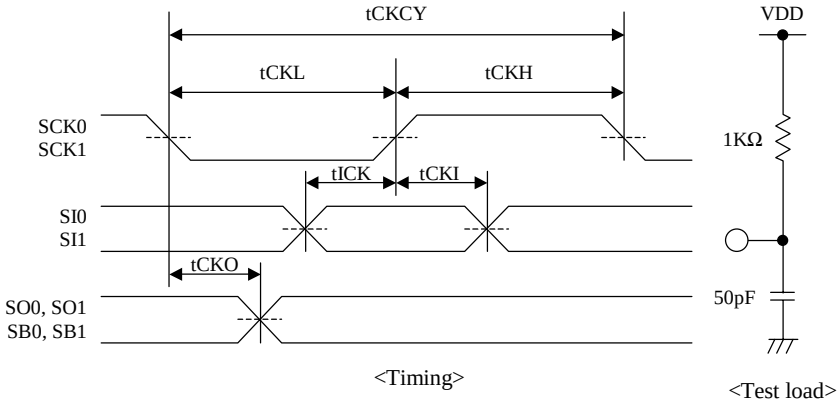


(Note) The values of CRES and RRES should be determined such that reset time is at least 200μs, measured from the moment the power exceeds the VDD lower limit.

Figure 4 Reset circuit



<AC timing point>



<Timing>

<Test load>

Figure 5 Serial input/output test conditions

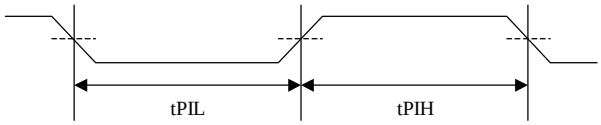


Figure 6 Pulse input timing conditions

Notice for use

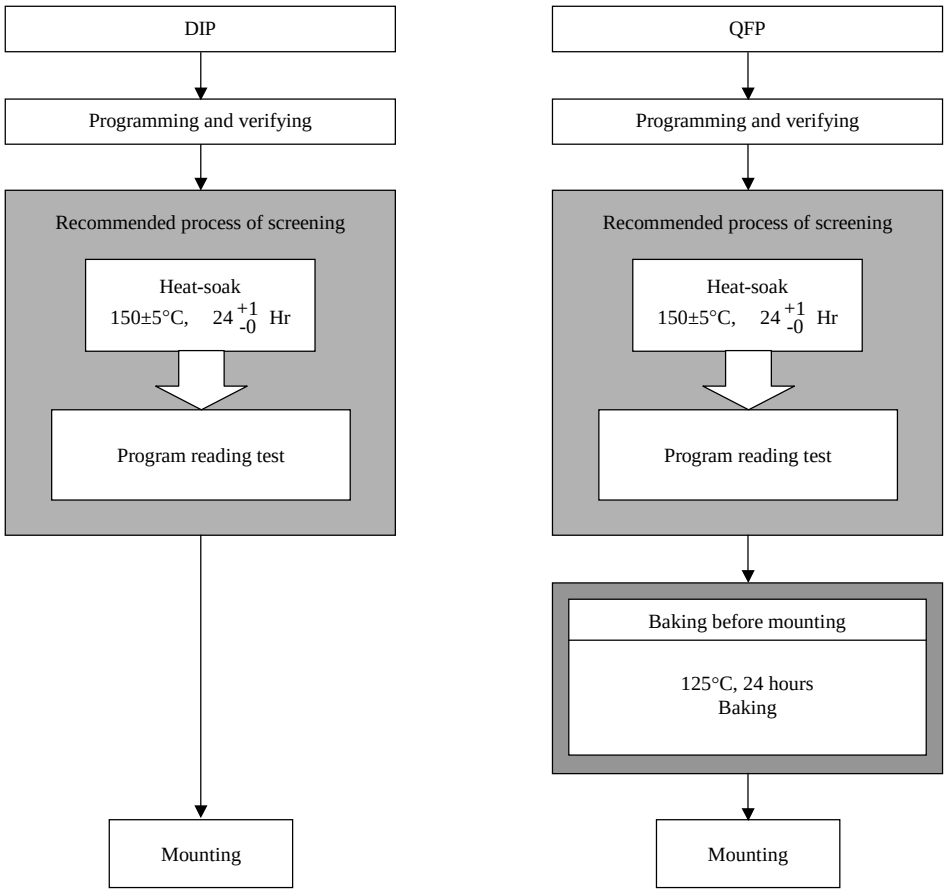
• The construction of the one-time programmable microcomputer with a blank built-in PROM makes it impossible for SANYO to completely factory-test it before shipping. To probe reliability of the programmed devices, the screening procedure shown in the following figure should always be followed.

• It is not possible to perform a writing test on the blank PROM.. 100% yield, therefore, cannot be guaranteed.

• Should be stored in dry conditions (QFP type only)
The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less.

• After opening the packing (QFP type only)
The preparation procedures shown in the following figure should always be followed prior to mounting the packages on the substrate. After opening the packing, a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less. Please solder within 8 hours.

a. Shipping with a blank PROM (Data to be programmed by customer)
This microcomputer is provided DIP/QFP packages, but the condition before mounting is not same.
Refer to the mounting precedure as follows;



b. Shipping with programmed PROM (Data programmed by Sanyo)