

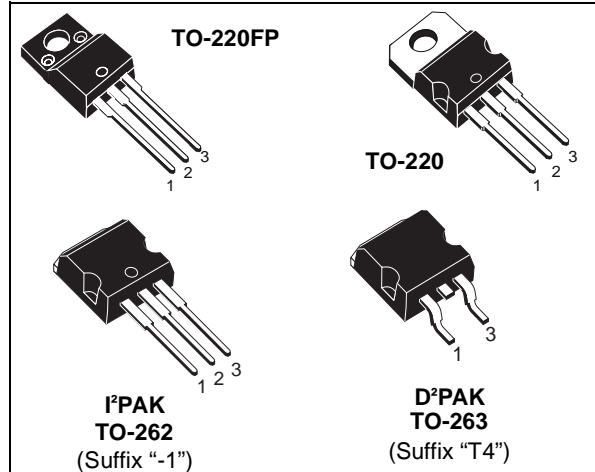


# STB55NF06 STB55NF06-1 STP55NF06 STP55NF06FP

N-CHANNEL 60V - 0.015  $\Omega$  - 50A TO-220/TO-220FP/I<sup>2</sup>PAK/D<sup>2</sup>PAK  
STripFET™ II POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP55NF06	60 V	<0.018 $\Omega$	50 A
STB55NF06-1	60 V	<0.018 $\Omega$	50 A
STB55NF06	60 V	<0.018 $\Omega$	50 A
STP55NF06FP	60 V	<0.018 $\Omega$	50 A(*)

- TYPICAL R<sub>DS(on)</sub> = 0.015  $\Omega$
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- SURFACE-MOUNTING D<sup>2</sup>PAK (TO-263) POWER PACKAGE IN TUBE (NO SUFFIX) OR IN TAPE & REEL (SUFFIX "T4")
- THROUGH-HOLE I<sup>2</sup>PAK (TO-262) POWER PACKAGE IN TUBE (SUFFIX "-1")



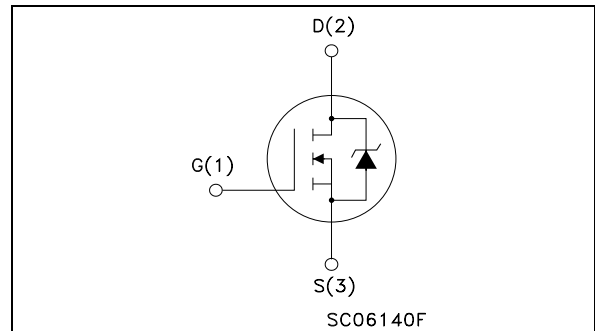
## DESCRIPTION

This Power MOSFET is the latest development of ST-Microelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

## APPLICATIONS

- HIGH CURRENT, HIGH SWITCHING SPEED
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS
- AUTOMOTIVE

## INTERNAL SCHEMATIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP_B55NF06(-1)	STP55NF06FP	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	60		V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	60		V
V <sub>GS</sub>	Gate- source Voltage	$\pm 20$		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	50	50(*)	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	35	35(*)	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	200	200(*)	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	110	30	W
	Derating Factor	0.73	0.2	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	7		V/ns
E <sub>AS</sub> (2)	Single Pulse Avalanche Energy	350		mJ
T <sub>stg</sub>	Storage Temperature	-55 to 175		°C
T <sub>j</sub>	Operating Junction Temperature			

(●) Pulse width limited by safe operating area  
(\*) Refer to soa for the max allowable current value on FP-type due to R<sub>th</sub> value

(1) I<sub>SD</sub>  $\leq$  50A, di/dt  $\leq$  400A/ $\mu$ s, V<sub>DD</sub>  $\leq$  V<sub>(BR)DSS</sub>, T<sub>j</sub>  $\leq$  T<sub>JMAX</sub>  
(2) Starting T<sub>j</sub> = 25 °C, I<sub>D</sub> = 25A, V<sub>DD</sub> = 30V

**STB50NF06 STB55NF06-1 STP55NF06 STP55NF06FP**

**THERMAL DATA**

			I <sup>2</sup> PAK D <sup>2</sup> PAK TO-220	TO-220FP	
R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max	1.36	5	°C/W
R <sub>thj-amb</sub> T <sub>I</sub>	Thermal Resistance Junction-ambient Maximum Lead Temperature For Soldering Purpose (1.6 mm from case, for 10 sec)	Max	62.5 300		°C/W °C

**ELECTRICAL CHARACTERISTICS** (T<sub>case</sub> = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>C</sub> = 125°C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			±100	nA

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 27.5 A		0.015	0.018	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> = 15 V I <sub>D</sub> = 27.5 A		18		S
C <sub>iSS</sub> C <sub>oSS</sub> C <sub>rSS</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		1530 300 105		pF pF pF

**ELECTRICAL CHARACTERISTICS** (continued)

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 30\text{ V}$ $I_D = 27.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		16 8		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 48\text{ V}$ $I_D = 55\text{ A}$ $V_{GS} = 10\text{ V}$		44.5 10.5 17.5	60	nC nC nC

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**SWITCHING OFF**

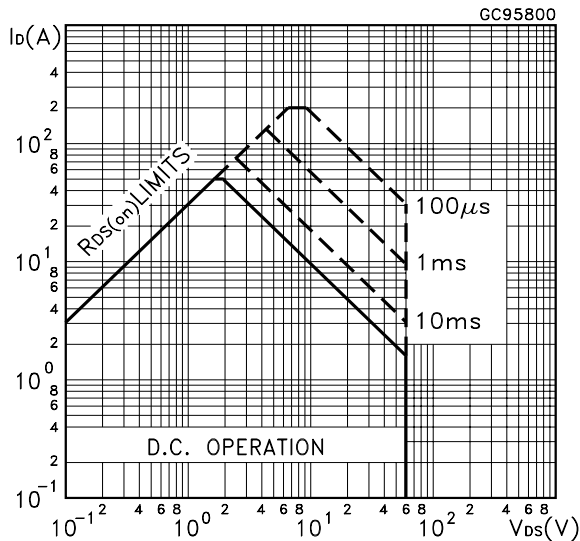
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 30\text{ V}$ $I_D = 27.5\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		36 15		ns ns

**SOURCE DRAIN DIODE**

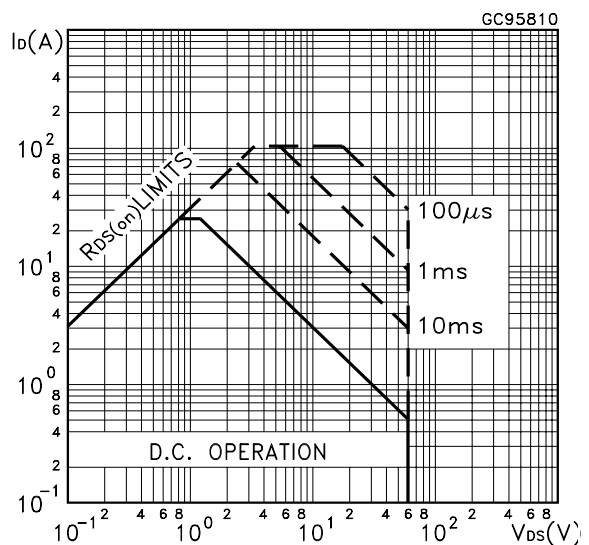
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				50 200	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 55\text{ A}$ $V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 55\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		75 170 4.5		ns nC A

(\*)Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.  
 (•)Pulse width limited by safe operating area.

Safe Operating Area for

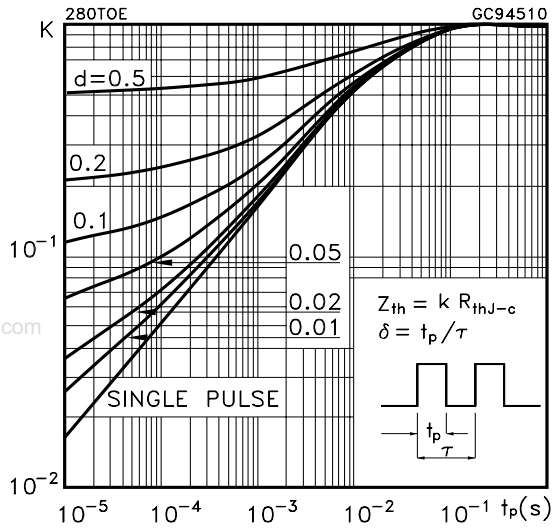


Safe Operating Area for TO-220FP

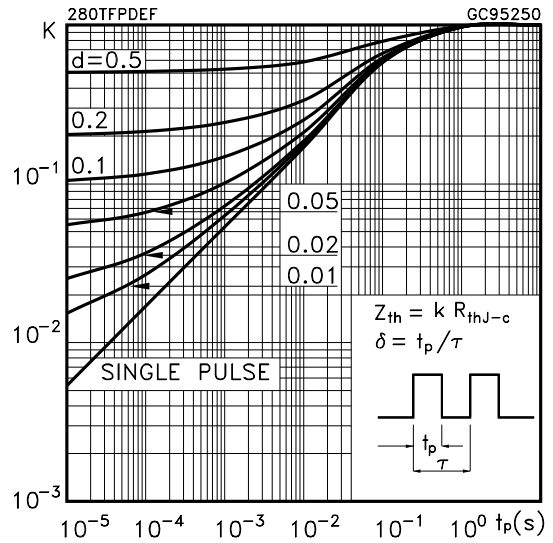


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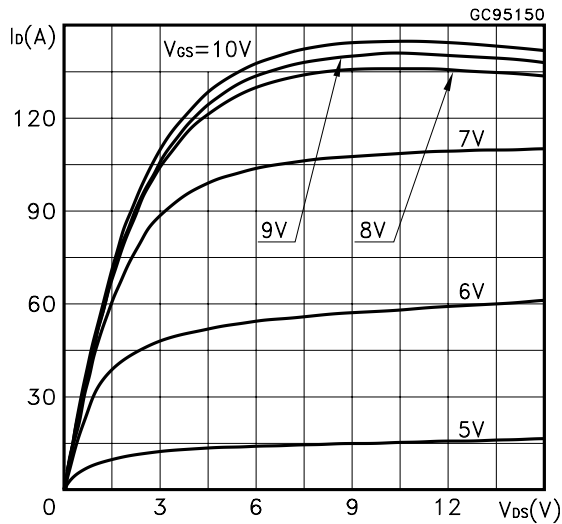
Thermal Impedance



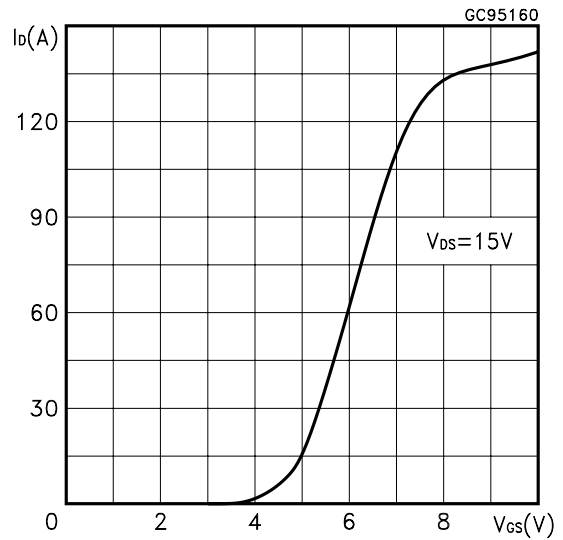
Thermal Impedance for TO-220FP



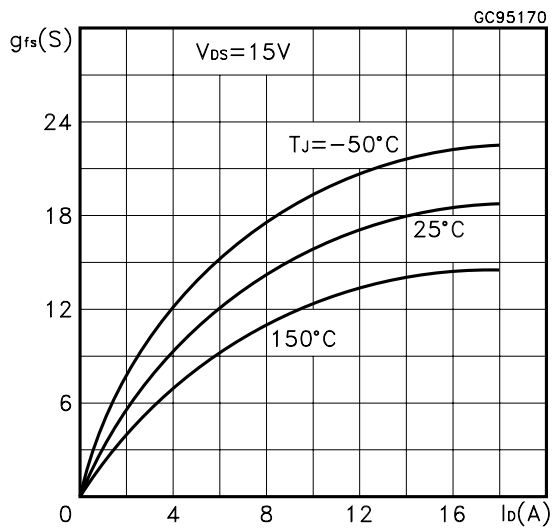
Output Characteristics



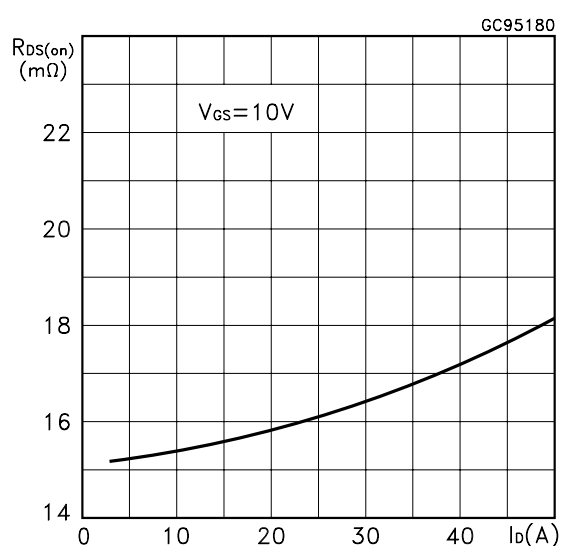
Transfer Characteristics



Transconductance

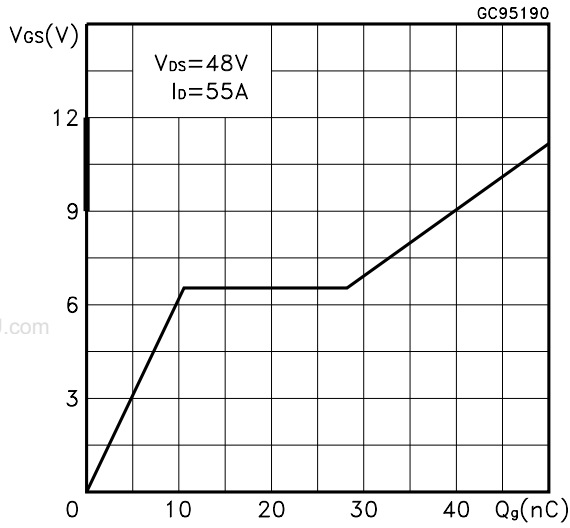


Static Drain-source On Resistance

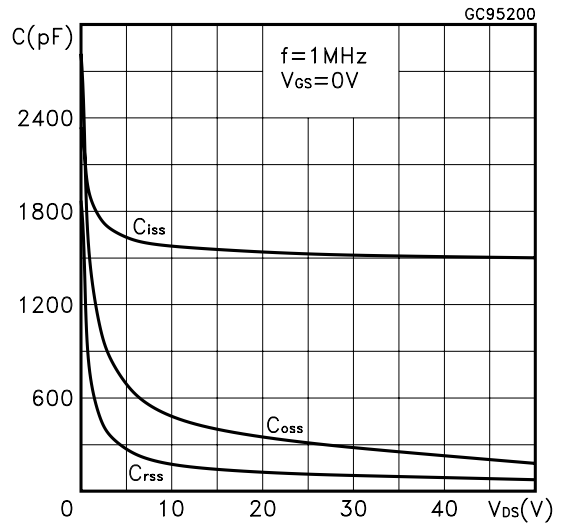


**STB50NF06 STB55NF06-1 STP55NF06 STP55NF06FP**

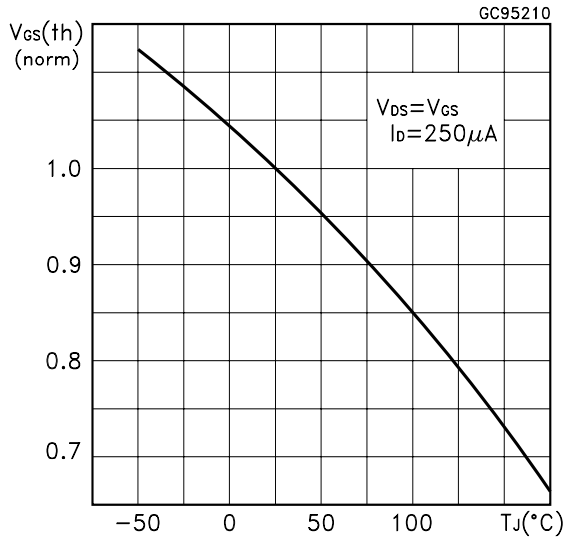
Gate Charge vs Gate-source Voltage



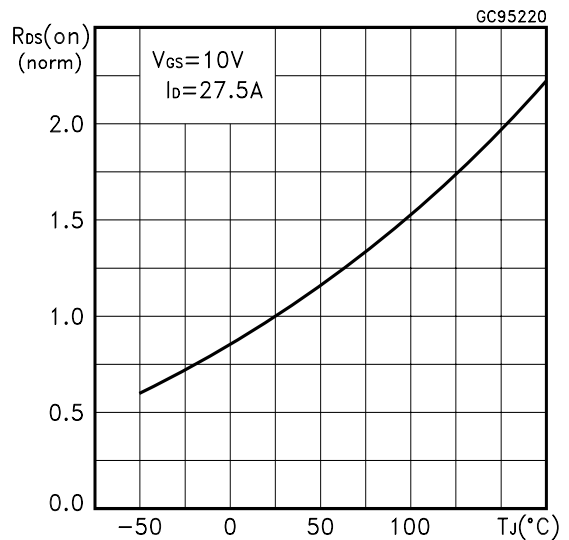
Capacitance Variations



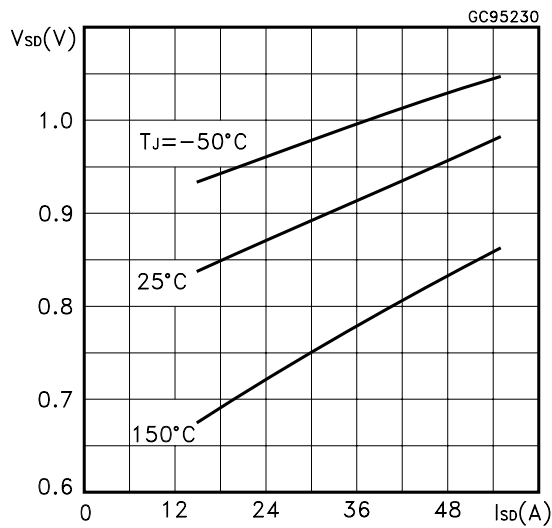
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage Temperature

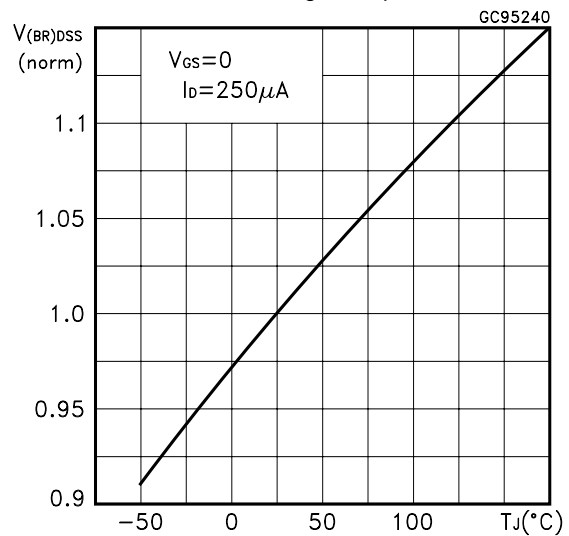


Fig. 1: Unclamped Inductive Load Test Circuit

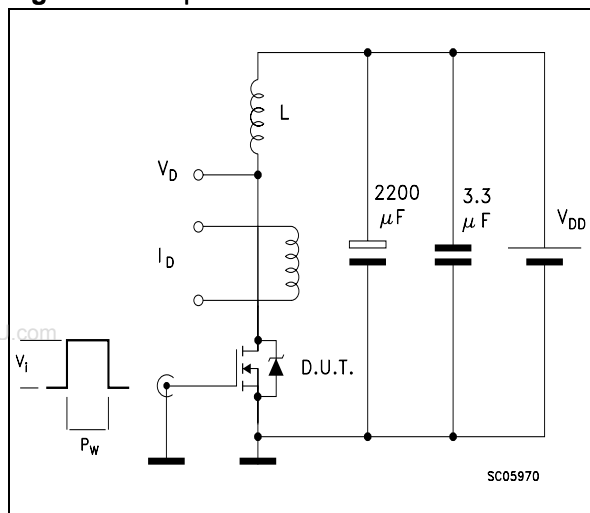


Fig. 2: Unclamped Inductive Waveform

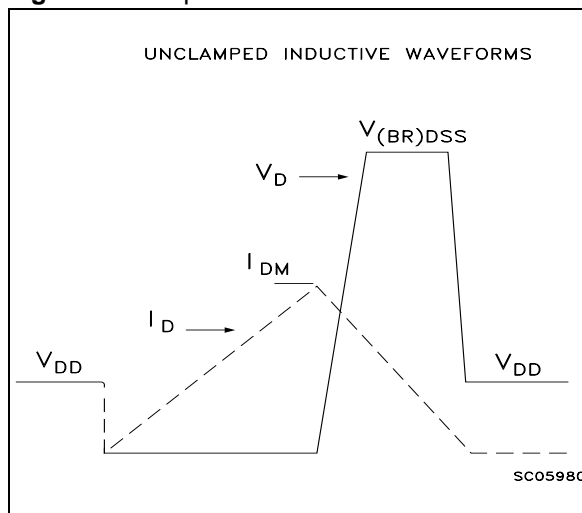


Fig. 3: Switching Times Test Circuits For Resistive Load

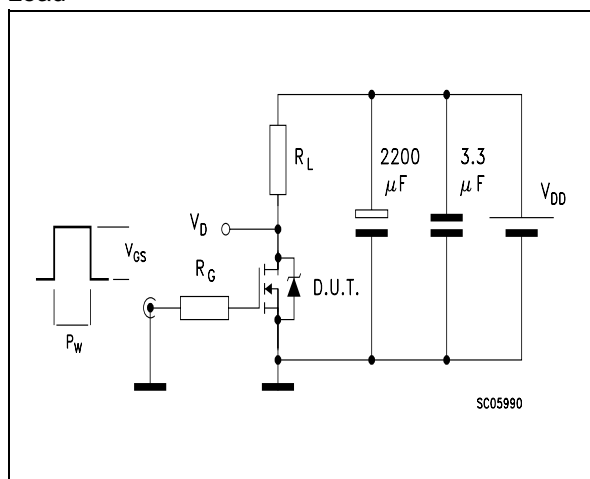


Fig. 4: Gate Charge test Circuit

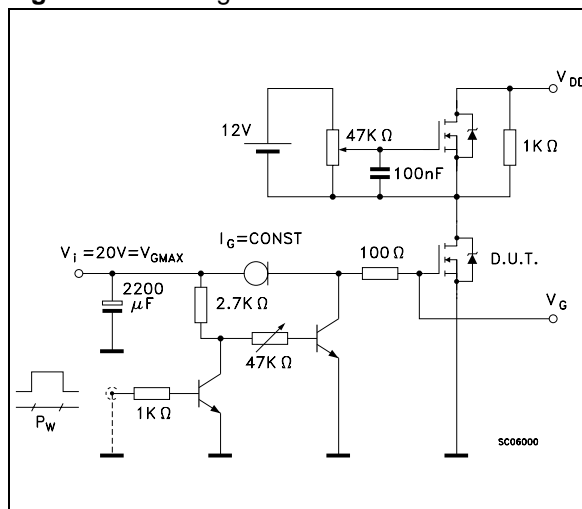
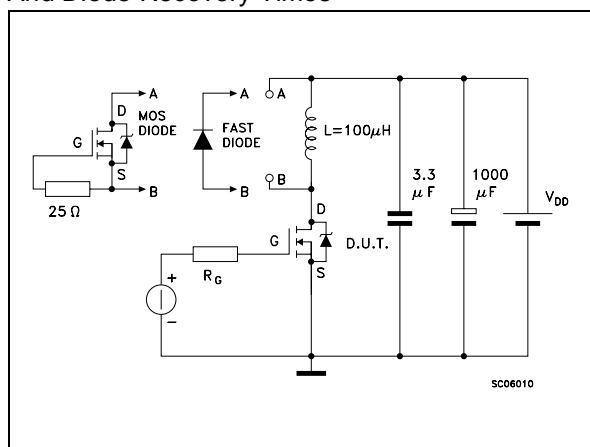


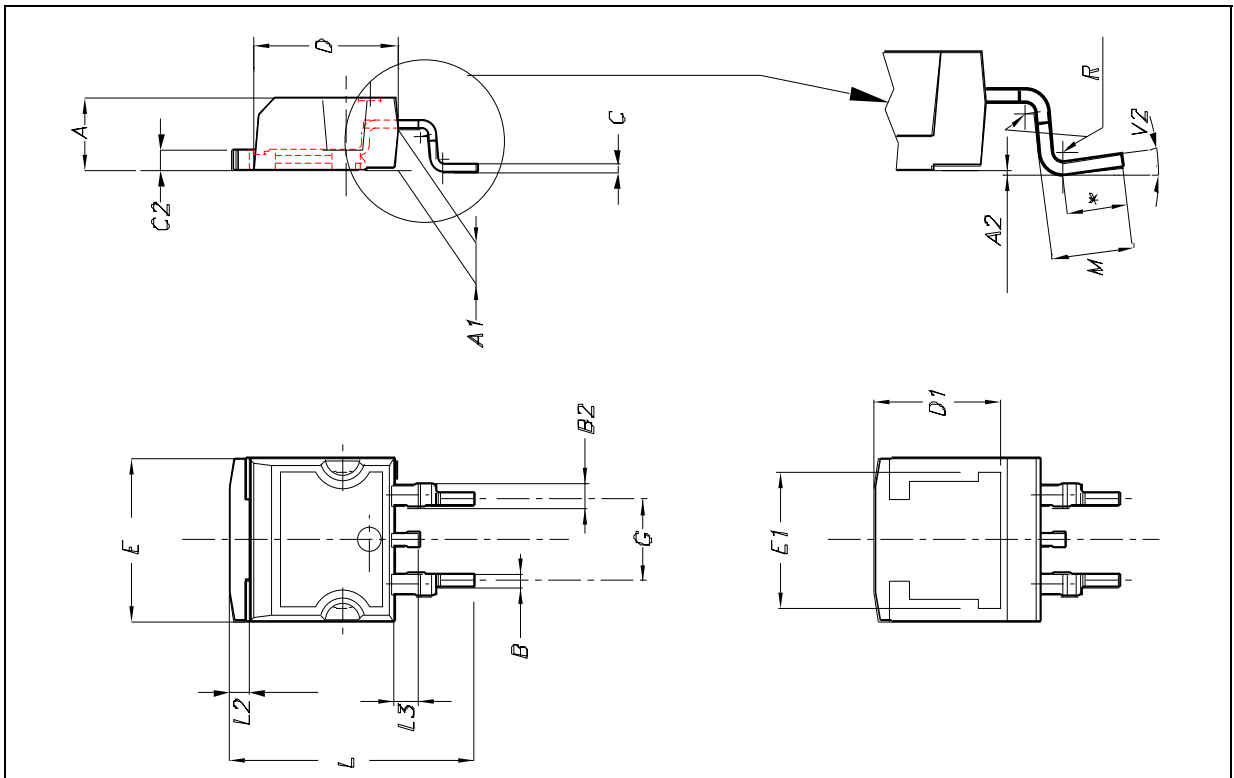
Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



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D<sup>2</sup>PAK MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.028		0.037
B2	1.14		1.7	0.045		0.067
C	0.45		0.6	0.018		0.024
C2	1.21		1.36	0.048		0.054
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.394		0.409
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.591		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.069
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°	0°		8°

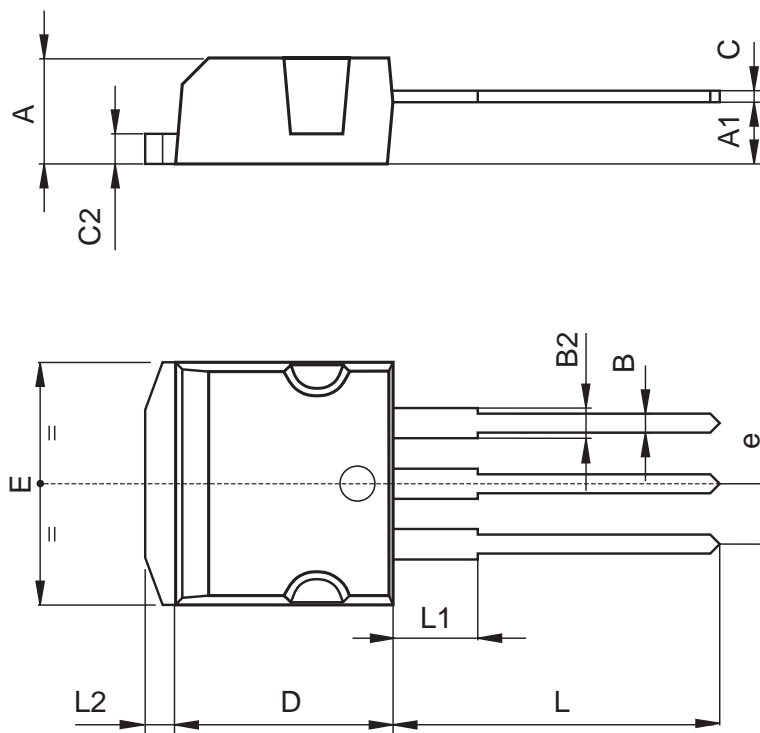






TO-262 (I<sup>2</sup>PAK) MECHANICAL DATA

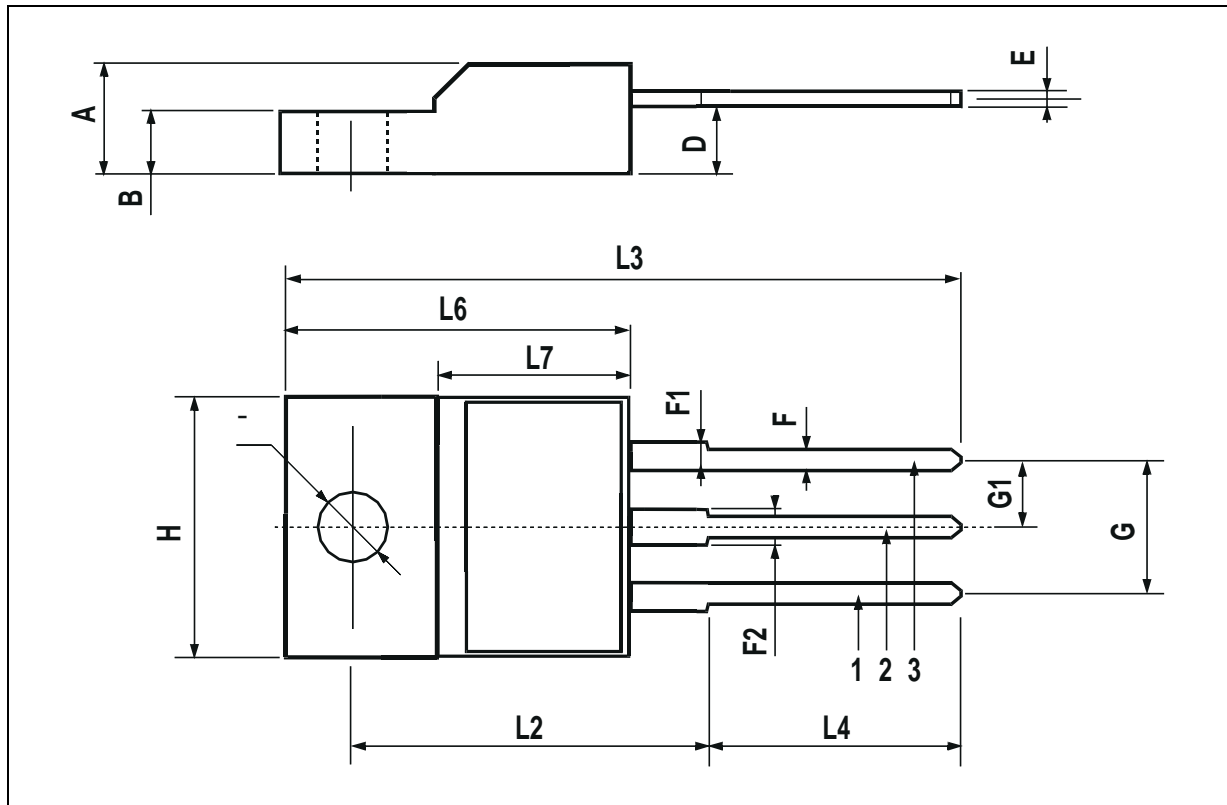
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
e	2.4		2.7	0.094		0.106
E	10		10.4	0.393		0.409
L	13.1		13.6	0.515		0.531
L1	3.48		3.78	0.137		0.149
L2	1.27		1.4	0.050		0.055



P011P5/E

**TO-220FP MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126





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