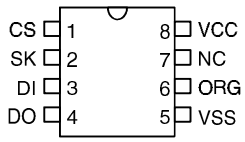
Features

- Operating voltage VCC: 2.4~5.5V
- Low power consumption
  - Operating: 5mA max.
  - Standby: 10μA max.
- User selectable internal organization
  - 1K(HT93LC46): 128 × 8 or 64 × 16
  - 2K(HT93LC56): 256 × 8 or 128 × 16
  - 4K(HT93LC66): 512 × 8 or 256 × 16
- Three-wire Serial Interface
- Write cycle time: 2ms (Max.)
- Automatic erase-before-write operation
- Word/chip erase and write operation
- Write operation with built-in timer
- Software controlled write protection
- 10-year data retention after 100K rewrite cycles
- 10^6 rewrite cycles per word
- 8-pin DIP/SOP package

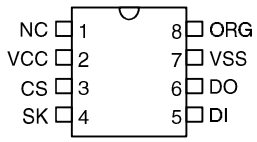
General Description

The HOLTEK's HT93LC46/56/66 is a 1K/2K/4K-bit low voltage nonvolatile, serial electrically erasable programmable read only memory device using the CMOS floating gate process. Its 1024/2048/4096 bits of memory are organized into 64/128/256 words of 16 bits each, when the ORG pin is connected to V_{CC} and 128/256/512 words of 8 bits each when it is tied to GND. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. By popular microcontroller, the versatile serial interface including chip select (CS), serial clock (SK), data input (DI) and data output (DO) can be easily controlled.

Pin Assignment

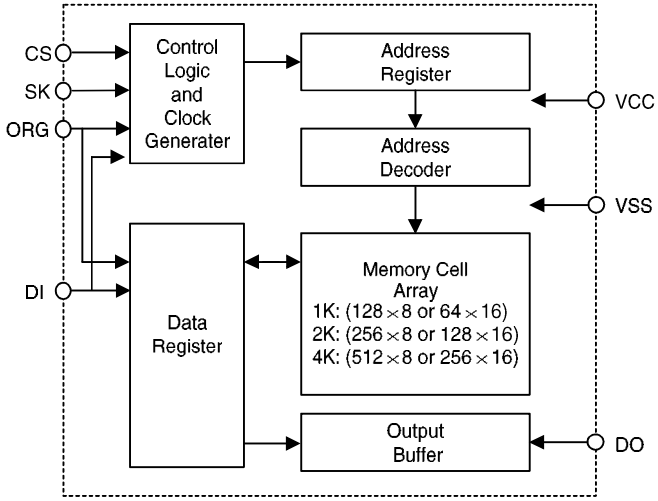


HT93LC46/56/66
– 8 DIP/SOP-A



HT93LC46/56/66
– 8 SOP-B

Block Diagram



Pin Description

Pin Name	I/O	Description
CS	I	Chip select input
SK	I	Serial clock input
DI	I	Serial data input
DO	O	Serial data output
VSS	I	Negative power supply
ORG	I	Internal Organization
NC	—	No connection
VCC	I	Positive power supply

Absolute Maximum Ratings*

Operation Temperature (Industrial) ..... –40°C to 85°C

Operation Temperature (Commercial) ..... 0°C to 70°C

Applied V_{CC} Voltage with Respect to GND ..... –0.3V to 6.0V

Applied V_{SS} Voltage on any Pin with Respect to GND ..... –0.3V to V_{SS}+0.3V

Supply READ Voltage ..... 2.4V to 5.5V

*Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Read operation

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{CC}	Operating Voltage	—	—	2.4	—	5.5	V
I_{CC1}	Operating Current (TTL)	5V	DO unload, SK=1MHz	—	—	5	mA
I_{CC2}	Operating Current (CMOS)	5V	DO unload, SK=1MHz	—	—	5	mA
I_{STB}	Standby Current (CMOS)	5V	CS=SK=DI=0V	—	—	10	μA
I_{LI}	Input Leakage Current	5V	$V_{IN}=V_{SS}$~V_{CC}	0	—	1	μA
I_{LO}	Output Leakage Current	5V	$V_{OUT}=V_{SS}$~V_{CC} CS=0V	0	—	1	μA
V_{IL}	Input Low Voltage	4.5~5.5V	—	0	—	0.8	V
		2.4~4.5V	—	0	—	$0.1V_{CC}$	V
V_{IH}	Input High Voltage	4.5~5.5V	—	2	—	V_{CC}	V
		2.4~4.5V	—	$0.9V_{CC}$	—	V_{CC}	V
V_{OL}	Output Low Voltage	4.5~5.5V	I_{OL}=2.1mA	—	—	0.4	V
		2.4~4.5V	I_{OL}=10μA	—	—	0.2	V
V_{OH}	Output High Voltage	4.5~5.5V	I_{OH}=–400μA	2.4	—	—	V
		2.4~4.5V	I_{OH}=–10μA	V_{CC}–0.2	—	—	V
C_{IN}	Input Capacitance	—	V_{IN}=0V, f=250kHz	—	—	5	pF
C_{OUT}	Output Capacitance	—	V_{OUT}=0V, f=250kHz	—	—	5	pF

A.C. Characteristics

Read operation

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
f_{SK}	Clock Frequency	2.4~.55V		0	—	500	kHz
		4.5~5.5V		0	—	2000	
t_{SKH}	SK High Time	2.4~.55V		1000	—	—	ns
		4.5~5.5V		250	—	—	
t_{SKL}	SK Low Time	2.4~.55V		1000	—	—	ns
		4.5~5.5V		250	—	—	
t_{CSS}	CS Setup Time	2.4~.55V		200	—	—	ns
		4.5~5.5V		50	—	—	
t_{CSH}	CS Hold Time	2.4~.55V		0	—	—	ns
		4.5~5.5V		0	—	—	
t_{CDS}	CS Deselect Time	2.4~.55V		1000	—	—	ns
		4.5~5.5V		250	—	—	
t_{DIS}	DI Setup Time	2.4~.55V		400	—	—	ns
		4.5~5.5V		100	—	—	
t_{DIH}	DI Hold Time	2.4~.55V		400	—	—	ns
		4.5~5.5V		100	—	—	
t_{PD1}	DO Delay to “1”	2.4~.55V		—	—	2000	ns
		4.5~5.5V		—	—	500	
t_{PD0}	DO Delay to “0”	2.4~.55V		—	—	2000	ns
		4.5~5.5V		—	—	500	
t_{SV}	Status Valid Time	2.4~.55V		—	—	2000	ns
		4.5~5.5V		—	—	500	
t_{HZ}	DO Disable Time	2.4~.55V		400	—	—	ns
		4.5~5.5V		100	—	—	
t_{PR}	Write Cycle Time	2.4~.55V		—	—	2	ms
		4.5~5.5V		—	—	2	

Functional Description

The HT93LC46/56/66 is accessed via a three-wire serial communication interface. The device is arranged into 64/128/256 words by 16 bits or 128/256/512 words by 8 bits depending whether the ORG pin is connected to VCC or GND. The HT93LC46/56/66 contains seven instructions: READ, ERASE, WRITE, EWEN, EWDS, ERAL and WRAL. When the user selectable internal organization is arranged into 64/128/256×16 (128/256/512×8), these instructions are all made up of 9/11/12 bits data: 1 start bit, 2 op code bits and 6/8/9 address bits.

By using the control signal CS, SK and data input signal DI, these instructions can be given to the HT93LC46/56/66 separately. These serial instruction data presented at the DI input will be written into the device at the rising edge of SK. During the READ cycle, DO pin acts as the data output and during the WRITE or ERASE cycle, DO pin indicates the BUSY/READY status. When the DO pin is active for read data or as a BUSY/READY indicator the CS pin must be high; otherwise DO pin will be in a high-impedance state. For successful instructions, CS must be low once after the instruction is sent. After power on, the device is by default in the EWDS state. And, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. The following are the functional descriptions and timing diagrams of all seven instructions.

READ

The READ instruction will stream out data at a specified address on the DO pin. The data on DO pin changes during the low-to-high edge of SK signal. The 8 bits or 16 bits data stream is preceded by a logical '0' dummy bit. Irrespective of the condition of the EWEN or EWDS instruction, the READ command is always valid and independent of these two instructions. After the data word has been read the internal address will be automatically incremented by 1 allowing the next consecutive data word to be read out without entering further address data. The address will wrap around with CS High until CS returns to LOW.

EWEN/EWDS

The EWEN/EWDS instruction will enable or disable the programming capabilities. At both the power on and power off state the device automatically entered the disable mode. Before a WRITE, ERASE, WRAL or ERAL instruction is given, the programming enable instruction EWEN must be issued, otherwise the ERASE/WRITE instruction is invalid. After the EWEN instruction is issued, the programming enable condition remains until power is turned off or a EWDS instruction is given. No data can be written into the device in the programming disabled state. By so doing, the internal memory data can be protected.

ERASE

The ERASE instruction erases data at the specified addresses in the programming enable mode. After the ERASE op-code and the specified address have been issued, the data erase is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signals for the internal erase, so the SK clock is not required. During the internal erase, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over, the DO pin will return to high and further instructions can be executed.

WRITE

The WRITE instruction writes data into the device at the specified addresses in the programming enable mode. After the WRITE op-code and the specified address and data have been issued, the data writing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signal for the internal writing, so the SK clock is not required. The auto-timing write cycle includes an automatic erase-before-write capability. So, it is not necessary to erase data before the WRITE instruction. During the internal writing, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over, the DO pin will return to high and further instructions can be executed.

ERAL

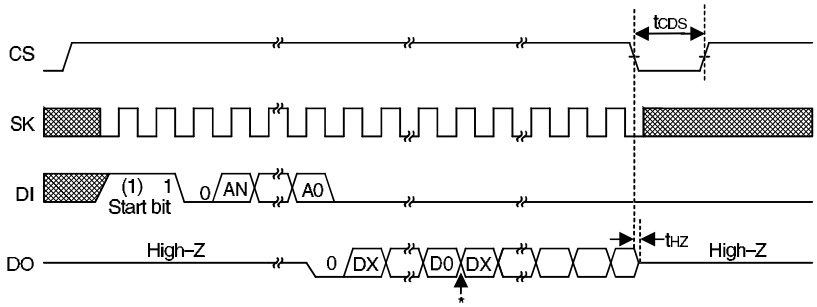
The ERAL instruction erases the entire 128/256x16 or 256/512x8 memory cells to logical '1' state in the programming enable mode. After the erase-all instruction set has been issued, the data erase feature is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signal for the erase-all operation, so the SK clock is not required. During the internal erase-all operation, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over, the DO pin will return to high and further instruction can be executed.

WRAL

The WRAL instruction writes data into the entire 64/128/256×16 or 128/256/512×8 memory cells in the programming enable mode. After the write-all instruction set has been issued, the data writing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signals for the write-all operation, so the SK clock is not required. During the internal write-all operation, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over the DO pin will return to high and further instruction can be executed.

Timing Diagrams

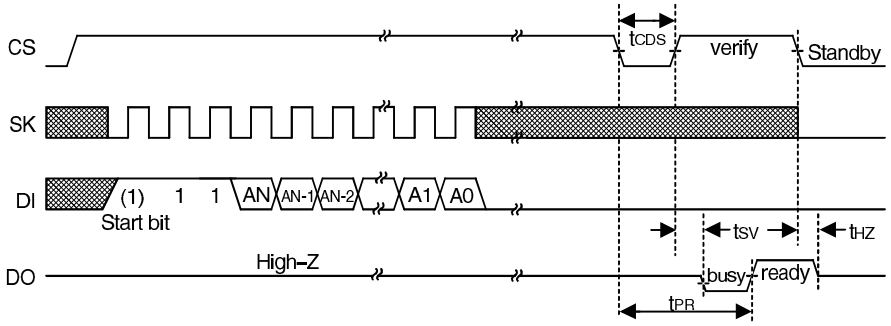
READ



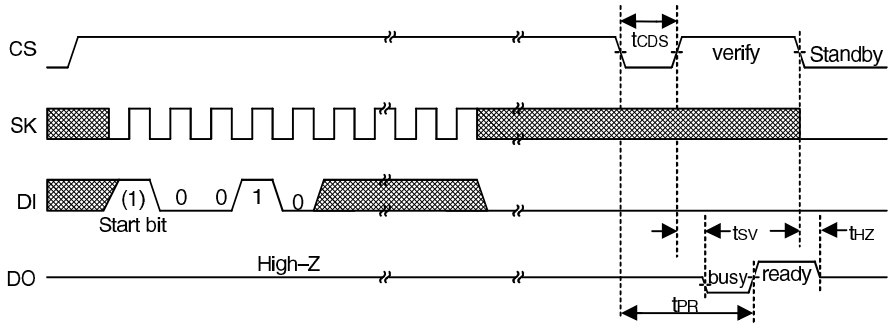
* Address bit A7 becomes a "don't care" (X16 mode) on 93LC56
* Address bit A8 becomes a "don't care" (X8 mode) on 93LC56
* Address pointer automatically cycles to the next word

Mode	(X16)	(X8)
AN	A7	A8
DX	D15	D7

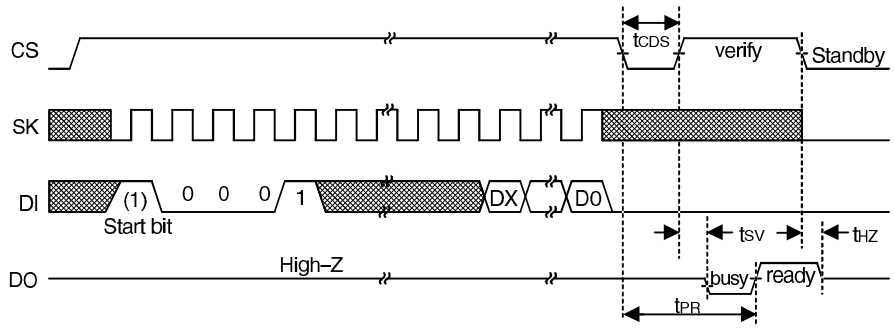
WRITE



ERAL



WRAL



Instruction Set Summary

HT93LC46

Instruction	Comments	Start bit	Op Code	Address ORG=0 X8	Address ORG=1 X16	Data ORG=0 X8	Data ORG=1 X16
READ	Read data	1	10	A6~A0	A5~A0	D7~D0	D15~D0
ERASE	Erase data	1	11	A6~A0	A5~A0	—	
WRITE	Write data	1	01	A6~A0	A5~A0	D7~D0	D15~D0
EWEN	Erase/Write Enable	1	00	11XXXXXXX	11XXXXXX	—	
EWDS	Erase/Write Disable	1	00	00XXXXXXX	00XXXXXX	—	
ERAL	Erase All	1	00	10XXXXXXX	10XXXXXX	—	
WRAL	Write All	1	00	01XXXXXXX	01XXXXXX	D7~D0	D15~D0

HT93LC56

Instruction	Comments	Start bit	Op Code	Address ORG=0 X8	Address ORG=1 X16	Data ORG=0 X8	Data ORG=1 X16
READ	Read data	1	10	A7~A0	A6~A0	D7~D0	D15~D0
ERASE	Erase data	1	11	A7~A0	A6~A0	—	
WRITE	Write data	1	01	A7~A0	A6~A0	D7~D0	D15~D0
EWEN	Erase/Write Enable	1	00	11XXXXXXX	11XXXXXX	—	
EWDS	Erase/Write Disable	1	00	00XXXXXXX	00XXXXXX	—	
ERAL	Erase All	1	00	10XXXXXXX	10XXXXXX	—	
WRAL	Write All	1	00	01XXXXXXX	01XXXXXX	D7~D0	D15~D0

HT93LC66

Instruction	Comments	Start bit	Op Code	Address ORG=0 X8	Address ORG=1 X16	Data ORG=0 X8	Data ORG=1 X16
READ	Read data	1	10	A8~A0	A7~A0	D7~D0	D15~D0
ERASE	Erase data	1	11	A8~A0	A7~A0	—	
WRITE	Write data	1	01	A8~A0	A7~A0	D7~D0	D15~D0
EWEN	Erase/Write Enable	1	00	11XXXXXXX	11XXXXXX	—	
EWDS	Erase/Write Disable	1	00	00XXXXXXX	00XXXXXX	—	
ERAL	Erase All	1	00	10XXXXXXX	10XXXXXX	—	
WRAL	Write All	1	00	01XXXXXXX	01XXXXXX	D7~D0	D15~D0

Ordering Information

Access Time (ms)	I_{CC} (mA) (Max.)	I_{STB} (μA) (Max.)	Package	Ordering Code	Temperature Range
2	5	10	8 DIP	HT93LC46 — 5/P	Commercial 0°C to 70°C
			8 SOP	HT93LC46A — 5/S	
				HT93LC46B — 5/S	
	5	10	8 DIP	HT93LC46 — 5/IP	Industrial –40°C to 85°C
			8 SOP	HT93LC46A — 5/IS	
				HT93LC46B — 5/IS	
2	5	10	8 DIP	HT93LC56 — 5/P	Commercial 0°C to 70°C
			8 SOP	HT93LC56A — 5/S	
				HT93LC56B — 5/S	
	5	10	8 DIP	HT93LC56 — 5/IP	Industrial –40°C to 85°C
			8 SOP	HT93LC56A — 5/IS	
				HT93LC56B — 5/IS	
2	5	10	8 DIP	HT93LC66 — 5/P	Commercial 0°C to 70°C
			8 SOP	HT93LC66A — 5/S	
				HT93LC66B — 5/S	
	5	10	8 DIP	HT93LC66 — 5/IP	Industrial –40°C to 85°C
			8 SOP	HT93LC66A — 5/IS	
				HT93LC66B — 5/IS