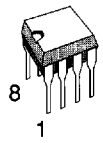
SGS-THOMSON MICROELECTRONICS

S G S-THOMSON

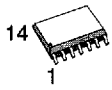
ST24C04

SERIAL ACCESS CMOS 4K (2 by 256 x 8) EEPROM

- 1,000,000 ERASE/WRITE CYCLES MINIMUM, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 3V TO 5.5V POWER SUPPLY
- USER DEFINED WRITE PROTECT AREA
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE AND MULTIBYTE WRITE (UP TO 4 BYTES)
- PAGE WRITE (UP TO 8 BYTES)
- BYTE, RANDOM AND SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- GUARANTED 4kV ESD PROTECTION, USING HUMAN BODY MODEL



PSDIP8 (B)
0.25mm Frame



PSO14 (ML)

DESCRIPTION

The ST24C04 is a 4K bit electrically erasable programmable memory (EEPROM), organised as 2 blocks of 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memory is compatible with the I^2C standard, two wire, serial interface which uses a bi-directional data bus and serial clock. The ST24C04 carries a built-in 4 bit, unique device identification code corresponding to the I^2C bus definition. This is used together with a 2 bit chip enable input to form a 6 bit memory select signal. In this way up to 4

Table 1. Signal Names

PRE	Write Protect Enable
E1 - E2	Chip Enable Inputs
SDA	Serial Data Address Input Output
SCL	Serial Clock
MODE	Write Mode
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

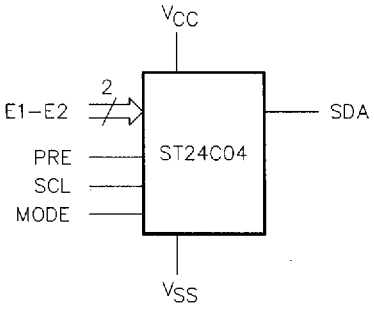


Figure 2A. DIP Pin Connections

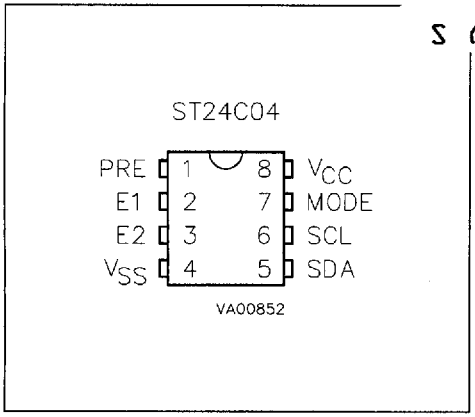
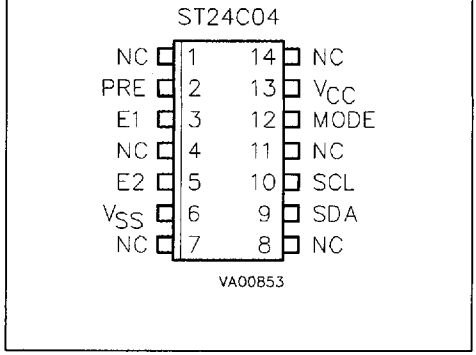


Figure 2B. SO Pin Connections

S G S-THOMSON T-46-13-28



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(PSO14 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)			4000	V
	Electrostatic Discharge Voltage (Machine model)			1000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

ST24C04's may be attached to the I^2C bus and selected individually.

The ST24C04 behaves as a slave device in the I^2C protocol with all memory operations synchronised by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 6 device select bits, one block select bit, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the upper block of the memory may be write protected. The protected area is programmable to start on any 8 byte boundary. Protection is enabled by setting a memory bit flag and the PRE signal input.

OPERATING MODES

There are both Read and Write modes. Each is entered by the correct sequence of serial bits sent to the device on the SDA bus line. For some Write modes the status of the MODE input is also used to set the operating mode. For the Protect mode

OPERATING MODES (cont'd)

the status of the PRE input determines whether protection is enabled or disabled.

The 8 bits sent after a START condition are made up of a device select of 4 bits that identify the device type, 2 chip enable bits, one block select bit and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation.

There are three modes both for read and write. These are summarised in Table 4 and described below.

Byte Write. In this mode a device select is sent with the $R\overline{W}$ bit at '0', followed by the address of the byte. This is followed by the 8 bit data to be written during the programing cycle.

Multibyte Write and Page Write. In these modes up to 4 or up to 8 bytes respectively may be written in one programing cycle. Multibyte Write mode is activated when the MODE pin is at V_{IH} level and Page Write when MODE is at V_{IL}. A device select is sent with the $R\overline{W}$ bit at '0', followed by the address of the first byte. This is followed by the data bytes to write. The bytes are written in the programing cycle. All 8 bytes written in the Page Write mode must have the same five upper address bits.

Current Address Read. In this mode the device select is sent with the $R\overline{W}$ bit at '1'. The address of the previous byte accessed is automatically incremented and the new byte read.

Random Address Read. This mode allows random access to the memory. A device select is sent with the $R\overline{W}$ bit at '0' (write), followed by the byte address. Then a new START condition is forced with the same device select is sent with the $R\overline{W}$ bit at '1' (read) and the byte is read.

Sequential Read. This mode starts with either a Current Address or Random Address read sequence, it reads consecutive bytes as long as the bus master acknowledges each one without generating a STOP condition.

Write Protect. Data in the upper 256 byte block of the memory may be write protected. The protection starts at any 8 byte boundary. The address at which protection starts is defined by the contents of the upper 5 bits (b7- b3 of the top memory location (block 1, byte address 1FFh). Bit 2 of this memory location is used as a flag to indicate that the protection is enabled (b2 = '0') or disabled (b2 = '1'). The lower two bits, b1 & b0, are not used. The sequence to follow to use the memory protect feature is as follows: write the memory contents to be protected into the top of the upper block of the memory, up to location 1FEh. Then establish the memory protect area and set the protection by writing the correct contents into location 1FFh. The area will now be protected when the PRE signal is active (High).

Table 3. Device Select Code

	Device Code				Chip Enable		Block Select	$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	A8	$R\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	$R\overline{W}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'	X		START, Device Select, $R\overline{W}$ = '0', Address
	'1'	X	1	reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 512	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IH} or V_{IL}	1	START, Device Select, $R\overline{W}$ = '0'
Multibyte Write	'0'	V_{IH}	4	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, $R\overline{W}$ = '0'

Note: X = V_{IH} or V_{IL}

Figure 3. Memory Protection

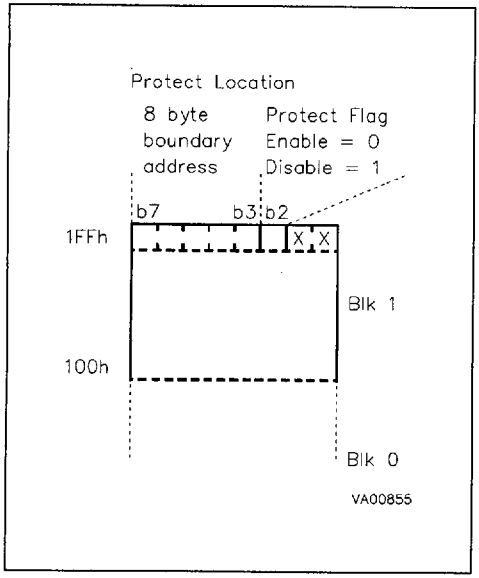


Figure 4. Typical Interface

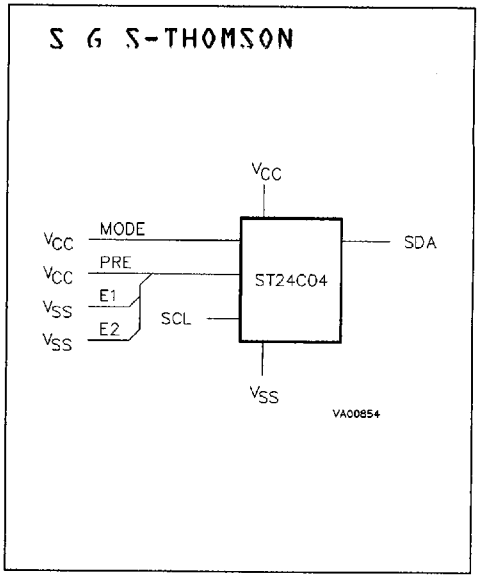
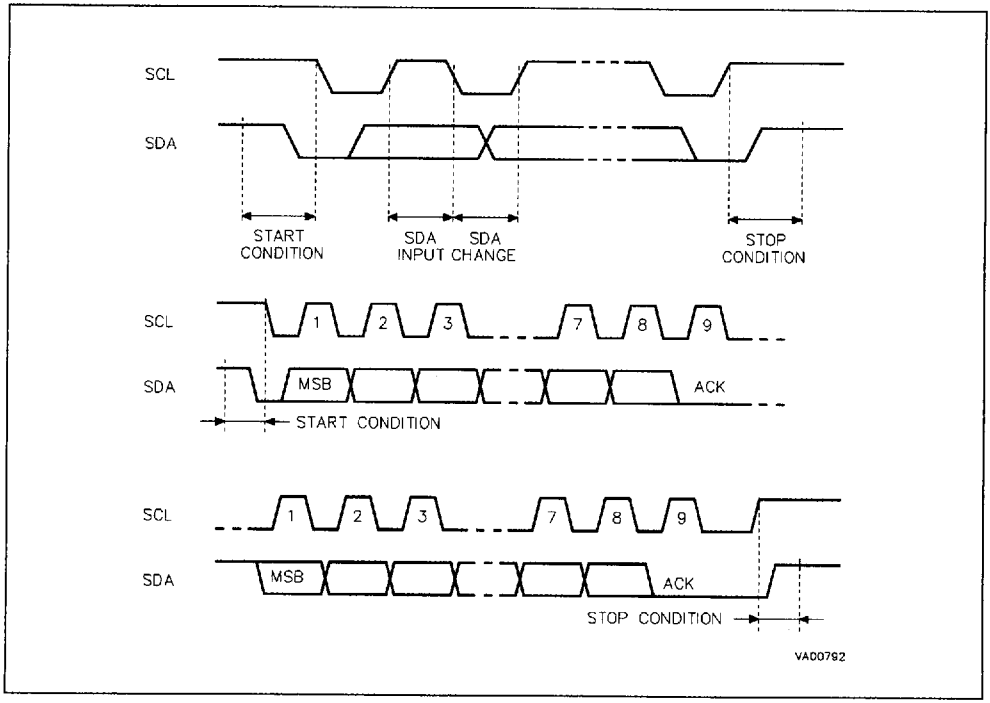


Figure 5. I²C Bus Protocol



AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 6. AC Testing Input Output Waveforms

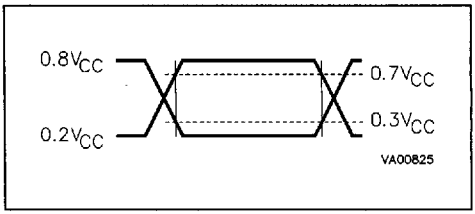


Table 7. Capacitance (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)		8	pF
C_{IN}	Input Capacitance (Other)		6	pF

Note: 1. Sampled only not 100% tested

Figure 7. AC Waveforms

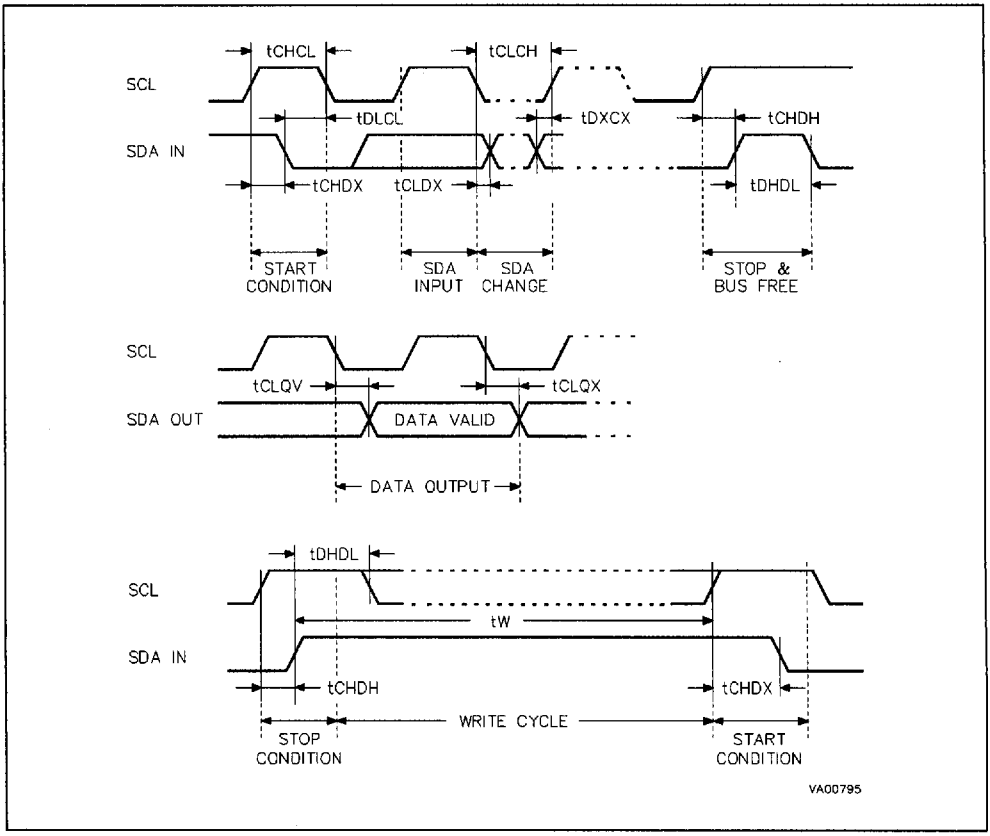


Table 5. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±2	µA
I_{CC}	Supply Current	f = 100kHz		2	mA
I_{CC1}	Supply Current (Standby)	V_{IN} = 0V or V_{CC}		100	µA
V_{IL}	Input Low Voltage (SCL & SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL & SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E1 - E2, PRE, MODE)		–0.3	0.5	V
V_{IH}	Input High Voltage (E1 - E2, PRE, MODE)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA		0.4	V

Table 6. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Output Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock High to Output Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{LPF}	T_I	Input Low Pass 1st Order Filter Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a re START condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive rows (upper 5 MSB must not change) the maximum programming time is doubled to 20ms.

Table 8. Endurance and Data Retention

Endurance	The ability of the EEPROM to withstand Erase/Write cycles without failure.
Failure	A failure after cycling is defined as any bit that cannot be written or loses its data after a subsequent retention bake of 2 years equivalent at 55 °C.
Guarantee	With 60% confidence, more than 99.9% of units can be cycled over 1,000,000 times.

OPERATING MODE (cont'd)

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input High). If the Multibyte write of up to 4 bytes starts at the location just before the protected area then it is able to write over the first 3 bytes in the protected area. The true area protected is therefore smaller and equal to the content of defined in the location 1FFh plus 3 bytes. This does not apply to the Page write mode as the address counter rolls over and thus cannot go above the 8 byte lower boundary of the protected area.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input is used to synchronise all Data In and Data Out of the memory. A resistor must be connected from the SCL line to V_{CC} to act as a pull up.

Serial Data (SDA). The SDA signal is bi-directional and used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up.

Chip Enable (E1 - E2). These chip enable inputs are used to set the 2 least significant bits of the 6 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL, compatible.

Mode (MODE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

Protect Enable (PRE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

DEVICE OPERATION

The ST24C04 supports the I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24C04 is always a slave device is all communications.

Communications Protocol

Data Transition or Change. Data changes on the SDA line must only occur when the SCL clock is low. SDA transitions while the clock is high are used to identify START or STOP conditions.

Start Condition. START is identified by a high to low transition of the data bus SDA signal while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24C04 continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the data bus SDA signal while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24C04 and the bus master and forces the device into the standby power state.

Acknowledge Bit. An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24C04 samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing

To start communication between the master and the slave ST24C04, the master must initiate a START condition. Following this the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code, block select bit and a READ or WRITE instruction.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For the ST24C04 these are fixed as 1010b (0Ah).

The following 2 bits identify the specific ST24C04 on the bus. They are matched to the chip enable signals E1 - E2. Thus up to 4 ST24C04's can be connected on the same bus giving a memory capacity total of 16k bits. After a START condition all ST24C04's on the bus will identify the device code and compare the following 2 bits to the chip enable inputs E1 - E2. If a match is found the corresponding ST24C04 will acknowledge the identification on the SDA bus during the 9th bit time.

The 7th bit sent selects one of the two blocks of 256 bytes of the memory, effectively acting as memory address A8 (A7 - A0 byte addresses are sent later).

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations.

Write Operation

The Multibyte Write mode is available when the MODE signal is at V_{IH} and the Page Write mode when this signal is at V_{IL}. The MODE signal may be driven dynamically with CMOS input levels. The Byte Write mode is independant of the state of the MODE signal and the pin could be left floating if only this mode was to be used. However it is recommended that the signal is connected to either V_{IH} or V_{IL}.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The ST24C04 acknowledges this and waits for a byte address. The byte address of 8 bits provides access to any of the 256 bytes in the selected block of the memory. After receipt of the byte address the ST24C04 again responds with an acknowledge.

Byte Write. In the Byte Write mode the master sends one data byte, this is acknowledged by the ST24C04. The master then terminates the transfer by generating a STOP condition.

Multibyte Write. For the Multibyte mode the MODE signal must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the ST24C04. The transfer is terminated by the master generating a STOP condition.

Page Write. For the Page mode the MODE signal must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A8-A4) are the same. The master sends from 1-8 bytes of data, which are each acknowledged by the ST24C04. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

For any write mode the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the ST24C04 will not respond to any request. The duration of this cycle is tw = 10ms maximum except when, in the Multibyte Write mode, bytes are accessed that are on different rows (that is have different values for the 5 most significant address bits), when the programing time is doubled to a maximum of 20ms.

Read Operation

Read operations are independent of the state of the MODE signal.

Current Address Read. The ST24C04 has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $R\overline{W}$ bit set to '1'. The ST24C04 acknowledges this and immediately outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the byte address into the memory. This is followed by another START condition from the master and the byte address repeated with the $R\overline{W}$ bit set to '1'. The ST24C04 acknowledges this and immediately outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

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Figure 8. Write Modes Sequence

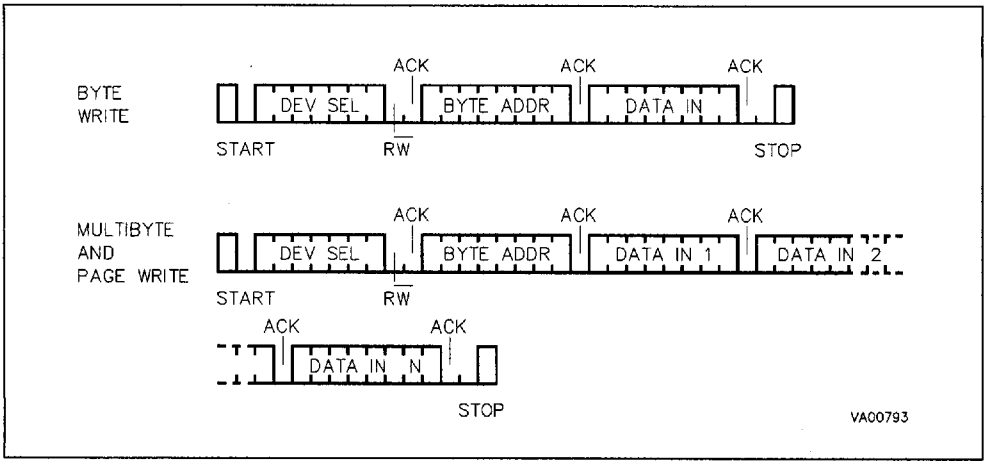
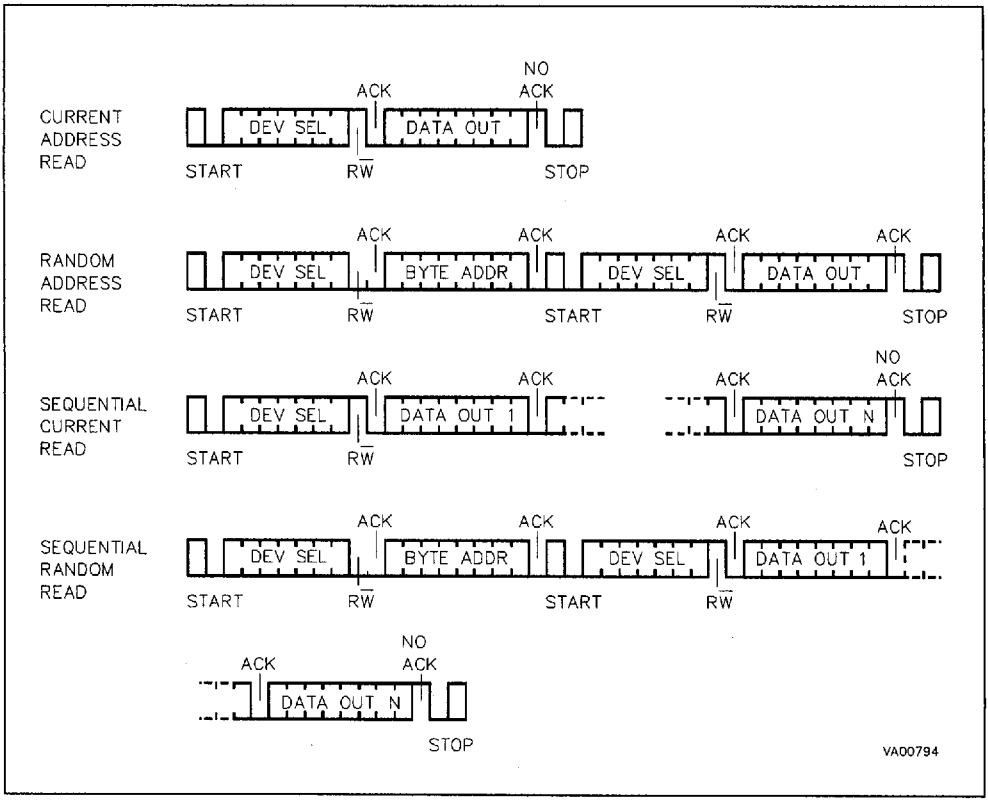


Figure 9. Read Modes Sequence



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T-46-13-28

DEVICE OPERATION (cont'd)

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However in this case the master DOES acknowledge the data byte output and the ST24C04 continues to output the next byte in sequence. To terminate the stream of bytes the master must NOT acknowledge the last byte output, but must generate a STOP sequence. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of 512 the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24C04 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24C04 terminates the data transfer and switches to a receiver state. The STOP condition is used only in the WRITE modes to initiate the write cycle and is ignored in the READ modes.

ORDERING INFORMATION

Example: ST24C04 ML 1 013TR

Package		Temperature Range		Option	
B	PSDIP8 0.25 mm Frame	1	0 to 70 °C	013TR	Tape & Reel
ML	PSO14	3	–40 to 125 °C		
		6	–40 to 85 °C		

Parts are shipped with the memory content set at all "1's" (0FFh).

For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.