V33642R05KG
3.3 VOLT 2M x 64 HIGH PERFORMANCE UNBUFFERED DIMM EDO MODULE

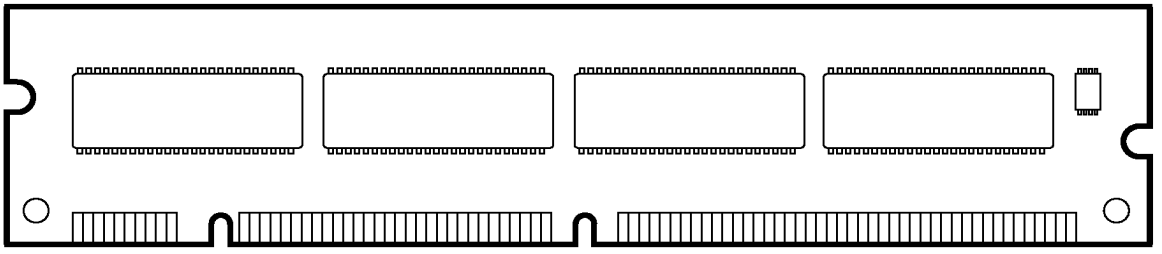
HIGH PERFORMANCE	50	60
Max. $\overline{RAS}$ Access Time, (t_{RAC})	50 ns	60 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	13 ns	15 ns
Min. Cycle Time, (t_{RC})	84 ns	104 ns
Min. EDO Mode Cycle Time, (t_{PC})	20 ns	25 ns

Features

- 168 Pin JEDEC standard, Unbuffered 16 byte dual in-line EDO module
- 1 Bank 2M x 64 organization
- Utilizes 8 1M x 16 EDO DRAMs in SOJ packages
- Fast Access Times: 50 or 60 ns
- JEDEC standard EDO DRAM
- Low power dissipation
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
  - Refresh Interval: 4096 cycles/64 ms 4K
- Single 3.3V ±10% Power Supply
- Decoupling capacitors mounted on substrate
- LVTTL Interface
- Fully pin and architecture compatible with 168 pin unbuffered DRAM DIMMs
- Serial Present Detect (SPD)

Description

The V33642R05KG memory module is organized as 2,097,152 x 64 bits in a 168 pin dual in-line memory module. The 2M x 64 memory uses 8 Mosel Vitelic 1M x 16 EDO DRAMs. The x 64 modules are ideal for use in high performance computer systems where increased memory density and fast access time are required.



V35642R05KG-01

Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)		Power	Temperature Mark
	K	T	50	60	Std.	
0°C to 70°C	•	•	•	•	•	Blank
–40°C to +85°C	•	•	•	•	•	I

Pin Configurations (Front Side/Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	$\overline{CAS1}$	57	I/O19	85	VSS	113	$\overline{CAS5}$	141	I/O51
2	I/O1	30	$\overline{RAS0}$	58	I/O20	86	I/O33	114	$\overline{RAS1}$	142	I/O52
3	I/O2	31	$\overline{OE0}$	59	VCC	87	I/O34	115	NC	143	VCC
4	I/O3	32	VSS	60	I/O21	88	I/O35	116	VSS	144	I/O53
5	I/O4	33	A0	61	NC	89	I/O36	117	A1	145	NC
6	VCC	34	A2	62	NC	90	VCC	118	A3	146	NC
7	I/O5	35	A4	63	NC	91	I/O37	119	A5	147	NC
8	I/O6	36	A6	64	VSS	92	I/O38	120	A7	148	VSS
9	I/O7	37	A8	65	I/O22	93	I/O39	121	A9	149	I/O54
10	I/O8	38	A10	66	I/O23	94	I/O40	122	A11	150	I/O55
11	I/O9	39	NC	67	I/O24	95	I/O41	123	NC	151	I/O56
12	VSS	40	VCC	68	VSS	96	VSS	124	VCC	152	VSS
13	I/O10	41	VCC	69	I/O25	97	I/O42	125	NC	153	I/O57
14	I/O11	42	NC	70	I/O26	98	I/O43	126	NC	154	I/O58
15	I/O12	43	VSS	71	I/O27	99	I/O44	127	VSS	155	I/O59
16	I/O13	44	$\overline{OE2}$	72	I/O28	100	I/O45	128	NC	156	I/O60
17	I/O14	45	$\overline{RAS2}$	73	VCC	101	I/O46	129	$\overline{RAS3}$	157	VCC
18	VCC	46	$\overline{CAS2}$	74	I/O29	102	VCC	130	$\overline{CAS6}$	158	I/O61
19	I/O15	47	$\overline{CAS3}$	75	I/O30	103	I/O47	131	$\overline{CAS7}$	159	I/O62
20	I/O16	48	$\overline{WE2}$	76	I/O31	104	I/O48	132	NC	160	I/O63
21	NC	49	VCC	77	I/O32	105	NC	133	VCC	161	I/O64
22	NC	50	NC	78	VSS	106	NC	134	NC	162	VSS
23	VSS	51	NC	79	NC	107	VSS	135	NC	163	NC
24	NC	52	NC	80	NC	108	NC	136	NC	164	NC
25	NC	53	NC	81	NC	109	NC	137	NC	165	SA0
26	VCC	54	VSS	82	SDA	110	VCC	138	VSS	166	SA1
27	$\overline{WE0}$	55	I/O17	83	SCL	111	NC	139	I/O49	167	SA2
28	$\overline{CAS0}$	56	I/O18	84	VCC	112	$\overline{CAS4}$	140	I/O50	168	VCC

Pin Names

A0–A11	Addresses
I/O1-I/O65	Data Inputs/Outputs
$\overline{RAS0}$-$\overline{RAS3}$	Row Address Strobes
$\overline{CAS0}$-$\overline{CAS7}$	Column Address Strobes
$\overline{WE0}$, $\overline{WE2}$	Write Enables
$\overline{OE0}$, $\overline{OE2}$	Output Enables
SDA	Serial Input/Output
SCL	Serial Clock
SA0–SA2	Serial PD Address
VCC	Power Supply (+3.3V)
VSS	Ground
NC	No Connection

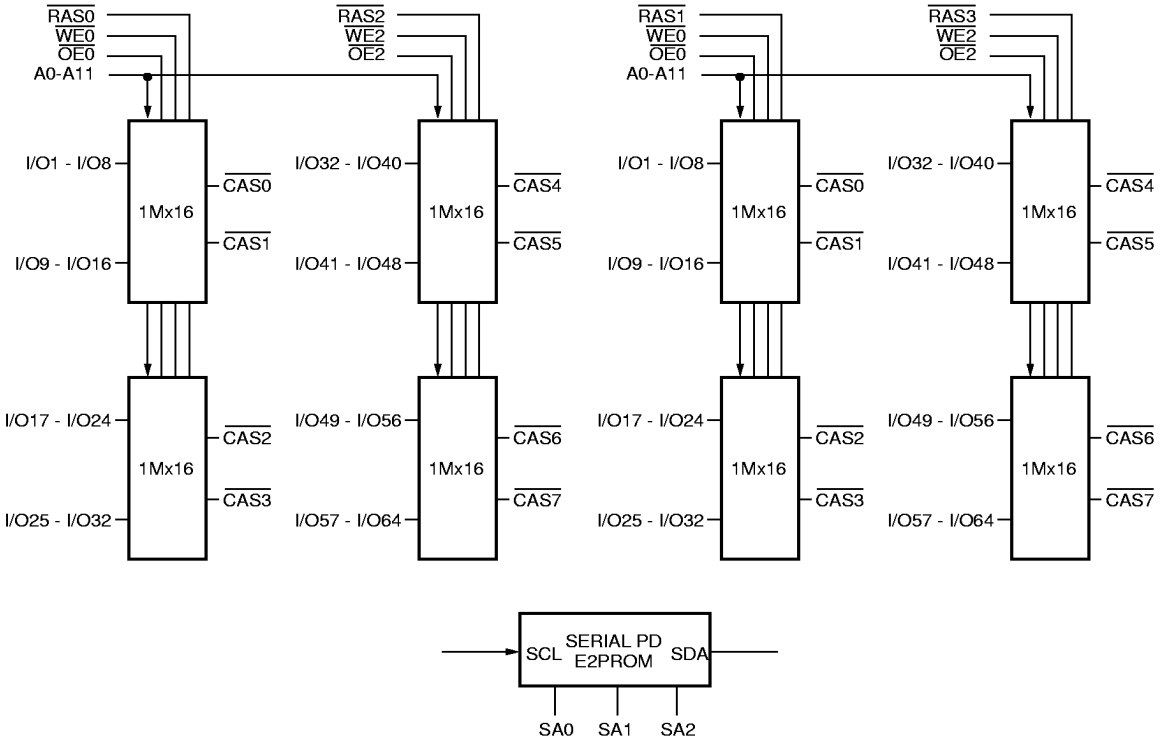
Serial Presence Detect Information

- SPD Interface Protocol: IIC
- Current sink capability of SDA driver ≤ 3mA
- Maximum Clock Frequency: 100 KHz

Byte Number	Function Described		SPD Entry Value	Hex 4K Refresh 50/60ns EDO
0	Number of SPD bytes		15	0F
1	Total bytes in serial PD		256	08
2	Memory type		EDO	02
3	Number of ROW addresses		12	0C
4	Number of COLUMN addresses		8	08
5	Number of Banks		2	02
6	Module Data Width		64	40
7	Module Data Width (continued)		0	00
8	Module Interface Levels		LVTTL	01
9	RAS Access Time	50 ns	50	32
		60 ns	60	3C
10	CAS Access Time	50 ns	13	0D
		60 ns	15	0F
11	DIMM Config (Error Det./Corr.)		none	00
12	Refresh Rate/Type		Normal/SF(15.6µs)-00	00
13	DRAM width, Primary		X16	10
14	Error Checking DRAM Data Width		UND	00
15-31	Reservered for Future Offerings			00h
32	Superset Memory Type (may be used in future)			00h
33–62	Superset Memory Specific Feature (may be used in future)			00h
63	Checksum for bytes 0–62			3Dh
64	Manufacturers JEDEC ID Code per JEP-106E		Continuation Code	7Fh
65			MVI	40h
66–71				00h
72	Manufacturing Location			
73	Manufacturer's Part Number	V	V33642R05KG	56h
74		3		33h
75		3		33h
76		6		36h
77		4		34h
78		2		32h
79		R		52h
80		0		30h

Byte Number	Function Described	SPD Entry Value	Hex 4K Refresh 50/60ns EDO
81	5		35h
82	K		4Bh
83	G		47h
84			20h
85			20h
86			20h
87			20h
88			20h
89			20h
90			20h
91–92	Revision Code	Rev0	00h
93	Date Code	WW	00h
94	Year	YY	62h (98)
95–98	Assembly Serial Number	Binary Incremental	00h
99–125	Manufactureer Specific Data‘	n/a	00h
126–127	Rserved		00h
128–255	Oper User Free-Form arean $ not defined		00h

Functional Block Diagram



Truth Table

FUNCTION		RAS	CAS	WE	OE	ROW ADDR	COL ADDR	I/O1-I/O4
Standby		H	X	X	X	X	X	High Impedance
Read		L	L	H	L	ROW	COL	Data Out
Early-Write		L	L	L	X	ROW	COL	Data In
Late-Write		L	L	H - L	H	ROW	COL	Data In
Read-Modify-Write (RMW)		L	L	H - L	L - H	ROW	COL	Data Out, Data In
EDO Page Mode Read	1st Cycle	L	H - L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H - L	H	L	n/a	COL	Data Out
EDO Page Mode Write	1st Cycle	L	H - L	L	X	ROW	COL	Data In
	2nd Cycle	L	H - L	L	X	n/a	COL	Data In
EDO Page Mode RMW	1st Cycle	L	H - L	H - L	L - H	ROW	COL	Data Out, Data In
	2st Cycle	L	H - L	H - L	L - H	n/a	COL	Data Out, Data In
$\overline{RAS}$ only refresh		L	H	X	X	ROW	n/a	High Impedance
$\overline{CAS}$-before-$\overline{RAS}$ refresh		H - L	L	H	X	X	n/a	High Impedance
Hidden Refresh	READ	L-H-L	L	H	L	ROW	COL	Data Out
	WRITE	L-H-L	L	L	X	ROW	COL	Data In
Self Refresh		H - L	L	H	X	X	X	High Impedance

Absolute Maximum Ratings*

Parameter	Commercial	Units
Operating Temperature Range	0 to 70	°C
Storage Temperature	-55 to +150	°C
Input/Output Voltage	-0.5 to min (V_{CC}+0.5, 4.6)	V
Power Supply Voltage	-1.0 to +4.6	V
Power Dissipation	9.95	W
Data Out Current (short circuit)	50	mA

***Note:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance*

T_A = 0 to 70°C, V_{CC} = 3.3 V ±10%, f = 1 MHz

Symbol	Parameter	Min.	Max.	Unit
C_{I1}	Input Capacitance (A0 to A11)	—	100	pF
C_{I2}	Input Capacitance ($\overline{RAS0}$–$\overline{RAS3}$)	—	75	pF
C_{I3}	Input Capacitance ($\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$)	—	18	pF
C_{IO1}	I/O Capacitance (I/O1-I/O64)	—	75	pF
C_S	Input Capacitance (SCL, SA0-2)	—	8	pF
C_S	Input/Output Capacitance (SDA)	—	10	pF

***Note:** Capacitance is sampled and not 100% tested.

DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC} = 3.3 V ±10%, V_{SS} = 0 V, t_T = 2ns, unless otherwise specified.

Symbol	Parameter	Access Time	Commercial		Unit	Test Conditions	Notes
			Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–10	10	µA	$V_{SS} \le V_{IN} \le V_{CC}$ + 0.5V	1
I_{LO}	Output Leakage Current (for High-Z State)		–10	10	µA	$V_{SS} \le V_{OUT} \le V_{CC}$+ 0.5V $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	1
I_{CC1}	V_{CC} Supply Current, Operating	50		800	mA	$t_{RC} = t_{RC}$ (min.)	2, 3, 4
		60		720			
I_{CC2}	V_{CC} Supply Current, TTL Standby			8	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-Only Refresh	50		800	mA	$t_{RC} = t_{RC}$ (min.)	2, 4
		60		720			
I_{CC4}	V_{CC} Supply Current, EDO Page Mode Operation	50		360	mA	Minimum Cycle	2, 3, 4
		60		300			
I_{CC5}	V_{CC} Supply Current, during $\overline{CAS}$-before-$\overline{RAS}$ Refresh	50		800	mA	$t_{RC} = t_{RC}$ (min.)	2, 4
		60		720			
I_{CC6}	V_{CC} Supply Current, CMOS Standby			4	mA	$\overline{RAS} \ge V_{CC} - 0.2$ V, $\overline{CAS} \ge V_{CC} - 0.2$ V other input ≥ V_{SS}	1
V_{CC}	Power Supply Voltage		4.5	5.5	V		
V_{IL}	Input Low Voltage		–0.5	0.8	V		1
V_{IH}	Input High Voltage		2.4	V_{CC}+0.5	V		1
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	1
V_{OH}	Output High Voltage		2.4		V	I_{OH} = –5.0 mA	1

AC Characteristics[5,6]

T_A = 0°C to 70°C, V_{CC} = 3.3 V ±10%, t_T = 2ns, unless otherwise noted

#	Symbol	Parameter	Limit Values				Unit	Note
			-50		-60			
			Min.	Max.	Min.	Max.		
Common Parameters								
1	t_{RC}	Random read or write cycle time	84	—	104	—	ns	
2	t_{RP}	$\overline{RAS}$ precharge time	30	—	40	—	ns	
3	t_{RAS}	$\overline{RAS}$ pulse width	50	10k	60	10k	ns	
4	t_{CAS}	$\overline{CAS}$ pulse width	8	10k	10	10k	ns	
5	t_{ASR}	Row address setup time	0	—	0	—	ns	
6	t_{RAH}	Row address hold time	8	—	10	—	ns	
7	t_{ASC}	Column address setup time	0	—	0	—	ns	
8	t_{CAH}	Column address hold time	8	—	10	—	ns	
9	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	12	37	14	45	ns	
10	t_{RAD}	$\overline{RAS}$ to column address delay	10	25	12	30	ns	
11	t_{RSH}	$\overline{RAS}$ hold time	13	—	15	—	ns	
12	t_{CSH}	$\overline{CAS}$ hold time	40	—	50	—	ns	
13	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	—	5	—	ns	
14	t_T	Transition time (rise and fall)	1	50	1	50	ns	7
15	t_{REF}	Refresh period	—	16	—	16	ms	
Read Cycle								
16	t_{RAC}	Access time from $\overline{RAS}$	—	50	—	60	ns	8, 9
17	t_{CAC}	Access time from $\overline{CAS}$	—	13	—	15	ns	8, 9
18	t_{CAA}	Access time from column address	—	25	—	30	ns	8,10
19	t_{OAC}	$\overline{OE}$ access time	—	13	—	15	ns	
20	t_{CAR}	Column address to $\overline{RAS}$ lead time	25	—	30	—	ns	
21	t_{RCS}	Read command setup time	0	—	0	—	ns	
22	t_{RCH}	Read command hold time	0	—	0	—	ns	11
23	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	0	—	0	—	ns	11
24	t_{CLZ}	$\overline{CAS}$ to output in low-Z	0	—	0	—	ns	8
25	t_{OFF}	Output buffer turn-off delay	0	13	0	15	ns	12
26	t_{OEZ}	Output turn-off delay from $\overline{OE}$	0	13	0	15	ns	12
27	t_{DZC}	Data to $\overline{CAS}$ low delay	0	—	0	—	ns	13
28	t_{DZO}	Data to $\overline{OE}$ low delay	0	—	0	—	ns	13
29	t_{CDD}	$\overline{CAS}$ high to data delay	10	—	13	—	ns	14
30	t_{ODD}	$\overline{OE}$ high to data delay	10	—	13	—	ns	14

#	Symbol	Parameter	Limit Values				Unit	Note
			-50		-60			
			Min.	Max.	Min.	Max.		
Write Cycle								
31	t_{WCH}	Write command hold time	8	–	10	–	ns	
32	t_{WP}	Write command pulse width	8	–	10	–	ns	
33	t_{WCS}	Write command setup time	0	–	0	–	ns	15
34	t_{RWL}	Write command to $\overline{RAS}$ lead time	8	–	10	–	ns	
35	t_{CWL}	Write command to $\overline{CAS}$ lead time	8	–	10	–	ns	
36	t_{DS}	Data setup time	0	–	0	–	ns	16
37	t_{DH}	Data hold time	8	–	10	–	ns	16
Read-modify-Write Cycle								
38	t_{RWC}	Read-write cycle time	113	–	138	–	ns	
39	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ delay time	64	–	77	–	ns	15
40	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay time	27	–	32	–	ns	15
41	t_{AWD}	Column address to $\overline{WE}$ delay time	39	–	47	–	ns	15
42	t_{OEH}	$\overline{OE}$ command hold time	10	–	13	–	ns	
EDO Page Mode Cycle								
43	t_{HPC}	EDO page mode cycle time	20	–	25	–	ns	
44	t_{CP}	$\overline{CAS}$ precharge time	8	–	10	–	ns	
45	t_{CPA}	Access time from $\overline{CAS}$ precharge	–	27	–	32	ns	7
46	t_{COH}	Output data hold time	5	–	5	–	ns	
47	t_{RASP}	$\overline{RAS}$ pulse width in EDO page mode	50	200k	60	200k	ns	
48	t_{RHPC}	$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	27	–	32	–	ns	
49	t_{OES}	$\overline{OE}$ setup time prior to CAS	5	–	5	–	ns	
EDO Page Mode Read-Modify-Write Cycle								
50	t_{PRWC}	EDO page mode read-write cycle time	58	–	68	–	ns	
51	t_{CPWD}	$\overline{CAS}$ precharge to $\overline{WE}$	41	–	49	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle								
52	t_{CSR}	$\overline{CAS}$ setup time	10	–	10	–	ns	
53	t_{CHR}	$\overline{CAS}$ hold time	10	–	10	–	ns	
54	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	5	–	5	–	ns	
55	t_{WRP}	Write to $\overline{RAS}$ precharge time	10	–	10	–	ns	
56	t_{WRH}	Write hold time referenced to $\overline{RAS}$	10	–	10	–	ns	

Notes:

1. All voltage are referenced to V_{SS}.
2. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on cycle rate.
3. I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4} it can be changed once or less during an EDO page mode cycle.
5. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 2ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
8. Measured with the specified current load and 100pF at V_{OL} = 0.8 V and V_{OH} = 2.0 V. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CAA}, t_{CPA}, t_{OAC}, t_{CAC} is measured from tristate.
9. Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
10. Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{CAA}.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. $t_{OFF\ (max.)}$, $t_{OEZ\ (max.)}$ define the time at which the outputs acheive the open-circuit condition and are not referenced to output voltage levels. t_{OFF} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.
13. Either t_{DZC} or t_{DZO} must be satisfied.
14. Either t_{CDD} or t_{ODD} must be satisfied.
15. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, and $t_{AWD} > t_{AWD}$ (min.), the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
16. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

Package Diagrams

168 Pin DIMM

Units in Inches [Millimeters]