VITELIC

V53C864 FAMILY HIGH PERFORMANCE, LOW POWER 64K X 8 BIT FAST PAGE MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE V53C864	70/70L	80/80L	10/10L	12/12L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	70 ns	80 ns	100 ns	120 ns
Max. Column Address Access Time, (t_{CAA})	35 ns	40 ns	45 ns	55 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	50 ns	55 ns	65 ns	75 ns
Min. Read/Write Cycle Time, (t_{RC})	130 ns	145 ns	175 ns	205 ns

LOW POWER V53C864L	70L	80L	10L	12L
Max. CMOS Standby Current, (I_{DD6})	1.0 mA	1.0 mA	1.0 mA	1.0 mA

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Features

- Low power dissipation for V53C864-12
  - Operating Current—60 mA max.
  - TTL Standby Current—3.5 mA max.
- Low CMOS Standby Current
  - V53C864—3.0 mA max.
  - V53C864L—1.0 mA max.
- Read-Modify-Write, $\overline{RAS}$-only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Fast Page Mode operation for a sustained data rate greater than 20 MHz
- 256 Refresh cycles/4 ms
- Standard packages are 24 pin Plastic DIP and 26/24 pin SOJ.

Description

The Vitelic V53C864 is a high-speed 65,536 x 8 bit CMOS dynamic random access memory. Fabricated with Vitelic's VICMOS III technology, the V53C864 offers a combination of size and features unattainable with NMOS technology: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh to 32 ms for lower power or portable applications.

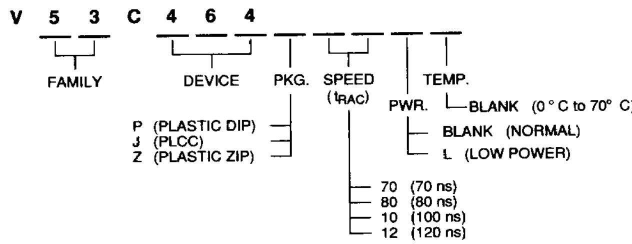
All inputs and outputs are TTL-compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 256 (x8) bits within a row with cycle times as short as 50 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C864 ideally suited for graphics, digital signal processing and high performance computing systems.

The V53C864L (-12) offers a maximum data retention power of 5.5 mW when operating in CMOS standby mode and performing $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. For selected V53C864L devices with Refresh Interval longer than 4 ms, consult the factory.

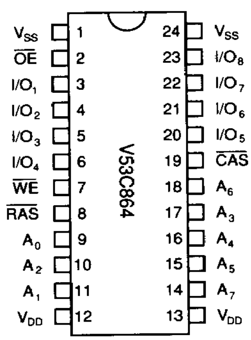
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)				Power		Temperature Mark
	P	K	70	80	100	120	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	•	Blank

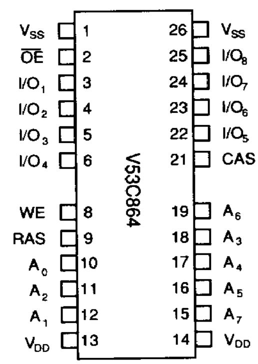
Description	Pkg.	Pin Count
Plastic DIP	P	24
SOJ	K	26/24



24 Lead Plastic DIP PIN CONFIGURATION
Top View



26/24 Lead SOJ PIN CONFIGURATION
Top View



Absolute Maximum Ratings*

Ambient Temperature
Under Bias .... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} .... –1.0 V to +7.0 V
Voltage on V_{DD} relative to V_{SS} .... –1.0 V to +7.0 V
Data Out Current .... 50 mA
Power Dissipation .... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

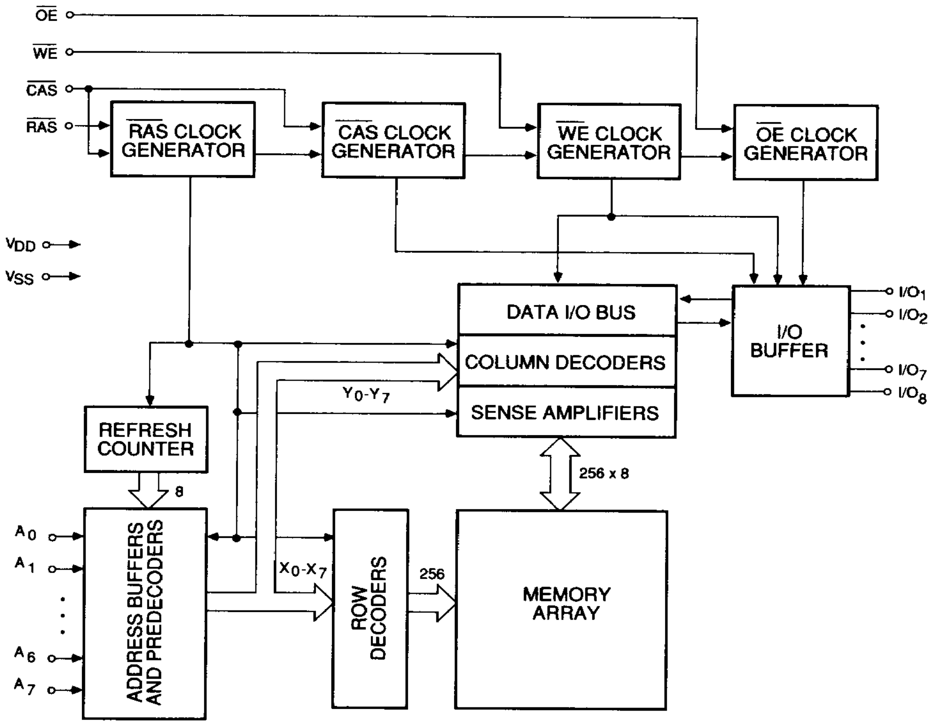
$T_A = 25°C, V_{DD} = 5\ V \pm 10\%, V_{SS} = 0\ V$

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	4	5	pF
C_{OUT}	I/O	5	7	pF

*Note: Capacitance is sampled and not 100% tested

Block Diagram

64K x 8 DRAM



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DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C864 Min.	V53C864 Typ.	V53C864 Max.	V53C864L Min.	V53C864L Typ.	V53C864L Max.	Unit	Test Conditions	Notes
I_{LI}	Input Leakage Current (any input pin)		–10		10	–10		10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		–10		10	–10		10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$,$\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	70			85			85	mA	$t_{RC} = t_{RC}$ (min.)	1,2
		80			75			75			
		100			65			65			
		120			60			60			
I_{DD2}	V_{DD} Supply Current, TTL Standby				3.5			2.0	mA	$\overline{RAS}$,$\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	70			85			85	mA	$t_{RC} = t_{RC}$ (min.)	2
		80			75			75			
		100			65			65			
		120			60			60			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	70			60			60	mA	Minimum Cycle	1,2
		80			55			55			
		100			50			50			
		120			45			45			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled				4			2.5	mA	$\overline{RAS}=V_{IH}$,$\overline{CAS}=V_{IL}$ other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby				3			1.0	mA	$\overline{RAS} \ge V_{DD}$ –0.2 V, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
V_{IL}	Input Low Voltage		–1		0.8	–1		0.8	V		3
V_{IH}	Input High Voltage		2.4		V_{DD} +1	2.4		V_{DD} +1	V		3
V_{OL}	Output Low Voltage				0.4			0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4			2.4			V	I_{OH} = –5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted
AC Test conditions, input pulse levels 0 to 3 V

#	JEDEC Symbol	Symbol	Parameter	70/L		80/L		10/L		12/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	70	75K	80	75K	100	75K	120	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	130		145		175		205		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{\text{RAS}}$ Precharge Time	50		55		65		75		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{\text{CAS}}$ Hold Time	70		80		100		120		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	25		30		35		40		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	25	45	25	50	25	65	30	80	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		15		15		20		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		20		25		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{\text{RAS}}$ Hold Time (Read Cycle)	25		30		35		40	ns		
13	t_{CH2RL2}	t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	15		15		15		20		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	5		5		5		5		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	5		5		5		5		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{OE}}$	0		0		0		0		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{\text{OE}}$		15		20		25		30	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{\text{CAS}}$		25		30		35		40	ns	6,7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{\text{RAS}}$		70		80		100		120	ns	6,8,9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		35		40		45		55	ns	6,7,10

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AC Characteristics *(Cont'd.)*

#	JEDEC Symbol	Symbol	Parameter	70/L		80/L		10/L		12/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CL1QX}	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		0		ns	16
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	15	0	20	0	25	0	30	ns	16
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55		60		70		80		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	35	20	40	20	55	25	65	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH (W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	25		30		35		40		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25		30		35		40		ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	12,13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		15		20		25		ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		15		20		25		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55		60		70		80		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25		30		35		40		ns	
32	t_{DVWL2}	t_{DS}	Data In Setup Time	0		0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data In Hold Time	15		15		20		25		ns	14
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	20		20		25		30		ns	
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	20		25		30		35		ns	
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	185		210		250		290		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	125		145		175		205		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	50		60		70		80		ns	12

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	70/L		80/L		10/L		12/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	95		110		135		160		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	80		95		110		125		ns	
41	t_{AVWL2}	t_{AWD}	Col. Address to $\overline{WE}$ Delay	60		70		80		85		ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	50		55		65		75		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	15		15		20		25		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	35		40		45		55		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		45		50		55		65	ns	6,7
46	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	55		60		70		80		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		10		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	20		25		30		40		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	80		90		100		115		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	15
		t_{RI}	Refresh Interval (256 Cycles)		4		4		4		4	ms	17

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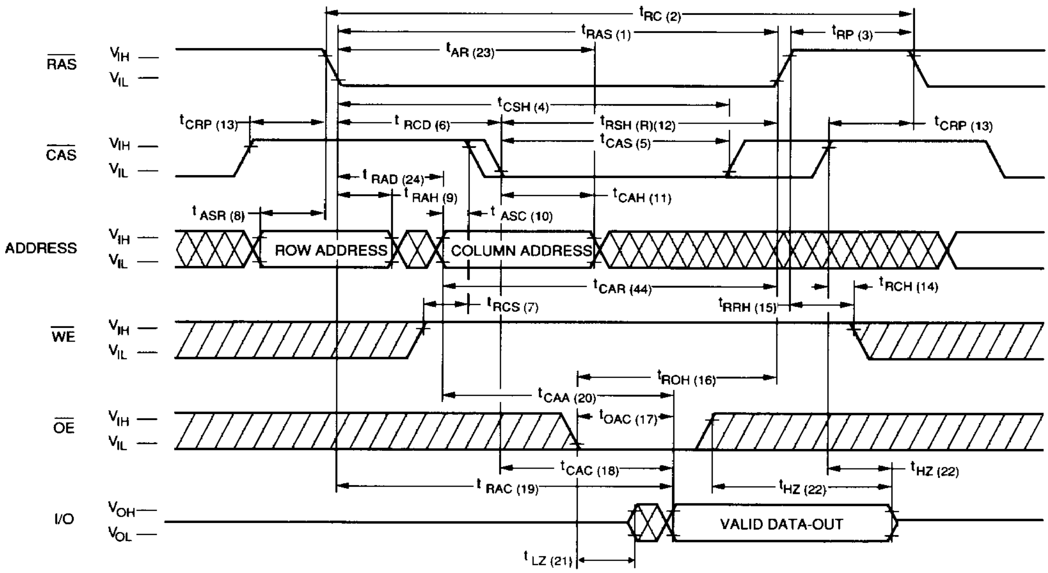
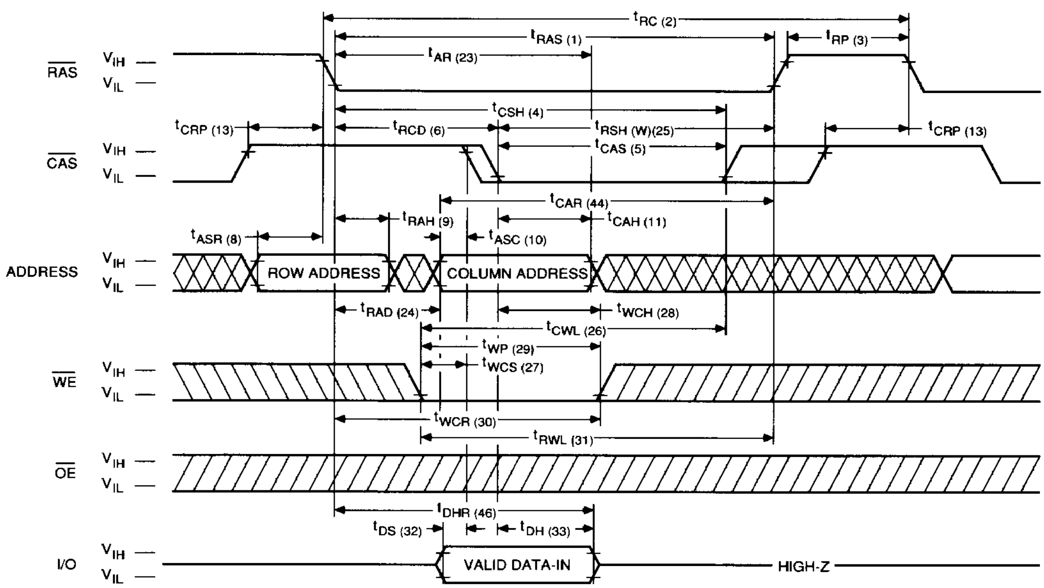
Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to −1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC measurements assume t_T = 5 ns.
16. Assumes a three-state test load (5pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

Waveforms of Read Cycle



Waveforms of Early Write Cycle



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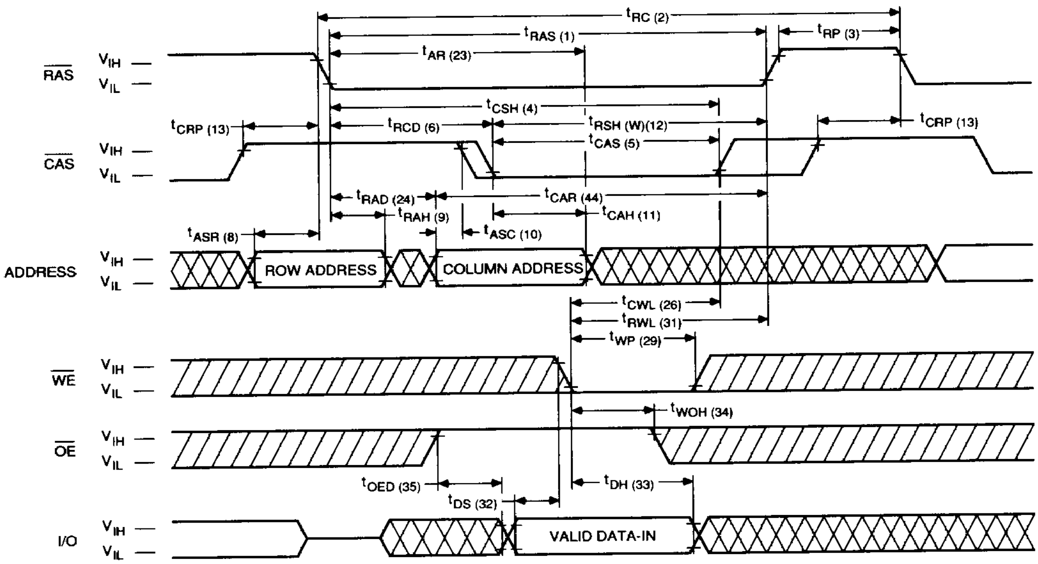
Waveforms of $\overline{OE}$-Controlled Write Cycle



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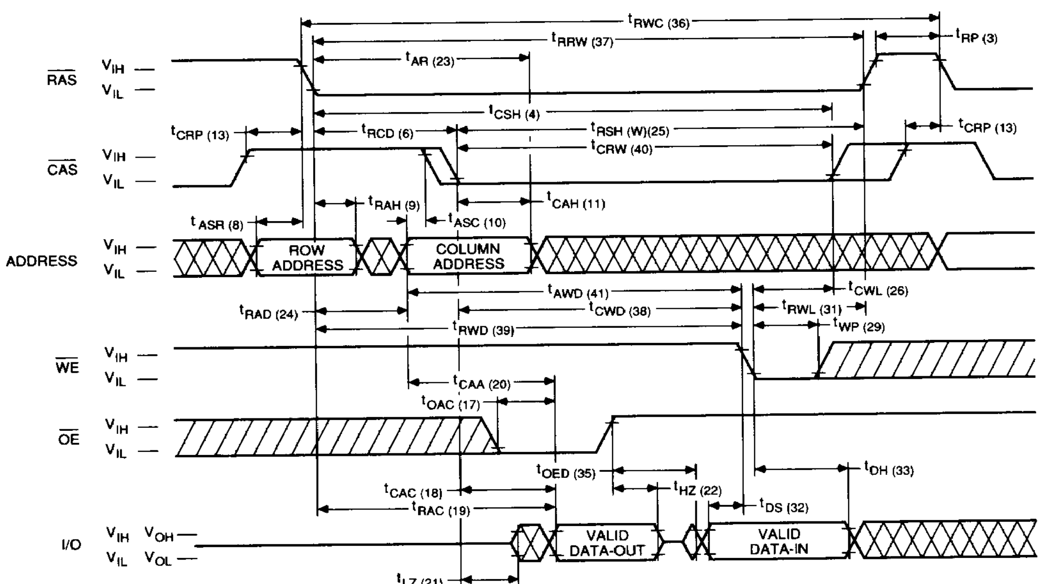
Waveforms of Read-Modify-Write Cycle



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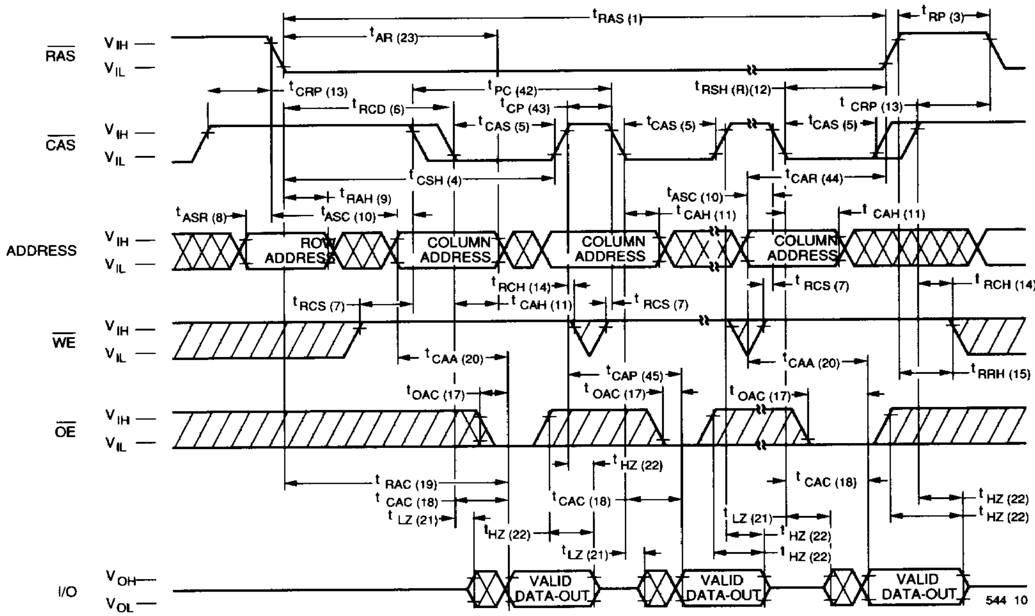
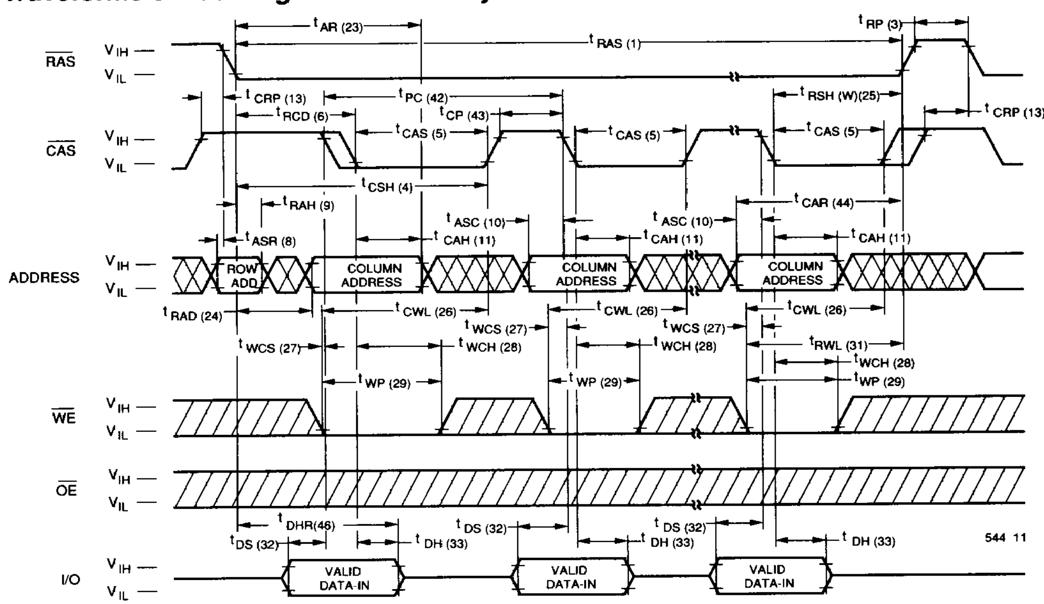
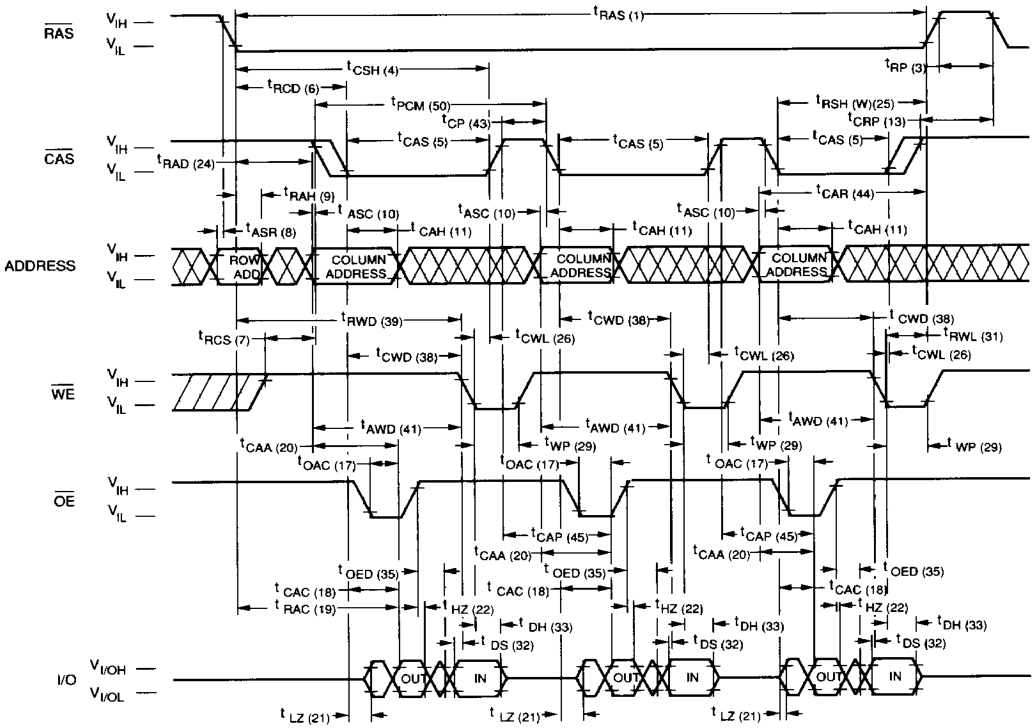
Waveforms of Fast Page Mode Read Cycle



Waveforms of Fast Page Mode Write Cycle



Waveforms of Fast Page Mode Read/Write Cycle



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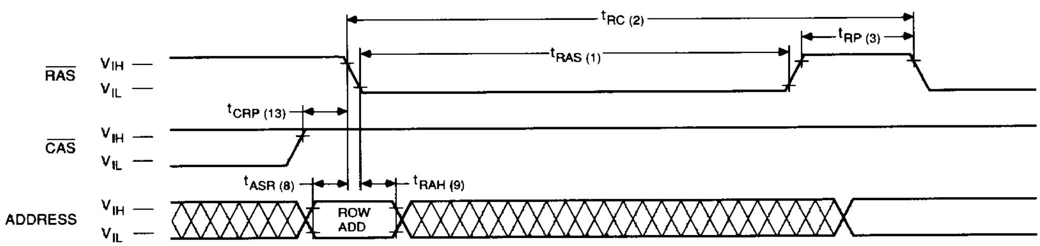
Waveforms of $\overline{RAS}$-Only Refresh Cycle



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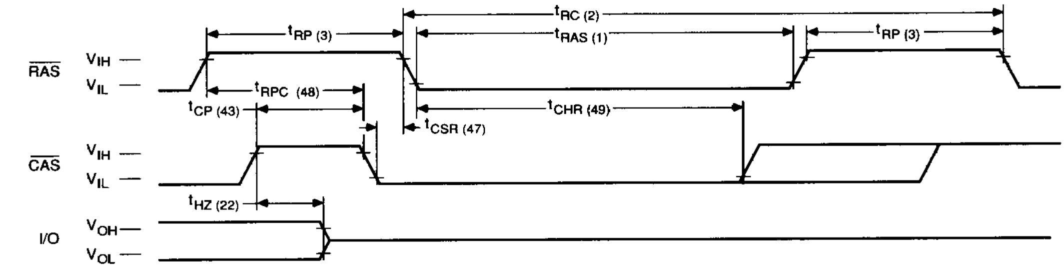
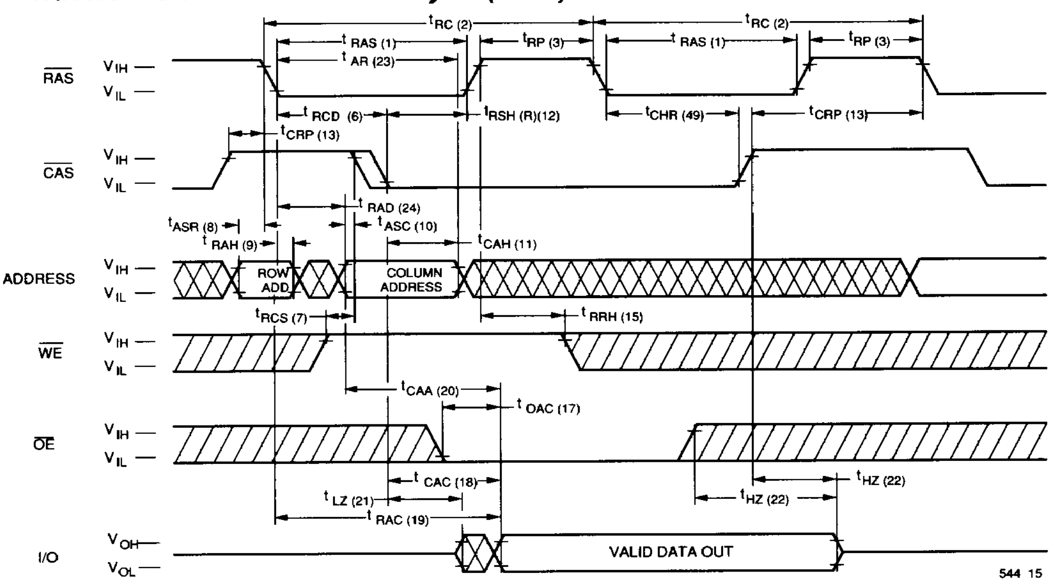
NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



NOTE: $\overline{WE}$, $\overline{OE}$, A_0–A_7 = Don't care

Waveforms of Hidden Refresh Cycle (Read)



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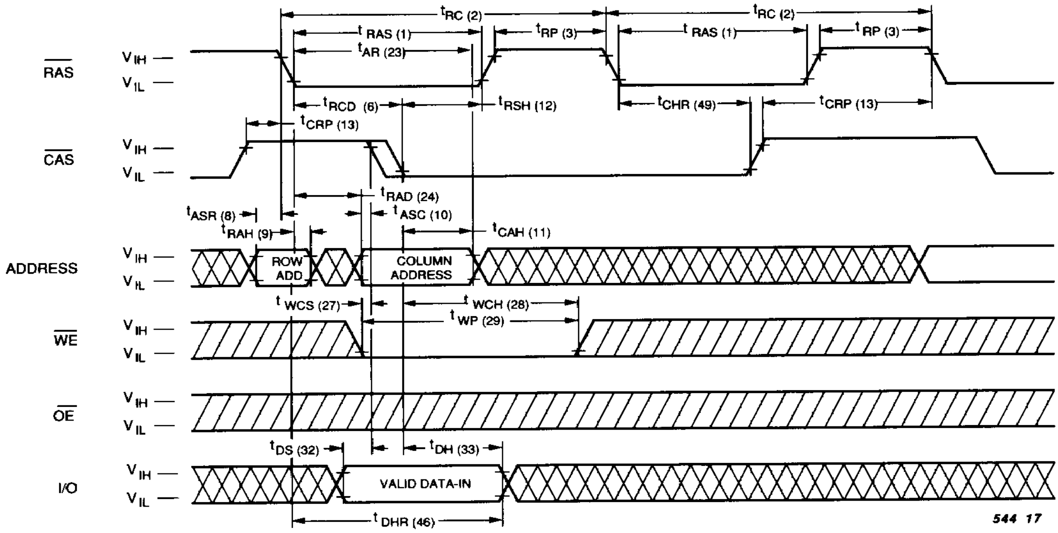
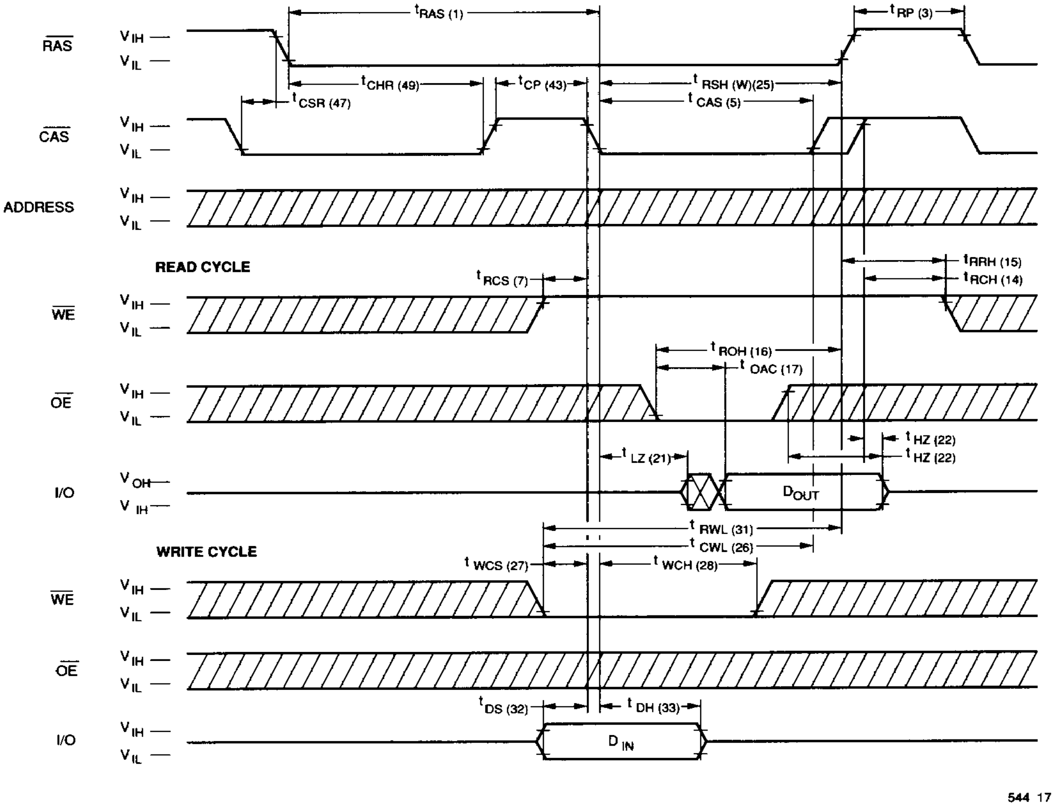
Waveforms of Hidden Refresh Cycle (Write)



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



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Functional Description

The V53C864 is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C864 reads and writes data by multiplexing a 16-bit address into an 8-bit row and an 8-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$-controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 256 Refresh Cycles are required in each 4 ms period. There are two ways to refresh the memory:

1. By selectint each of the 256 row addresses determined by A_0 through A_7 at least once every 4 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ is low during the falling edge of $\overline{RAS}$, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C864 uses the output of an internal 8-bit counter as the source of row addresses and ignores external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode, and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V53C864 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C864 power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 256

Fast Page Mode Operation

Fast Page Mode operation permits all 256 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining RAS low while performing succesive CAS cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while CAS is high. Thus, access begins from the occurence of a valid column address rather than from the falling edge of CAS, eliminating t_{ASC} and t_T from the critical timing path. CAS latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA}- or t_{CAP}-controlled. If the column address is valid prior to the rising edge of CAS, the access time is referenced to the CAS rising edge and is specified by t_{CAP}. If the column address is valid after the rising CAS edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of CAS latches the address and enables the output.

Fast Page Mode provides a sustained data rate of over 19 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{256}{t_{RC} + 255 \times t_{PC}}$$

Data Output Operation

The V53C864 Input/Output is controlled by OE, CAS, WE and RAS. A RAS low transition enables the transfer of data to and from the selected row address in the Memory Array. A RAS high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a RAS low transition, a CAS low transition or CAS low level enables the internal I/O path. A CAS high transition or a CAS high level disables the I/O path and the output driver if it is enabled. A CAS low transition while RAS is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding OE high. The OE signal has no effect on any data stored in the output latches. A WE low level can also disable the output drivers when CAS is low. During a Write cycle, if WE goes low at a time in relationship to CAS that would normally cause the outputs to be active, it is necessary to use OE to disable the output drivers prior to the WE low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a RAS clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the V_{DD} current requirement of the V53C864 is dependent on the input levels of RAS and CAS. If RAS is low during Power-On, the device will go into an active cycle, and I_{DD} will exhibit current transients. It is recommended that RAS and CAS track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. Vitelic V53C864 Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
CAS-Controlled Write Cycle (Early Write)	High–Z
WE-Controlled Write Cycle (Late Write)	OE-Controlled. High OE = High–Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
RAS-only Refresh	High-Z
CAS-before-RAS Refresh Cycle	Data remains as in previous cycle
CAS-only Cycles	High-Z