



512MB- 64Mx72 SDRAM, UNBUFFERED W/PLL

FEATURES

- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V $\pm$ 0.3V Power Supply
- 144 Pin SO-DIMM JEDEC

DESCRIPTION

The WED3DG7265V is a 64Mx72 synchronous DRAM module which consists of nine 64Mx8 DDR SDRAM components in TSOP II package, and one 2Kb EEPROM in an 8 pin TSSOP package for Serial Presence Detect which are mounted on a 144 pin SO-DIMM multilayer FR4 Substrate.

*This product is subject to change without notice.

PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

PINOUT											
PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	V _{SS}	2	V _{SS}	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	V _{CC}	102	V _{CC}
7	DQ2	8	DQ34	55	V _{SS}	56	V _{SS}	103	A6	104	A7
9	DQ3	10	DQ35	57	CB0	58	CB4	105	A8	106	BA0
11	V _{CC}	12	V _{CC}	59	CB1	60	CB5	107	V _{SS}	108	V _{SS}
13	DQ4	14	DQ36	61	CLK0	62	CKE0	109	A9	110	BA1
15	DQ5	16	DQ37	63	V _{CC}	64	V _{CC}	111	A10	112	A11
17	DQ6	18	DQ38	65	RAS#	66	CAS#	113	V _{CC}	114	V _{CC}
19	DQ7	20	DQ39	67	WE#	68	NC	115	DQMB2	116	DQMB6
21	V _{SS}	22	V _{SS}	69	SO#	70	NC	117	DQMB3	118	DQMB7
23	DQMB0	24	DQMB4	71	NC	72	NC	119	V _{SS}	120	V _{SS}
25	DQMB1	26	DQMB5	73	NC	74	CLK1	121	DQ24	122	DQ56
27	V _{CC}	28	V _{CC}	75	V _{SS}	76	V _{SS}	123	DQ25	124	DQ57
29	A0	30	A3	77	CB2	78	CB6	125	DQ26	126	DQ58
31	A1	32	A4	79	CB3	80	CB7	127	DQ27	128	DQ59
33	A2	34	A5	81	V _{CC}	82	V _{CC}	129	V _{CC}	130	V _{CC}
35	V _{SS}	36	V _{SS}	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	V _{SS}	92	V _{SS}	139	V _{SS}	140	V _{SS}
45	V _{CC}	q46	V _{CC}	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	V _{CC}	144	V _{CC}

PIN NAMES

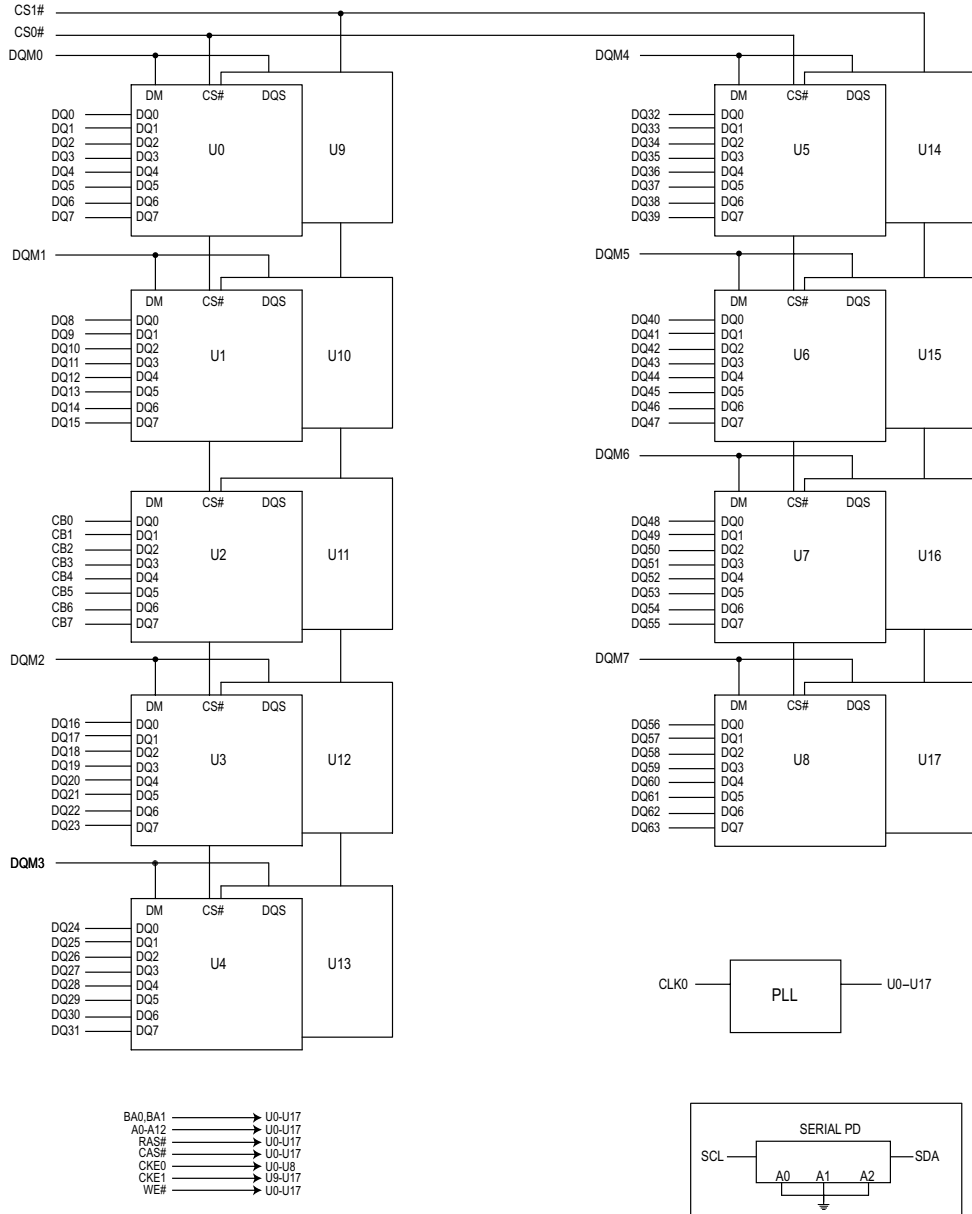
A0 – A12	Address Input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CLK0	Clock Input
CB0-7	Check Bit (Data-In/Data-Out)
CKE0, CKE1	Clock Enable Input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-7	DQM
V _{CC}	Power Supply (3.3V)
V _{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock
DNU	Do Not Use
NC	No Connect

* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.



FUNCTIONAL BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC} , V _{CCQ}	-1.0 ~ 4.6	V
Storage Temperature	T _{STG}	-55 ~ +150	°C
Power Dissipation	P _D	9	W
Short Circuit Current	I _{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage Referenced to: V_{SS} = 0V, T_A ≤ 0°C ≤ +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V _{CC}	3.0	3.3	3.6	V	
Input High Voltage	V _{IH}	2.0	3.0	V _{CCQ} +0.3	V	1
Input Low Voltage	V _{IL}	-0.3	—	0.8	V	2
Output High Voltage	V _{OH}	2.4	—	—	V	I _{OH} = -2mA
Output Low Voltage	V _{OL}	—	—	0.4	V	I _{OL} = -2mA
Input Leakage Current	I _{LI}	-10	—	10	μA	3

Note: 1. V_{IH} (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V_{IL} (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V_{IN} ≤ V_{CCQ}

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

(T_A = 23°C, f = 1MHz, V_{CC} = 3.3V, V_{REF}=1.4V 6200mV)

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C _{IN1}	15	pF
Input Capacitance (RAS#,CAS#,WE#)	C _{IN2}	15	pF
Input Capacitance (CKE0)	C _{IN3}	15	pF
Input Capacitance (CLK0)	C _{IN4}	20	pF
Input Capacitance (CS0#)	C _{IN5}	15	pF
Input Capacitance (DQM0-DQM7)	C _{IN6}	15	pF
Input Capacitance (BA0-BA1)	C _{IN7}	15	pF
Data input/output capacitance (DQ0-DQ63)	C _{OUT}	22	pF
Data input/output capacitance (CB0-7)	C _{OUT1}	22	pF



OPERATING CURRENT CHARACTERISTICS

($V_{CC} = 3.3V$, $T_A = 0^{\circ}C \leq +70^{\circ}C$)

			Version			
Parameter	Symbol	Conditions	133	100	Units	Note
Operating Current (One bank active)	I _{CC1}	Burst Length = 1 t _{RC} ≥ t _{RC} (min) I _{OL} = 0mA	1,530	1,400	mA	1
Precharge Standby Current in Power Down Mode	I _{CC2P}	CKE ≤ V _{IL} (max), t _{CC} = 10ns	50		mA	
	I _{CC2PS}	CKE & CLK ≤ V _{IL} (max), t _{CC} = ∞	50			
Precharge Standby Current in Non-Power Down Mode	I _{CC2N}	CKE ≥ V _{IH} (min), CS ≥ V _{IH} (min), t _{CC} = 10ns Input signals are charged one time during 20	370		mA	
	I _{CC2NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), t _{CC} = ∞ Input signals are stable	200			
Active standby current in power-down mode	I _{CC3P}	CKE ≥ V _{IL} (max), t _{CC} = 10ns	80		mA	
	I _{CC3PS}	CKE & CLK ≤ V _{IL} (max), t _{CC} = ∞	80			
Active standby current in non power-down mode	I _{CC3N}	CKE ≥ V _{IH} (min), CS ≥ V _{IH} (min), t _{CC} = 10ns Input signals are changed one time during 20ns	550		mA	
	I _{CC3NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), t _{CC} = ∞ Input signals are stable	410		mA	
Operating current (Burst mode)	I _{CC4}	I _O = mA Page burst 4 Banks activated t _{CCD} = 2CLK	2,070	1,620	mA	1
Refresh current	I _{CC5}	t _{RC} ≥ t _{RC} (min)	3,150	2,880	mA	2
Self refresh current	I _{CC6}	CKE ≤ 0.2V	60		mA	

- Notes: 1. Measured with outputs open.
 2. Refresh period is 64ms.
 3. Unless otherwise noticed, input swing level is CMOS ($V_{IH}/V_{IL} = V_{CC}/V_{SSQ}$)



PACKAGE DIMENSIONS





<u>REV.</u>	<u>DATE</u>	<u>REQUESTED BY</u>	<u>DETAILS</u>
A	4-8-02	PAUL MARIEN	CREATED
B	5-6-02	PAUL MARIEN	MAKE CORRECTIONS TO THE PINOUT MAKE CORRECTIONS TO THE PACKAGE DRAWING CHANGE THE BLOCK DIAGRAM
0	9-11-02	PAUL MARIEN	CHANGE FROM ADVANCED TO FINAL