GATED J-K MASTER-SLAVE FLIP-FLOPS

GENERAL DESCRIPTION

The MMC 4095/4096 (intermediate or extended temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package.
The MMC 4095 and MMC 4096 are J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K inputs control tansfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and $\overline{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

FEATURES

- 16 MHz toggle rate (typ.) at $V_{DD} - V_{SS} = 10$ V
- Gated inputs.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

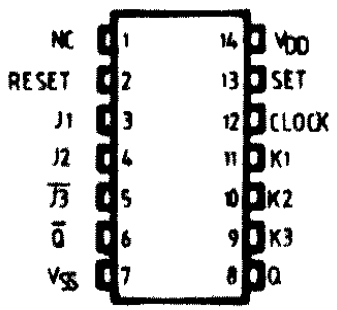
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

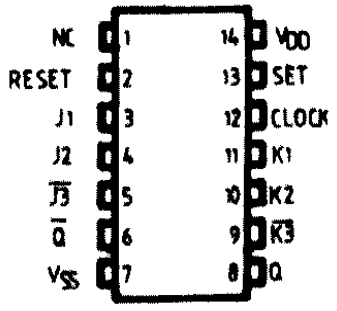
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM

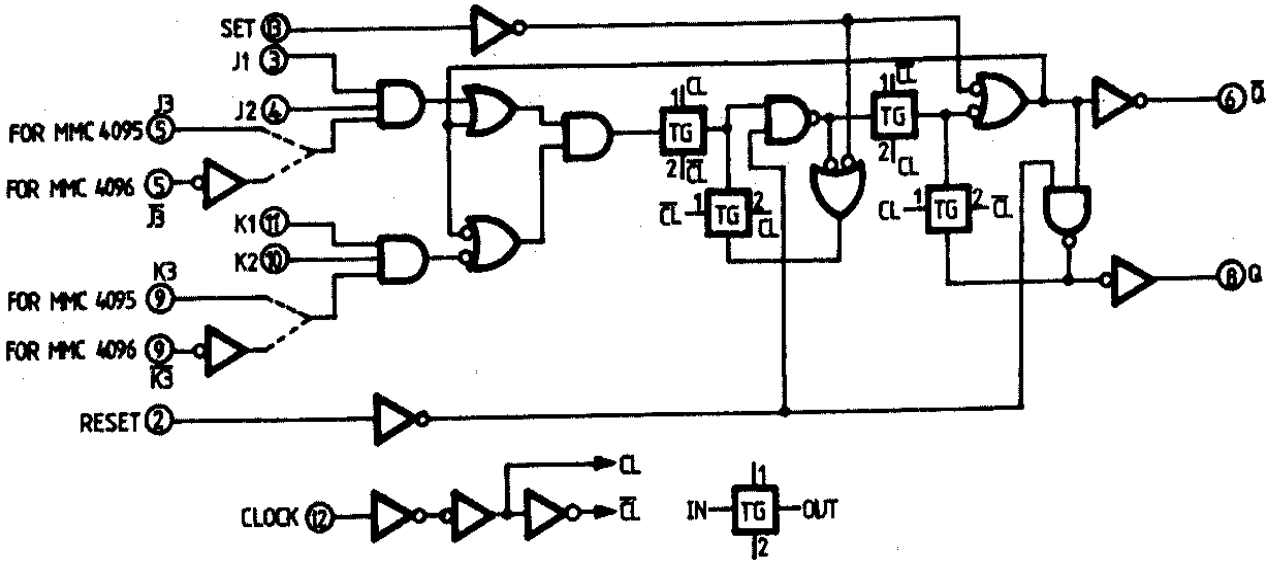
MMC 4095



MMC 4096



LOGIC DIAGRAM



TRUTH TABLES

SYNCHRONOUS OPERATION

(S = 0 R = 0)

Inputs before positive clock transition		Outputs after positive clock transition	
J*	K*	Q	$\overline{Q}$
0	0	No change	
0	1	0	1
1	0	1	0
1	1	Toggles	

* For MMC 4095
$J = J1 \cdot J2 \cdot J3$
$K = K1 \cdot K2 \cdot K3$

For MMC 4096
$J = J1 \cdot J2 \cdot \overline{J3}$
$K = K1 \cdot K2 \cdot \overline{K3}$

ASYNCHRONOUS OPERATION

(J and K — DON'T CARE)

S	R	Q	$\overline{Q}$
0	0	No change	
0	1	0	1
1	0	1	0
1	1	0	0

0 = V_{SS}, 1 = V_{DD}

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\lvert I_O \rvert$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		E, F types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	

PARAMETER			TEST CONDITIONS V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	VALUES 25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	UNIT
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	C, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$±10^{-5}$	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.
The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

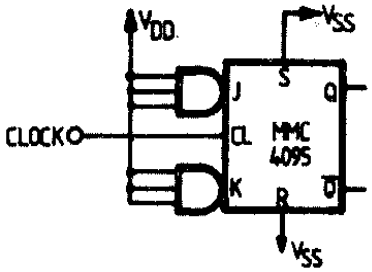
(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/ C all input rise and fall times = 20 ns).

PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min.	typ.	max.	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	5		250	500	ns
		10		100	200	
		15		75	150	
t_{PLH}, t_{PHL}	Propagation delay time (Set or reset)	5		150	300	ns
		10		75	150	
		15		50	100	

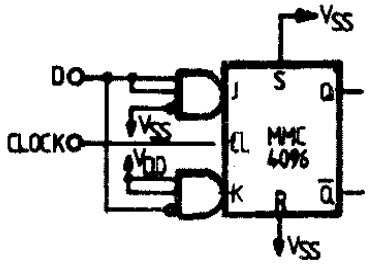
	PARAMETER	TEST CONDITIONS	VALUES			UNIT
		V_{DD} (V)	min.	typ.	max.	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL}	Maximum clock input frequency	5	3.5	7		MHz
		10	8	16		
		15	12	24		
t_W	Clock pulse width	5	140	70		ns
		10	60	30		
		15	40	20		
t_r, t_f	Clock input rise or fall time	5			15	μs
		10			5	
		15			5	
t_W	Set or reset pulse width	5	200	100		ns
		10	100	50		
		15	50	25		
t_{setup}	Data setup time	5	400	200		ns
		10	160	80		
		15	100	50		

TYPICAL APPLICATIONS

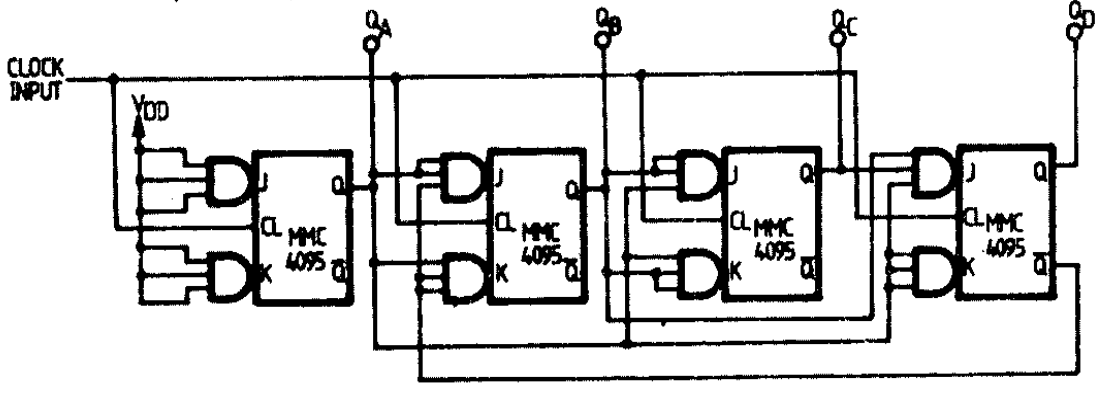
T-type flip-flop

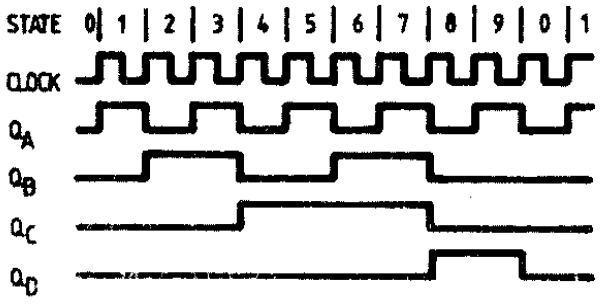


D-type flip-flop



Synchronous binary divide-by-ten counter



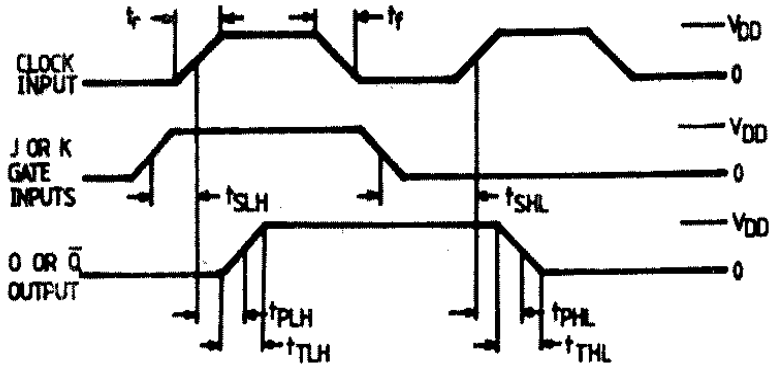


STATE	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

In all MMC 4095 units the Set and Reset are connected to V_{SS}

WAVEFORMS

Propagation delay, transition and setup-time



Clock pulse rise and fall time