

National Semiconductor DS92LX2121 / DS92LX2122

ADVANCE INFORMATION

June 1, 2010

10 - 50 MHz Channel Link III Serializer and Deserializer with **Embedded Bi-Directional Control Channel**

General Description

The DS92LX2121/DS92LX2122 chipset offers a Channel Link III interface to deliver clock, high-speed data and a lowspeed, bidirectional I2C control bus over a single twisted wire pair. This single serial stream simplifies transferring a wide data bus over PCB traces and cable by eliminating clock to data skew, while reducing cable width and connector size. The DS92LX2121/DS92LX2122 incorporates differential signaling on both the high-speed and bi-directional back channel control data paths.

The Serializer/ Deserializer pair is ideally suited for driving video data with up to 18-bit color depth (RGB666 + HS, VS, and DE) along with a bi-directional back channel control bus.

In addition, the Deserializer provides input equalization to compensate for loss from the media over longer distances. Internal DC balanced encoding/decoding is used to support AC-Coupled interconnects. Deserializer features such as output slew rate control, spread spectrum clock generation and staggered outputs can be enabled to lower EMI.

A sleep function provides a power-savings mode when the high speed forward channel and embedded bi-directional control channel are not needed.

The Serializer is offered in a 40-pin lead in LLP and Deserializer is offered in a 48-pin LLP packages.

Features

- Up to 1050 Mbits/sec data throughput
- 10 MHz to 50 MHz input clock support
- -Supports 18-bit color depth (RGB666 + HS, VS, DE)
- Embedded clock with DC Balanced coding to support ACcoupled interconnects
- Capable to drive up to 10 meters shielded twisted-pair
- Bi-directional control interface channel with I²C support
- I²C interface for device configuration. Single-pin ID addressing
- Up to 4 GPI on DES and GPO on SER .
- AT-SPEED BIST diagnosis feature to validate link integrity -
- . Individual power-down controls for both SER and DES
- User-selectable clock edge for parallel data on both SER and DES
- Integrated termination resistors
- -1.8V- or 3.3V-compatible parallel bus interface
- Single power supply at 1.8V
- IEC 61000-4-2 ESD compliant
- Temperature range -40°C to +85°C
- No reference clock required on Deserializer
- Programmable Receive Equalization
- LOCK output reporting pin to ensure
- EMI/EMC Mitigation
 - DES Programmable Spread Spectrum (SSCG) outputs
 - DES Receiver Output clock and data slew rate select
 - DES Receiver staggered outputs

Applications

- Industrial Displays, Touch Screens
- Medical Imaging

Typical Application Diagram



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DS92LX2121 / DS92LX2122



DS92LX2121 Serializer Pin Descriptions

| Pin Name | Number of Pins | I/O, Type | Description | | | |
|---------------------------|-------------------------------|-------------------------------|---|--|--|--|
| LVCMOS PARALLEL INTERFACE | | | | | | |
| DIN[20:0] | 21 | Inputs, LVCMOS w/ | Parallel data inputs. | | | |
| | | pull down | | | | |
| PCLK | 1 | Input, LVCMOS w/ | Pixel Clock Input Pin. Strobe edge set by TRFB configuration. | | | |
| | | pull down | | | | |
| GENERAL PUR | GENERAL PURPOSE OUTPUT (GPO) | | | | | |
| GPO[3:0] | 4 | Output, Digital | General-purpose pins individually configured as outputs; which are used to | | | |
| | | | control and respond to various commands. | | | |
| SERIAL CONTR | ROL BUS - I ² C CO | MPATIBLE | | | | |
| SCI | 1 | Input/Output, Open | Clock line for the serial control bus communication | | | |
| | | Drain | SCL requires an external pull-up resistor to V _{DDIO} . | | | |
| SDA | 1 | Input/Output, Open | Data line for the serial control bus communication | | | |
| | I | Drain | SDA requires an external pull-up resistor to V _{DDIO} . | | | |
| | | Input, LVCMOS w/ | I ² C Master / Slave select | | | |
| M/S | 1 | | M/S = L, Master (default)r; device generates and drives the SCL clock line | | | |
| | | | M/S = H, Slave; device accepts SCL clock input | | | |
| | 1 | Input, analog | Continuous Address Decoder | | | |
| CAD | | | Input pin to select the Slave Device Address. | | | |
| •••• | | | Input is connect to external resistor divider to programmable Device ID | | | |
| | | | address (see Serial Control Bus Connection). | | | |
| CONTROL AND | | N . | | | | |
| | | Input, LVCMOS w/ pull down | Power down Mode Input Pin. | | | |
| PDB | 1 | | PDB = H, I ransmitter is enabled and is ON. | | | |
| | | | PDB = L, Transmitter is in Sleep (Power Down). When the transmitter is in | | | |
| | | | Deserved This sin MUCT he field OW | | | |
| RES | 2 | | | | | |
| | | | | | | |
| | | Input/Output_CMI | Non invorting differential output, back channel input | | | |
| | 1 | | | | | |
| Bower and Grou | und | | | | | |
| | | | | | | |
| | | Power, Analog | PLL POWER, 1.8V ±5% | | | |
| | 1 | Power, Analog | I X Analog Power, 1.8V ±5% | | | |
| | | Power, Analog | LVDS & BC Dr Power, 1.8V ±5% | | | |
| | 1 | Power, Digital | Digital Power, 1.8V ±5% | | | |
| VDDIO | 1 | Power, Digital | Power for input stage, The single-ended inputs are powered from V _{DDIO} . | | | |
| VSS | - | Ground, DAP | All VSS pads are down bonded to DAP. DAP must be grounded. | | | |



DS92LX2122 Deserializer Pin Descriptions

| Prinkanie Vol. Type Description VCMOS PARALLEL INTERFACE Prizel Clock Output Pin. Prizel Clock Output Pin. PCLK 1 Output, LVCMOS Prizel Clock Output Pin. PCLK 1 Output, LVCMOS Strobe edge set by RFB configuration. In SLEEP, outputs are controlled by the OSS, SEL. General Purpose Input (GPI) General-purpose pins individually configured as inputs; which are used to control and respond to various commands. SERIAL CONTROL BUS - PC COMPATIBLE Clock line for the serial control bus communication SCL 1 Input/Output, Open Clock line for the serial control bus communication SDA 1 Input/Output, Open Data line for serial control bus communication SDA 1 Input/Output, Open Data line for serial control bus communication SDA 1 Input, LVCMOS w/ WS = L, Master, Slave select M/S 1 Input, LVCMOS w/ WS = L, Slave (default); device accepts SCL clock line the Slave Device Address. CAD 1 Input, LVCMOS w/ PDB = L, Receiver is in Sleep (Power down mode). When the Receiver is in the Slave Device rise rabled and is ON. PDB 1 Input, LVCMOS w/ | Din Nomo | Din Name Number of Dine 1/0 Ture | | | | | | |
|---|----------------------------|----------------------------------|-------------------------------|--|--|--|--|--|
| LVUMOS PARLEEL INTERFACE PCUT[20:0] 21 Outputs, LVCMOS Parallel data outputs. PCLK 1 Output, LVCMOS Strobe edge set by RFB configuration. In SLEEP, outputs are controlled by the OSS_SEL. General Purpose Input (GPI) Input/Output, Digital General-purpose pins individually configured as inputs; which are used to control and respond to various commands. SERIAL CONTROL BUS - IPC COMPATIBLE Input/Output, Open Data line for serial control bus communication SDA 1 Input/Output, Open Data line for serial control bus communication SDA 1 SERIAL CONTROL BUS - IPC COMPATIBLE Concentral pull-up resistor to V _{DOIO} . SDA 1 Input/Output, Open Data line for serial control bus communication SDA requires an external pull-up resistor to V _{DOIO} . SDA 1 Input, UCMOS W pull up PC Master / Slave select MVS = 1, Master; device generates and drives the SCL clock line MVS = 1, Master; device generates and drives the SCL clock line MVS = 1, Master; device generates and drives the SCL clock line MVS = 1, Master; device generates and drives the SCL clock line MVS = 1, Master; device generates and drives the SCL clock line MVS = 1, Master; device generates and drives the SCL clock line MVS = 1, Master; device generates and drives the SCL clock line MVS = 1, Master; device generates and drives the SCL clock line MVS = 1, Master; device generates and drives the SCL clock line MVS = 1, Master; device generates and drives the SCL clock line MVS = 1, Master; device generates and drives the SCL clock line MVS = 1 | | | | Description | | | | |
| HOUT(200) 21 Duputs, LVCMOS Parallel data outputs. PCLK 1 Output, LVCMOS Pixel Clock Output Pin. Strobe edge set by RFB configuration. In SLEEP, outputs are controlled by the OSS_SEL. General Purpose Input (GPI) General Purpose Input (GPI) General-purpose pins individually configured as inputs; which are used to control and respond to various commands. SERIAL CONTROL BUS - PC COMPATIBLE Clock line for the serial control bus communication SCL 1 Input/Output, Open Clock line for the serial control bus communication SDA 1 Input/Output, Open Data line for serial control bus communication SDA 1 Input/Output, Open Data line for serial control bus communication SDA 1 Input, UCMOS will pull up WS = L, Master, device generates and drives the SCL clock line M/S 1 Input, analog Input, analog Power down Mode Input Pin. PDB 1 Input, LVCMOS will pull down Pomer down Mode Input Pin. PDB 1 Input, LVCMOS will pull down Pomer down Mode Input Pin. PDB 1 Input, LVCMOS will down PDB = H, Receiver is enabled and is ON.< | | | | | | | | |
| PCLK 1 Output, LVCMOS Proceeding of the cost of the | ROUT[20:0] | 21 | Outputs, LVCMOS | Parallel data outputs. | | | | |
| PCLK 1 Output, LVGMOS Strobe edge set by PFB configuration. In SLEEP, outputs are controlled by the OSS_SEL. General Purpose Input (GPI) General Purpose pins individually configured as inputs; which are used to conitoi and respond to various commands. SERIAL CONTROL BUS - IPC COMPATIBLE General-purpose pins individually configured as inputs; which are used to conitoi and respond to various communication SCL 1 Input/Output, Open Drain Clock line for the serial control bus communication SDA requires an external pull-up resistor to V _{DDO} . SDA 1 Input/Output, OPen Drain Data line for serial control bus communication SDA requires an external pull-up resistor to V _{DDO} . M/S 1 Input, LVCMOS wi pull up Miss = L, Master; Slave select M/S 1 Input, analogi and sess (see Serial Control Bus Connection) CONTROL AND CONFIGURATION POB = L, Receiver is in Sileep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS Output are active LOCK LOCK 1 Output, LVCMOS wi pull dwn PDB = L, Receiver is in Sileep (Power down mode). When the Receiver is in shuddown and IDD is minimized. LOCK 1 Output, LVCMOS wi pull dwn PDB = L, Receiver is in Sileep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS Output Pin. LOCK 1 | | | | Pixel Clock Output Pin. | | | | |
| General-Purpose Input (GPI) (are GOU_SUL: General-Purpose Input (GPI) General-purpose pins individually configured as inputs; which are used to control and respond to various commands. SERIAL CONTROL BUS - IPC COMPATIBLE General-purpose pins individually configured as inputs; which are used to control and respond to various commands. SCL 1 Input/Output, Open Drain Clock line for the serial control bus communication SDA 1 Input/Uput, Open Drain SDA requires an external pull-up resistor to V _{DDO} . M/S 1 Input, LVCMOS with pull up for select SDA requires an external pull-up resistor to V _{DDO} . M/S 1 Input, LVCMOS with pull up for select the Slave Device Address. N/S = L, Master / Slave select M/S 1 Input, analog Input, ip in to select the Slave Device Address. N/S = L, Receiver is no Slave Gleauth, divice to programmable Device ID address (see Serial Control Bus Connection) CONTROL AND CONFIGURATION POWer down Mode Input Pin. PDB = L, Receiver is no Slave (Power down mode). When the Receiver is in the SLEEP State, the LVCMOS outputs are active LOCK = L, PLL is incloced, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Pin 46. This pin MUST be tied LOW. PDB Input, LVCMO | POLK | | | the OSS SEI | | | | |
| General-purpose input (GPT) Input/Output, Digital General-purpose pins individually configured as inputs; which are used to control and respond to various commands. SERIAL CONTROL BUS - IPC COMPATIBLE Input/Output, Open Clock line for the serial control bus communication SCL 1 Input/Output, Open Data line for serial control bus communication SDA 1 Input/Output, Open Data line for serial control bus communication SDA 1 Input/Output, Open Data line for serial control bus communication SDA 1 Input, UCMOS w/ pull up IPC Master / Slave select M/S 1 Input, analog IPC Master / Slave select Input, analog Input, analog Power down Mode Input Pin. PDB PDB 1 Input, LVCMOS w/ pull down POWer down Mode Input Pin. PDB = H. Receiver is in shee (Power down mode). When the Receiver is in the SLEEP state. the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. LOCK 1 Output, LVCMOS LOCK Status Output are as clive LOCK 1 Output, LVCMOS BIST MODE BIST MODE BIST MODE Reserved. Pin 46: This pin MUST be tied LOW. Pin 38, 39, 43: Leave pin open. | Caparal Durpa | [the USS_SEL. | | | | | | |
| GPI[3:0] 4 Input/Output, Digital Control and respond to various commands. SERIAL CONTROL BUS - IPC COMPATIBLE Input/Output, Open Drain Control and respond to various commands. SCL 1 Input/Output, Open Drain Clock line for the serial control bus communication SDA requires an external pull-up resistor to V _{DDO} . SDA 1 Input, LVCMOS w/ pull up Pasta for serial control bus communication SDA requires an external pull-up resistor to V _{DDO} . M/S 1 Input, LVCMOS w/ pull up IRC Master / Slave select M/S 1 Input, LVCMOS w/ pull up IRC Master / Slave Gedreass. Input is connect to external resistor divider to programmable Device ID address (see Serial Control Bus Connection) CONTROL AND CONFIGURATION Power down Mode Input Pin. PDB 1 Input, LVCMOS w/ pull down PDB 1 Input, LVCMOS w/ pull down PDB = L, Receiver is in Sleeg (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. LOCK 1 Output, LVCMOS w/ pull down SS SEL. May be used as Link Status. RES 4 - PIn 46: This pin MUST be tied LOW. Pin 38, 39, 43: Leave pin oppen. BIST Enable Pin. BISTEN = | | | | | | | | |
| Technol and respond of values communication SCL 1 Input/Output, Open Drain Clock line for the serial control bus communication SCL requires an external pull-up resistor to V _{DDOC} . SDA 1 Input/Output, Open Drain SCL requires an external pull-up resistor to V _{DDOC} . MS 1 Input/LVCMOS w/ pull up PC Master, device generates and drives the SCL clock line M/S = L, Master, device accepts SCL clock input CAD 1 Input, LVCMOS w/ pull up PC Master, device generates and drives the SCL clock line M/S = L, Master, device accepts SCL clock input CAD 1 Input, LVCMOS w/ pull up PC Master, device accepts SCL clock input CAD 1 Input, LVCMOS w/ pull down Power down Mode Input Pin. PDB = L, Receiver is enabled and is ON. PDB = L, Receiver is in Sleep (Power down mode). When the Receiver is in shutdown and IDD is minimized. LOCK 1 Output, LVCMOS POK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open. BISTEN 1 Input, LVCMOS w/ pull down BIST Enable Pin. BISTEN = L, BIST Mode is enabled. BISTEN = L, BIST | GPI[3:0] | 4 | Input/Output, Digital | control and respond to various commande | | | | |
| SCH. 2011 TOLE DOS FPC COMPATIBLE. Input/Cutput, Open Drain Clock line for the serial control bus communication SCL requires an external pull-up resistor to V _{DDO} . SDA 1 Input/Cutput, Open Data line for serial control bus communication SDA 1 Input/Cutput, Open Data line for serial control bus communication M/S 1 Input, LVCMOS w/ pull up PC Master / Slave select M/S 1 Input, LVCMOS w/ pull up PC Master / Slave select CAD 1 Input, LVCMOS w/ pull up PC Master / Slave select CAD 1 Input, analog Input is connect to external resistor divider to programmable Device ID address (see Serial Control Bus Connection) CONTROL AND CONFIGURATION Power down Mode Input Pin. POB = L, Receiver is in Sleep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. LOCK 1 Output, LVCMOS US DCK = H, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Pin 46. This pin MUST be tied LOW. Pin 38, 39, 43: Leave pin open. BIST Enable Pin. BISTEN 1 Input, LVCMOS w/ pull down BIST Enable Pin. BIST MODE BIST Mode is disab | | CONTROL BUS, 12C COMPATIBLE | | | | | | |
| SCL 1 Input/Output, Open Clock mile for the senial control dus sommunication SDA 1 Input/Output, Open Data line for serial control bus communication SDA 1 Input, LVCMOS w/ pull up PC Master / Slave select M/S 1 Input, LVCMOS w/ pull up PC Master / Slave select CAD 1 Input, LVCMOS w/ pull up PC Master / Slave select CAD 1 Input, analog Input is connect to external resistor divider to programmable Device ID address (see Serial Control Bus Connection) CONTROL AND CONFIGURATION POB 1 Input, LVCMOS w/ pull down PDB 1 Input, LVCMOS w/ pull down Power down Mode Input Pin. PDB = H, Receiver is nalbed and is ON. PDB = L, Receiver is nalbed and is ON. LOCK 1 Output, LVCMOS w/ pull down POK Status Output Pin. LOCK = 1, PL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Pin 46: This pin MUST be tied LOW. Pin 38, 39, 43: Leave pin open. BIST MODE Input, LVCMOS w/ pull down BIST Enable Pin. BISTEN = L, BIST Mode is disabled. BISTEN = L, BIST Mode is disabled. BISTEN = L, BIST Mode is disabled. BISTEN = L, BIST Mode is di | | | | Clock line for the serial control hus communication | | | | |
| Bit Note Distaine Description SDA 1 Input/Output, Open Drain Data line for serial control bus communication SDA requires an external pull-up resistor to V _{DDO} . M/S 1 Input, LVCMOS w/ pull up IPC Master / Slave select M/S = L, Master; device generates and drives the SCL clock line M/S = L, Master; device generates and drives the SCL clock line M/S = L, Master; device generates and drives the SCL clock line M/S = L, Master; device generates and drives the SCL clock line M/S = L, Master; device generates and drives the SCL clock line M/S = L, Master; device generates and drives the SCL clock line M/S = L, Master; device generates and drives the SCL clock line M/S = L, Master; device generates and drives the SCL clock line M/S = L, Master; device generates and drives the SCL clock line M/S = L, Master; device generates and drives the SCL clock line M/S = L, Master; device generates and drives the SCL clock line M/S = L, Master; device generates and drives the SCL clock line Input is connect to external resistor divider to programmable Device ID address (see Serial Control Bus Connection) CONTROL AND CONFIGURATION POWer down Mode Input Pin. PDB = L, Receiver is in Sleep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS OULD stare are in TRI-STATE, the PLL is shutdown and IDD is minimized. LOCK 1 Output, LVCMOS LOCK Status Output Pin. LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open. | SCL | 1 | Drain | | | | | |
| SDA 1 Input/Output, Open Drain Data regives an external pull-up resistor to V _{DDIO} . M/S 1 Input, LVCMOS w/ pull up M/S 1 Input, LVCMOS w/ pull up CAD 1 Input, analog Input, analog Input, analog Continuous Address Decoder Input is connect to external resistor divider to programmable Device ID address (see Serial Control Bus Connection) Contentious Address Decoder PDB 1 Input, LVCMOS w/ pull down Power down Mode Input Pin. PDB = H, Receiver is enabled and is ON. PDB = H, Receiver is enabled and is ON. PDB = 1 Input, LVCMOS w/ pull down PDB = H, Receiver is nabled and is ON. PDB = 1 Output, LVCMOS w/ pull down PDB = H, Receiver is nabled and is ON. PDB = 1 Output, LVCMOS w/ pull down PDB = H, Receiver is nabled and is ON. PDB = 1 Output, LVCMOS LOCK Status Output Pin. LOCK 1 Output, LVCMOS BIST MODE Reserved. Pin 46: This pin MUST be tied LOW. Pin 38; 39; 43: Leave pin open. BIST Enable Pin. BISTEN 1 Input, LVCMOS w/ pull down BIST EN = 1, BIST Mode is enabled. BISTEN = H, BIST Mode is disabled. PASS 1 Output, LVCMOS w/ pull down BISTEN = 1, | | | | Data line for parial control hus communication | | | | |
| Drain Processed M/S 1 Input, LVCMOS w/ pull up PC Master / Slave select M/S = L, Master; device generates and drives the SCL clock line M/S = H, Slave (default); device accepts SCL clock input CAD 1 Input, analog Input in to select the Slave Device Address. Input is connect to external resistor divider to programmable Device ID address (see Serial Control Bus Connection) CONTROL AND CONFIGURATION POBe H, Receiver is enabled and is ON. PDB = L, Receiver is in Sleep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS of Uputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. LOCK 1 Output, LVCMOS LOCK Status Output Pin. LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Pin 46: This pin MUST be tied LOW. Pin 38, 39, 43: Leave pin open. BIST MODE BIST Enable Pin. BISTEN Input, LVCMOS w/ pull down BIST Enable Pin. BISTEN = H, BIST Mode is disabled. PASS = L, ORE or more errors were detected in the received payload. Leave Open if unused | SDA | 1 | Drain | SDA requires an external null-un resistor to V | | | | |
| M/S 1 Input, LVCMOS w/ pull up Input, analog Instar: device generates and drives the SCL clock line M/S = H, Slave (default); device accepts SCL clock input CAD 1 Input, analog Continuous Address Decoder Input to select the Slave Device Address. Input is connect to external resistor divider to programmable Device ID address (see Serial Control Bus Connection) CONTROL AND CONFIGURATION Power down Mode Input Pin. PDB 1 PDB 1 Input, LVCMOS w/ pull down POWer down Mode Input Pin. PDB = L, Receiver is enabled and is ON. PDB = L, Receiver is enabled and is ON. PDB = L, Receiver is in Sleep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. LOCK 1 Output, LVCMOS LOCK Status Output Pin. LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open. BIST MODE BIST Enable Pin. BISTEN 1 Input, LVCMOS w/ pull down BIST Enable Pin. BISTEN = L, BIST Mode is enabled. BISTEN = L, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled. PASS 1 Output, LVCOMS PASS = H, ERPOR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE Input/Output, CML Noninverting differential input, back channel output. | | | | In the second part of the second | | | | |
| Image: Section of the sectin the sectin the sectin the secting and the section o | M/S | 1 | Input, LVCMOS w/ | M/S = 1 Master: device generates and drives the SCL cleak line | | | | |
| CAD 1 Input, analog Continuous Address Decoder Input, analog Input, analog Input is connect to external resistor divider to programmable Device ID address (see Serial Control Bus Connection) CONTROL AND CONFIGURATION Power down Mode Input Pin. PDB 1 Input, LVCMOS w/ pull down Power down Mode Input Pin. PDB 1 Input, LVCMOS w/ pull down Power down Mode Input Pin. PDB 1 Input, LVCMOS w/ pull down PDB = L, Receiver is enabled and is ON. PDB 1 Output, LVCMOS w/ pull down PDB = L, Receiver is in Sleep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. LOCK 1 Output, LVCMOS LOCK Status Output Pin. LOCK 1 Output, LVCMOS LOCK Status Output Pin. LOCK 1 Output, LVCMOS BiST Enable Pin. BIST MODE BIST Enable Pin. BIST Enable Pin. BISTEN 1 Input, LVCMOS w/ pull down BIST Enable Pin. BISTEN 1 Output, LVCMOS w/ pull down BISTEN = L, BIST Mode is disabled. PASS <t< td=""><td>101/3</td><td></td><td>pull up</td><td>M/S = H. Slave (default): device accepts SCL clock input</td></t<> | 101/3 | | pull up | M/S = H. Slave (default): device accepts SCL clock input | | | | |
| CAD 1 Input, analog Input in to select the Slave Device Address. Input in to select the Slave Device Address. CONTROL AND CONFIGURATION Power down Mode Input Pin. PDB 1 Input, LVCMOS w/ pull down Power down Mode Input Pin. PDB 1 Input, LVCMOS w/ pull down POB = H, Receiver is enabled and is ON. LOCK 1 Output, LVCMOS PDB = L, Receiver is in Sleep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. LOCK 1 Output, LVCMOS LOCK = L, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open. BIST Enable Pin. BIST MODE BIST Enable Pin. PASS 1 Output, LVCOMS PASS 1 Output, LVCOMS PASS 1 Output, LVCOMS PASS 1 Output, LVCOMS PASS 1 Input, LVCOMS PASS 1 Output, LVCOMS PASS 1 Output, LVCOMS PASS Outpu | | | | Continuous Address Deceder | | | | |
| CAD 1 Input, analog Input, pin to solect the stared resistor divider to programmable Device ID address (see Serial Control Bus Connection) CONTROL AND CONFIGURATION Power down Mode Input Pin. Power down Mode Input Pin. PDB 1 Input, LVCMOS w/ pull down Power down Mode Input Pin. PDB = H, Receiver is enabled and is ON. PDB 1 Input, LVCMOS w/ pull down Power down Mode Input Pin. PDB = H, Receiver is in Sleep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. LOCK 1 Output, LVCMOS LOCK Status Output Pin. LOCK = L, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open. BIST MODE BISTEN 1 Input, LVCMOS w/ pull down BISTEN = H, BIST Mode is disabled. PASS Output Pin for BIST mode. PASS 1 Output, LVCOMS ASS Output Pin for BIST mode. PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE 1 Input/Output, CML Noninverting differential input, back channel output. <td></td> <td></td> <td></td> <td>Linut nin to colori the Slove Device Address</td> | | | | Linut nin to colori the Slove Device Address | | | | |
| Input is connect to external resistor divident or programmable bender by address (see Serial Connection) CONTROL AND CONFIGURATION PDB 1 Input, LVCMOS w pull down Power down Mode Input Pin. PDB = H, Receiver is enabled and is ON. PDB = L, Receiver is in Sleep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. LOCK 1 Output, LVCMOS LOCK Status Output Pin. LOCK = L, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Reserved. BIST MODE BIST Enable Pin. BISTEN BIST Enable Pin. BISTEN = H, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled. PASS 1 Output, LVCOMS BIST Enable Pin. BISTEN = L, BIST Mode. PASS 1 Output, LVCOMS PASS Output Pin for BIST mode. PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE Filtheret RIN- 1 Input/Output, CML Noninverting differential input, back channel output. | CAD | 1 | Input, analog | Input pin to select the Slave Device Address. | | | | |
| Tendences (dec control Dub Control | | | | address (see Serial Control Bus Connection) | | | | |
| PDB 1 Input, LVCMOS w pull down Power down Mode Input Pin. PDB = H, Receiver is enabled and is ON. PDB = L, Receiver is in Sleep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. LOCK 1 Output, LVCMOS LOCK Status Outputs are active LOCK = H, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open. BIST MODE Input, LVCMOS w pull down BIST Enable Pin. BISTEN 1 BISTEN 1 Output, LVCMOS w pull down BIST Enable Pin. BISTEN = H, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled. PASS 1 Output, LVCOMS PASS Output Pin for BIST mode. PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE RiN+ 1 Input/Output, CML Noninverting differential input, back channel output. | | | | | | | | |
| PDB1Input, LVCMOS w/ pull downPDB = H, Receiver is enabled and is ON. PDB = H, Receiver is in Sleep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized.LOCK1Output, LVCMOSLOCK Status Output Pin. LOCK = L, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status.RES4-Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open.BIST MODEInput, LVCMOS w/ pull downBIST Enable Pin. BISTEN = L, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled.PASS1Output, LVCOMS pull downPASS1Output, LVCOMS pull downPASS1Input, LVCOMS pull downPASS1Input/Output, LVCOMS pull downPASS1Input/Output, CML pull downPASS1Input/Output, CML pull downPASS1Input/Output, CML pull downPASS1Input/Output, CML pull downPASS <td></td> <td></td> <td></td> <td>Power down Mode Input Pin</td> | | | | Power down Mode Input Pin | | | | |
| PDB 1 Input, LVCMOS w/ pull down PDB = 1, Receiver is in Steep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. LOCK 1 Output, LVCMOS LOCK Status Output Pin. LOCK 1 Output, LVCMOS LOCK Status Output Pin. LOCK LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open. BIST Enable Pin. BISTEN 1 Input, LVCMOS w/ pull down BIST Enable Pin. BISTEN 1 Output, LVCMOS w/ pull down BIST Enable Pin. BISTEN 1 Output, LVCMOS w/ pull down BIST Enable Pin. BISTEN 1 Output, LVCMOS w/ pull down BIST Enable Pin. BISTEN 1 Output, LVCMOS w/ pull down PASS Output Pin for BIST mode. PASS 1 Output, LVCOMS PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE ENN+ 1 Input/Output, CML Noninverting differential input, back channel output. | | | Input, LVCMOS w/ pull down | PDB = H. Beceiver is enabled and is ON | | | | |
| pull down pull down the SLEEP state, the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. LOCK 1 Output, LVCMOS LOCK Status Output Pin. LOCK = L, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 Pin 46: This pin MUST be tied LOW. Pin 38, 39, 43: Leave pin open. BIST MODE BISTEN 1 Input, LVCMOS w/ pull down BISTEN 1 Input, LVCMOS w/ pull down BISTEN 1 Output, LVCOMS PASS 1 Output, LVCOMS PASS 1 Output, LVCOMS PASS 1 Input, LVCOMS PASS 1 Output, LVCOMS PASS 1 Output, LVCOMS PASS 1 Output, LVCOMS PASS 1 Output, LVCOMS PASS = L, ene or more errors were detected in the received payload. Leave Open if unused. Route to test | PDB | 1 | | PDB = 1, Receiver is in Sleep (Power down mode). When the Receiver is in | | | | |
| LOCK1Output, LVCMOSLOCK Status Output Pin. LOCK = H, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status.RES4-Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open.BIST MODE1Input, LVCMOS w/ pull downBIST Enable Pin. BISTEN = H, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled.PASS1Output, LVCOMS pull downPASS Output Pin for BIST mode. PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended.Channel Link III INTERFACE1Input/Output, CMLNoninverting differential input, back channel output.RIN-1Input/Output, CMLInverting differential input, back channel output. | | | | the SLEEP state, the LVCMOS Outputs are in TRI-STATE, the PLL is | | | | |
| LOCK 1 Output, LVCMOS LOCK Status Output Pin. LOCK = H, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open. BIST MODE Input, LVCMOS w/ pull down BIST Enable Pin. BISTEN 1 1 Input, LVCMOS w/ pull down BIST Enable Pin. BISTEN = L, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled. PASS 1 Output, LVCOMS PASS Output Pin for BIST mode. PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE Input/Output, CML Noninverting differential input, back channel output. RIN- 1 Input/Output, CML Inverting differential input, back channel output. | | | | shutdown and IDD is minimized. | | | | |
| LOCK1Output, LVCMOSLOCK = H, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status.RES4-Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open.BIST MODEBISTEN1Input, LVCMOS w/ pull downBIST Enable Pin. BISTEN = H, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled.PASS1Output, LVCOMS pull downPASS Output Pin for BIST mode. PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended.Channel Link III INTERFACEInput/Output, CMLNoninverting differential input, back channel output.RIN-1Input/Output, CMLInverting differential input, back channel output. | | | Output, LVCMOS | LOCK Status Output Pin. | | | | |
| LOCK I Output, LVCMOS LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status. RES 4 - Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open. BIST MODE Input, LVCMOS w/ pull down BIST Enable Pin. BIST Mode is enabled. BISTEN = H, BIST Mode is disabled. PASS 1 Output, LVCOMS PASS Output Pin for BIST mode. PASS = H, ERROR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE Input/Output, CML Noninverting differential input, back channel output. RIN- 1 Input/Output, CML Inverting differential input, back channel output. | | 4 | | LOCK = H, PLL is Locked, outputs are active | | | | |
| Image: Constraint of the second se | LUCK | | | LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by | | | | |
| RES4-Reserved. Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open.BIST MODEBISTEN1Input, LVCMOS w/ pull downBIST Enable Pin. BISTEN = H, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled.PASS1Output, LVCOMS PASS = H, ERROR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended.Channel Link III INTERFACEInput/Output, CMLNoninverting differential input, back channel output.RIN+1Input/Output, CMLInverting differential input, back channel output. | | | | OSS_SEL. May be used as Link Status. | | | | |
| RES 4 - Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open. BIST MODE BIST MODE BIST Enable Pin. BISTEN BIST Enable Pin. PUII down BIST Enable Pin. BISTEN = H, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled. PASS 1 Output, LVCOMS Output, LVCOMS PASS Output Pin for BIST mode. PASS = H, ERROR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE Input/Output, CML Noninverting differential input, back channel output. RIN+ 1 Input/Output, CML Inverting differential input, back channel output. | RES | 4 | - | Reserved. | | | | |
| BIST MODE BISTEN 1 Input, LVCMOS w/ pull down BIST Enable Pin. BISTEN = H, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled. PASS 1 Output, LVCOMS PASS Output Pin for BIST mode. PASS = H, ERROR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE Input/Output, CML Noninverting differential input, back channel output. RIN- 1 Input/Output, CML Inverting differential input, back channel output. | | | | Pin 46: This pin MUST be tied LOW. | | | | |
| BIST MODE BISTEN 1 Input, LVCMOS w/ pull down BIST Enable Pin. BISTEN = H, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled. PASS 1 Output, LVCOMS PASS Output Pin for BIST mode. PASS = H, ERROR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE Input/Output, CML Noninverting differential input, back channel output. RIN- 1 Input/Output, CML Inverting differential input, back channel output. | | | | Pins 38, 39, 43: Leave pin open. | | | | |
| BISTEN 1 Input, LVCMOS w/ pull down BIST Enable Pin. BISTEN = H, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled. PASS 1 Output, LVCOMS PASS Output Pin for BIST mode. PASS = H, ERROR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE Noninverting differential input, back channel output. RIN- 1 Input/Output, CML Noninverting differential input, back channel output. | BIST MODE | | | | | | | |
| BISTEN 1 Imput, LVCMOS W/ pull down BISTEN = H, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled. BISTEN = L, BIST Mode is disabled. PASS 1 Output, LVCOMS PASS Output Pin for BIST mode. PASS = H, ERROR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE Input/Output, CML Noninverting differential input, back channel output. RIN- 1 Input/Output, CML Inverting differential input, back channel output. | | 1 | Input, LVCMOS w/ pull down | BIST Enable Pin. | | | | |
| PASS 1 Output, LVCOMS PASS Output Pin for BIST mode. PASS 1 Output, LVCOMS PASS Output Pin for BIST mode. PASS = H, ERROR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE Input/Output, CML Noninverting differential input, back channel output. RIN- 1 Input/Output, CML Inverting differential input, back channel output. | BISTEN | | | BISTEN = H, BIST Mode is enabled. | | | | |
| PASS 1 Output, LVCOMS PASS Output Pin for BIST mode. PASS = H, ERROR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE Input/Output, CML Noninverting differential input, back channel output. RIN- 1 Input/Output, CML Inverting differential input, back channel output. | | | | BISTEN = L, BIST Mode is disabled. | | | | |
| PASS 1 Output, LVCOMS PASS = H, ERROR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE RIN+ 1 Input/Output, CML Noninverting differential input, back channel output. RIN- 1 Input/Output, CML Inverting differential input, back channel output. | PASS | 1 | Output, LVCOMS | PASS Output Pin for BIST mode. | | | | |
| PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended. Channel Link III INTERFACE RIN+ 1 Input/Output, CML Noninverting differential input, back channel output. RIN- 1 Input/Output, CML Inverting differential input, back channel output. | | | | PASS = H, ERROR FREE Transmission | | | | |
| Channel Link III INTERFACE Leave Open if unused. Route to test point (pad) recommended. RIN+ 1 Input/Output, CML Noninverting differential input, back channel output. RIN- 1 Input/Output, CML Inverting differential input, back channel output. | | | | PASS = L, one or more errors were detected in the received payload. | | | | |
| Channel Link III INTERFACE RIN+ 1 Input/Output, CML Noninverting differential input, back channel output. RIN- 1 Input/Output, CML Inverting differential input, back channel output. | | | | Leave Open if unused. Route to test point (pad) recommended. | | | | |
| RIN+ 1 Input/Output, CML Noninverting differential input, back channel output. RIN- 1 Input/Output, CML Inverting differential input, back channel output. | Channel Link III INTERFACE | | | | | | | |
| RIN- 1 Input/Output, CML Inverting differential input, back channel output. | RIN+ | 1 | Input/Output, CML | Noninverting differential input, back channel output. | | | | |
| | RIN- | 1 | Input/Output, CML | Inverting differential input, back channel output. | | | | |

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| DS |
| DSS |
| DS92 |
| DS92L |
| DS92LX |
| DS92LX2 |
| DS92LX21 |
| DS92LX212 |
| DS92LX2122 |

| Pin Name | Number of Pins | I/O, Type | Description | | |
|------------------|----------------|---------------|---|--|--|
| POWER AND GROUND | | | | | |
| VDDSSCG | 1 | Digital Power | SSCG Power, 1.8V ±5% | | |
| VDDOR1/2/3 | 3 | Digital Power | ver TTL Output Buffer Power, The single-ended outputs and control input are powered from V_{DDIO} . V_{DDIO} can be connected to a 1.8V ±5% or 3.3V ±10 | | |
| VDDD | 1 | Digital Power | Digital Core Power, 1.8V ±5% | | |
| VDDR | 1 | Analog Power | Rx Analog Power, 1.8V ±5% | | |
| VDDCML | 1 | Analog Power | BC Driver Power, 1.8V ±5% | | |
| VDDPLL | 1 | Analog Power | PLL Power, 1.8V ±5% | | |
| VSS | - | Ground | All VSS pads are down bonded to DAP. DAP must be grounded. | | |

DS92LX2121 / DS92LX2122



Notes

Notes

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| Switching Regulators | www.national.com/switchers | Distributors | www.national.com/contacts |
| LDOs | www.national.com/ldo | Quality and Reliability | www.national.com/quality |
| LED Lighting | www.national.com/led | Feedback/Support | www.national.com/feedback |
| Voltage References | www.national.com/vref | Design Made Easy | www.national.com/easy |
| PowerWise® Solutions | www.national.com/powerwise | Applications & Markets | www.national.com/solutions |
| Serial Digital Interface (SDI) www.national.com/sdi | | Mil/Aero | www.national.com/milaero |
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