HD49211BFS

Single-Chip Signal Processing LSI

Description

The HD49211BFS is a CMOS LSI chip designed for R-DAT (rotary head digital audio tape) signal processing. It has the following functions and features.

Functions

- Interfaces to microprocessor using clock-synchronous serial communication
- 8 of 9 modulation/demodulation of record and playback signals
- Zero-cross mute and fade mute
- RAM control
- Parity generate and parity error correction
- Digital audio interface
- A/D-D/A converter control

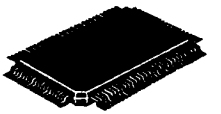
Features

- Works with 3 types of sampling frequencies:
  48 kHz 16-bit 2-channel
  44.1 kHz 16-bit 2-channel
  32 kHz 16-bit 2-channel
- 200x search of subcode data
- Subcode data after-recording
- Variable-speed playback of PCM voice data and subcode data
- On-chip 8-fold error correction circuitry
  C1 : maximum 2-fold EDC
  C2 : maximum 6-fold EDC
- On-chip A/D and D/A control circuit
  Control logic for 3-slope integrating A/D-D/A converters HA12096NT, HA12108NT/MP, HA12131MP, HA12132MP
- On-chip digital audio interface circuit
- On-chip digital level meter circuit

Ordering Information

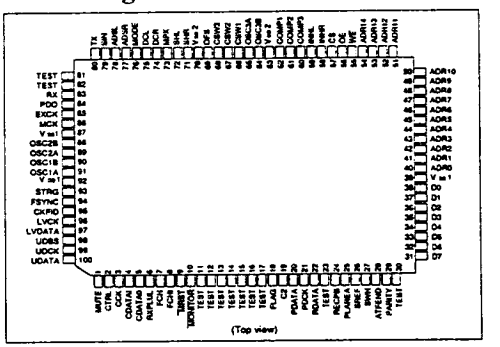
Type No.	Package
HD49211BFS	FP-100A

• HD49211BFS



(FP-100A)

Pin Arrangement



Pin Descriptions

Pin No.	Pin Name	Designation	I	O	Connection	Function	Settings H	Settings L	I/O type
1	MUTE	Mute	○		Microprocessor	Mute control signal	EN	Norm	CI
2	CTRL	Control	○		Microprocessor	Microprocessor data transfer mode control signal input	EN	Norm	C
3	CCK	Microcomputer data clock	○		Microprocessor	Microprocessor data transfer synchronous clock input			C
4	CDATAI	Microcomputer data input	○		Microprocessor transfer input	Microprocessor data		C	
5	CDATAO	Microcomputer data output		○	Microprocessor	Microprocessor data transfer output			
6	RXPLUL	RX PLL unlock		○	Microprocessor	Lock/unlock output during RX input	UN LOCK	LOCK	
7	FCH	Channel frequency		○	FCH I HD49212	Channel clock output (9.408 MHz)			HS
8	FCHI	Channel input frequency	○		FCH	Channel clock input			C
9	MRST	Master reset	○		Pull up	Master reset	Norm	RST	CR
10	MONITOR	Monitor	○		Pull up	Monitor control signal for internal signals	Norm	En	CR
11	TEST	—	○		Pull up				
12	TEST	—			NC				
13	TEST	—			NC				
14	TEST	—			NC				
15	TEST	—			NC				
16	TEST	—			NC				
17	TEST	—			NC				
18	FLAG	Error flag		○	Monitor	Correction flag output			
19	C2	C2 area		○	Monitor	C2 corrected area output			
20	PDATA	Playback data	○		HA12062A	Playback signal input			C
21	PDCK	Playback data Clock	○		HA12062A	Playback signal synchronous clock input		C	
22	RDATA	Rec data		○	HA12133	Record signal output			HS
23	TEST	—	○		Pull up				
24	RECPB	Rec playback select		○	HA12133	Record/playback control signal output	REC	PB	
25	PLAREA	Pilot area		○	HA12133	ATF pilot signal record area output	AREA		
26	SREF	Servo reference		○	Servo reference signal output				
27	SWH	Switch head	○		HD49212	Switch head signal input			C
28	ATFEND	ATF end	○		HD49212	ATF area detection signal input			C
29	PARITY	Parity		○	HD49212	Parity detection output	OK		
30	TEST	—	○		Pull up				
31	D7	Data 7	○	○	HM62256 (HM65256B)	RAM data input/output			B
32	D6	Data 6	○	○	HM62256 (HM65256B)	RAM data input/output			B

Pin Descriptions (cont)

Pin No.	Pin Name	Designation	I	O	Connection	Function	Settings H	Settings L	I/O type
33	D5	Data 5	○	○	HM62256 (HM65256B)	RAM data input/output			B
34	D4	Data 4	○	○	HM62256 (HM65256B)	RAM data input/output			B
35	D3	Data 3	○	○	HM62256 (HM65256B)	RAM data input/output			B
36	D2	Data 2	○	○	HM62256 (HM65256B)	RAM data input/output			B
37	D1	Data 1	○	○	HM62256 (HM65256B)	RAM data input/output			B
38	D0	Data 0	○	○	HM62256 (HM65256B)	RAM data input/output			B
39	V_{SS} 1	V_{SS} 1			GND	Ground for signal processing circuitry			
40	ADR 0	Address 0		○	HM62256 (HM65256B)	RAM address output			
41	ADR 1	Address 1		○	HM62256 (HM65256B)	RAM address output			
42	ADR 2	Address 2		○	HM62256 (HM65256B)	RAM address output			
43	ADR 3	Address 3		○	HM62256 (HM65256B)	RAM address output			
44	ADR 4	Address 4		○	HM62256 (HM65256B)	RAM address output			
45	ADR 5	Address 5		○	HM62256 (HM65256B)	RAM address output			
46	ADR 6	Address 6		○	HM62256 (HM65256B)	RAM address output			
47	ADR 7	Address 7		○	HM62256 (HM65256B)	RAM address output			
48	ADR 8	Address 8		○	HM62256 (HM65256B)	RAM address output			
49	ADR 9	Address 9		○	HM62256 (HM65256B)	RAM address output			
50	ADR 10	Address 10		○	HM62256 (HM65256B)	RAM address output			
51	ADR 11	Address 11		○	HM62256 (HM65256B)	RAM address output			
52	ADR 12	Address 12		○	HM62256 (HM65256B)	RAM address output			
53	ADR 13	Address 13		○	HM62256 (HM65256B)	RAM address output			
54	ADR 14	Address 14		○	HM62256 (HM65256B)	RAM address output			
55	$\overline{WE}$	$\overline{Write\ enable}$		○	HM62256 (HM65256B)	RAM write enable signal	INH	EN	
56	$\overline{OE}$	$\overline{Output\ enable}$		○	HM62256 (HM65256B)	RAM output enable signal	INH	EN	
57	$\overline{CS}$	$\overline{Chip\ select}$		○	(HM65256B)	RAM chip select (MONITOR = L→SLOT Number Monitor)	INH	EN	

Pin Descriptions (cont)

Pin No.	Pin Name	Designation	I	O	Connection	Function	Settings H	Settings L	I/O type
58	INHR	Inhibit R	○		A/D right channel	Inhibit control signal for operation	Norm	INH	
59	INHL	Inhibit M	○			Inhibit control signal for A/D left channel operation	Norm	INH	
60	COMP 3	Comparator 3	○		HA12131 (HA12132)	A/D comparator signal input			C
61	COMP 2	Comparator 2	○		HA12131 (HA12132)	A/D comparator signal input			C
62	COMP 1	Comparator 1	○		HA12131 (HA12132)	A/D comparator signal input			C
63	V_{DD} 2	V_{DD} 2			+5V	Power supply for A/D-D/A output signals			
64	OSC 3B	Oscillator 3B		○	X'tal	37.632 MHz oscillator output			
65	OSC 3A	Oscillator 3A	○		X'tal	37.632 MHz oscillator input			C
66	CSW 1	Current switch 1		○	HA12131 (HA12132)	A/D-D/A current source control signal-output	ON	OFF	HS
67	CSW 2	Current switch 2		○	HA12131 (HA12132)	A/D-D/A current source control signal-output	ON	OFF	HS
68	CSW 3	Current switch 3		○	HA12131 (HA12132)	A/D-D/A current source control signal-output	ON	OFF	HS
69	OFS	Offset switch		○	HA12131 (HA12132)	D/A offset circuit control signal output	ON	OFF	HS
70	V_{SS} 2	V_{SS} 2			GND	Ground for A/D-D/A output signals			
71	SHR	Sample hold R		○	HA12131 (HA12132)	D/A right channel sample-hold signal output INHL = 0 or INHR = 0→ Serial Out output)	S S	H H	
72	SHL	Sample hold M		○	HA12131 (HA12132)	D/A left channel sample-hold signal output INHL = 0 or INHR = 0→ BCK output	S	H	
73	MPX	Multiplexer		○	HA12131 (HA12132)	I/O left/right select signal output	R	M	
74	DCR	Discharge R		○	HA12131 (HA12132)	D/A right channel dischargesignal output INHL = 0 or INHR = 0→FX × 2	D		
75	DCL	Discharge M		○	HA12131 (HA12132)	output) D/A left channel discharge signal output) INHL = 0 or INHR = 0→ FS × 4 output	DC		
76	MODE	Mode		○	HA12131 (HA12132)	A/D-D/A switching signal output INHL = 0 or INHR = 0→interpolation flag output)	A/D	D/A	

Pin Descriptions (cont)

Pin No.	Pin Name	Designation	I	O	Connection	Function	Settings H	Settings L	I/O type
77	ADSR	AD servo R		○	HA12131 (HA12132)	A/D right channel offset PWM signal output for servo			
78	ADSL	AD servo M		○	HA12131 (HA12132)	A/D left channel offset PWM signal output for servo			
79	SIN	Serial input	○		External A/D	Serial signal input			C
80	TX	TX		○	Digital output	Digital audio interface			HS
81	TEST	—			N.C.				
82	TEST	—		○	GND				
83	RX	RX		○	Digital input	Digital audio interface input			C
84	PDO	Phase detector output		○	PLL	Phase comparator output			
85	EXCK	External clock	○		PLL	External master clock input			B
86	MCK	Master clock		○		Master clock output			HS
87	V_{SS} 1	V_{SS} 1			GND	Ground for signal processing circuitry			
88	OSC 2B	Oscillator 2B		○	X'tal	11.2896/22.5792 MHz oscillator output			
89	OSC 2A	Oscillator 2A	○		X'tal	11.2896/22.5792 MHz oscillator input			C
90	OSC 1B	Oscillator 1B		○	X'tal	11.288/24.576 MHz oscillator output			
91	OSC 1A	Oscillator 1A	○		X'tal	11.288/24.576 MHz oscillator input			C
92	V_{DD} 1	V_{DD} 1			+5V	Power supply for signal processing circuitry			
93	STRG	Sync trigger	○			Frame synchronizing signal input			C
94	FSYNC	Frame sync		○	Microprocessor	Frame synchronizing signal output			
95	CKFID	Clock fidelity	○		pull up	TX clock fidelity control input	LEVEL 2	LEVEL 1	CR
96	LVCK	Level meter clock	○		Microprocessor	CR clock input for level meter data			C
97	LVDATA	Level meter data		○	Microprocessor	Level meter data output			
98	UDBS	U Data block sync		○	Microprocessor	RX input U-bit data synchronous output			
99	UDCK	U Data clock		○	Microprocessor	RX input U-bit data synchronous clock output			
100	UDATA	U Data		○	Microprocessor	RX input U-bit data output			

C: CMOS-level input buffer
B: TTL-level input buffer
HS: High-speed output buffer
CR: Pull-up resistor buffer

Functional Description

Figure 1 shows an example configuration of a DAT system using the HD49211BFS. The HD49211BFS performs R-DAT signal processing through eight different blocks: record/playback block, microprocessor interface block, interpolation block, RAM control block, timing generation block, error correction block, digital audio interface block, and A/D-D/A control block.

- Microprocessor interface block

  This block interfaces to a microprocessor through clock-synchronous serial communication.

- Record/playback block

  During recording and playback, this block performs 8-10 modulation and demodulation, area control, as well as safeguarding of synchronous detection.

- Interpolation block

  This block performs interpolation of error datatogether with zero-cross mute and fade mute, and performs REC muting with zero-cross mute.

- RAM control block

  This block controls the RAM as well as generates interleaved and de-interleaved addresses.

- Timing generation block

  This block generates the system clock within the HD49211BFS and controls the timing of each block.

- Error correction block

  This block generates C1 parity and C2 parity during recording and performs 8-fold error correction during playback.

- Digital audio interface block

  This block performs the digital audio interface with the external system through controlling the states of the RX and TX pins.

- A/D-D/A control block

  This block controls external 3-slope integrating A/D-D/A converters: HA12131MP HA12132MP, HA12108MP/NT, or HA12096NT.

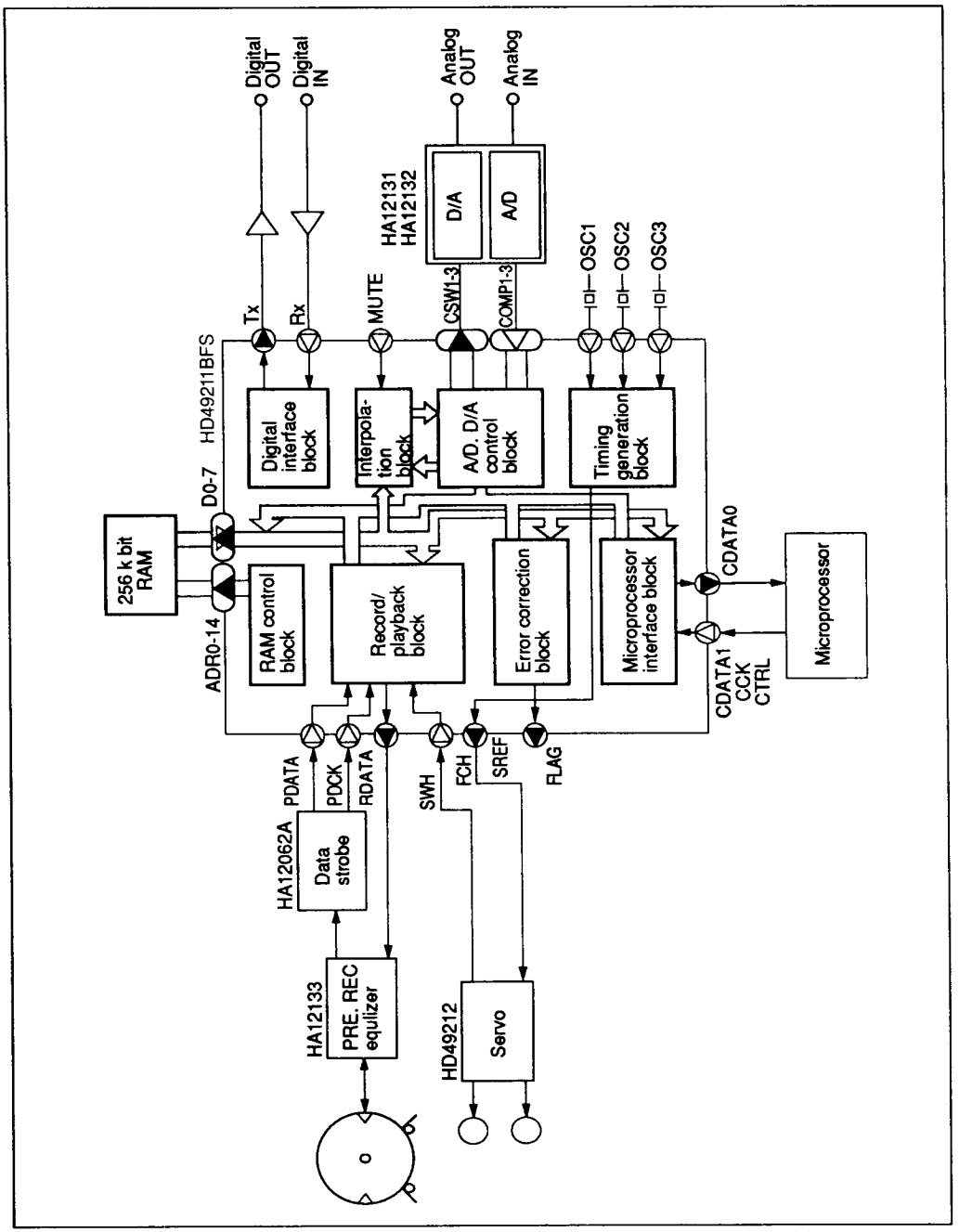


Figure 1 Example Configuration of DAT System using the HD49211BFS

Microprocessor Interface Block

Block Overview

This block takes care of the transfer of mode data, subcode data, level meter data, and digital audio interface U-bit data between the system control microprocessor and the HD49211BFS. Figure 2 shows an interface circuit with the system control microprocessor. Note that the CCK, CDATAI, and CTRL pins are also shared with the servo control LSI (HD49212).
The system microprocessor interface pins are as follows:

FSYNC (pin 94) : 30 ms/period synchronizing signal.

CCK (pin 3) : I/O clock for CDATAI and CDATAO. CDATAI is latched on the rising edge and CDATAO changes on the falling edge.

CDATAI (pin 4) : Input for control data, subcode data control signals, etc.

CDATAO (pin 5) : Output for subcode data, etc.

CTRL (pin 2) : As a control signal for CDATAI, brought to "H" when control data is input.

UDBS (pin 98) : When mode data IS=2 and RP=1 or 2, inputs data from the digital interface.

UDCK (pin 99) : Output for the U-bit data.

UDATA (pin 100) : Details are explained in Microprocessor access cycles.

LVCK (pin 96) : Digital level meter output. Described in Lecel meter data ouput.

LVDATA (pin 97) :

MUTE (pin 1) : Mutes the audio data output. An "H" level turns mute on, and all zeroes will be output. During recording it becomes the mute for the record monitor output, so only the record monitor output will become all zeroes.

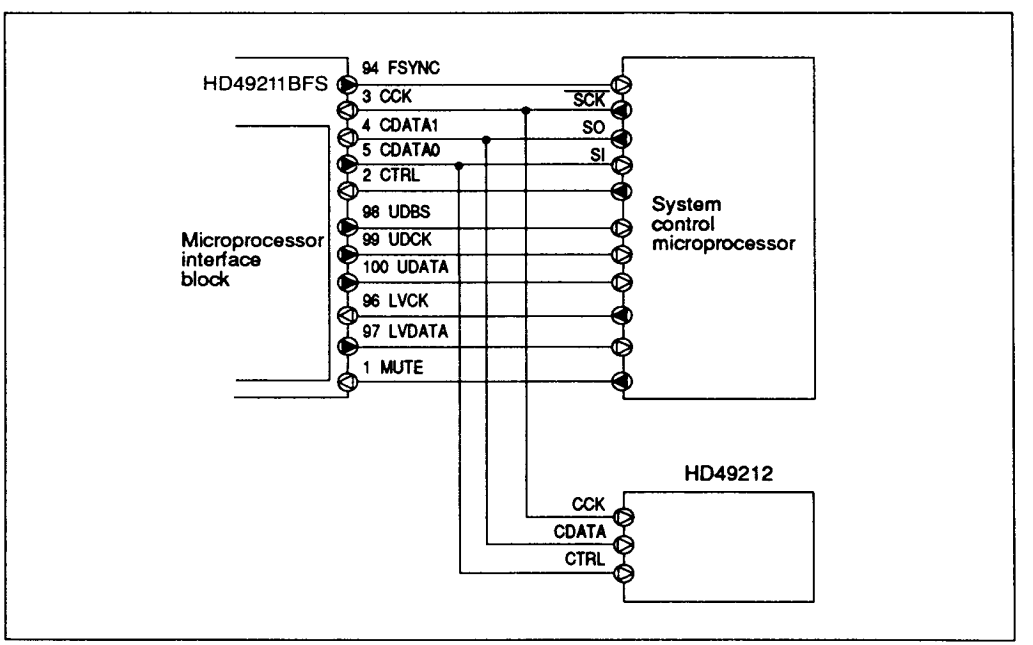


Figure 2 Interface Circuit with System Microprocessor

Block Function

Transfer Function for Mode Data and Subcode Data

Corresponding to the states of CTRL (pin 2), CCK (pin 3), CDATAI (pin 4), and CDATAO (pin 5). Mode data for controlling the HD49211BFS will be transferred or subcode data record/playback will be performed. Figure 3 shows the basic sequence for transferring data.

First, CTRL is brought to "H" and control data is transferred. Control data determines HD49211FS chip selection, CDATAO bus control, and transfer data type.

Next, transfer of the specified data begins. Since these interface pins are also shared with servo control LSI (HD49212) pins, when controlling the HD49211BFS the control data MSB must be "L".

CDATAI is latched on the rising edge of CCK and CDATAO changes on the falling edge.

Microprocessor Access cycles

During variable-speed playback (mode data AC=1) or search (mode data AC=2), the FSYNC signal (pin 94) frequency and duty cycle will not change, so the microprocessor should be accessed in conjunction with FSYNC. Also, as shown in figure 4, accesses should be ended by transferring an "OFF mode" before the falling edge of FSYNC (falling or rising edge of FSYNC for subcode data accesses during playback).

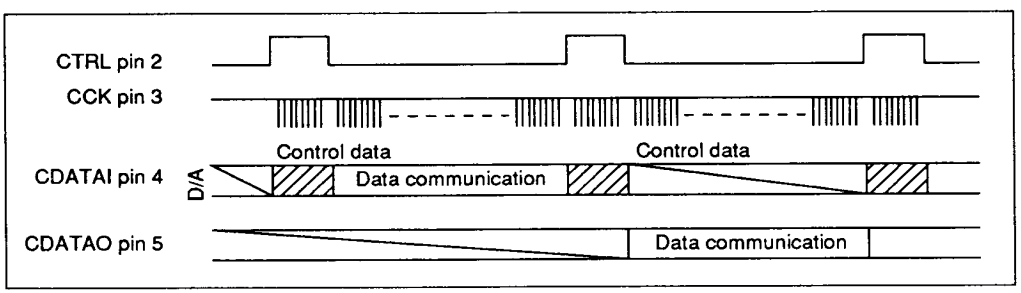


Figure 3 Transfer Timing

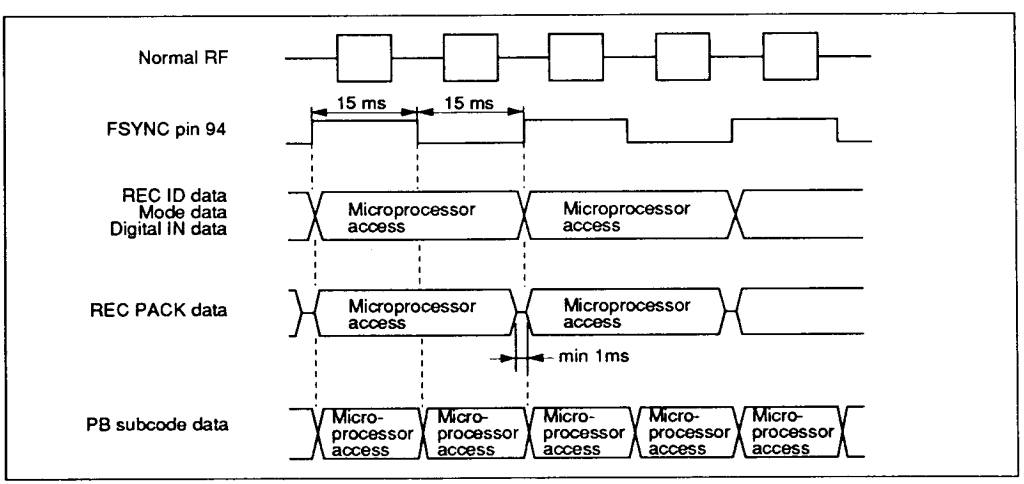


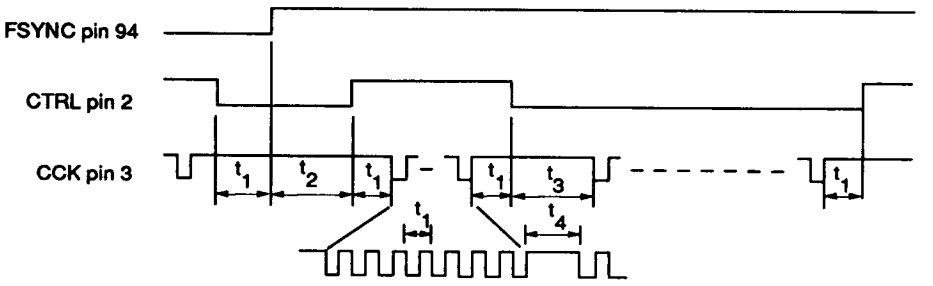
Figure 4 Microprocessor Access Timing

Transfer timing

Microproccessor accesses should strictly follow the timing of figure 5.

Transfer format

As shown in figure 6, data is input to CDATAI with the LSB first, but packed toward the MSB. Data will be output on CDATAO with the MSB first, but packed toward the LSB.



Symbol	Conditions	Min	Typ	Max	Unit
t_1	—	1	—	—	µs
t_2	Mode data EXS=1	100	—	—	µs
	All other	2	—	—	µs
t_3	CLDT="ITEM"	100	—	—	µs
	PB with CLDT="PACK"	20	—	—	µs
	All other	1	—	—	µs
t_4	CLDT="ITEM" or CLDT="PACK"	20	—	—	µs
	All other	1	—	—	µs

Figure 5 CTRL and CCK Timing

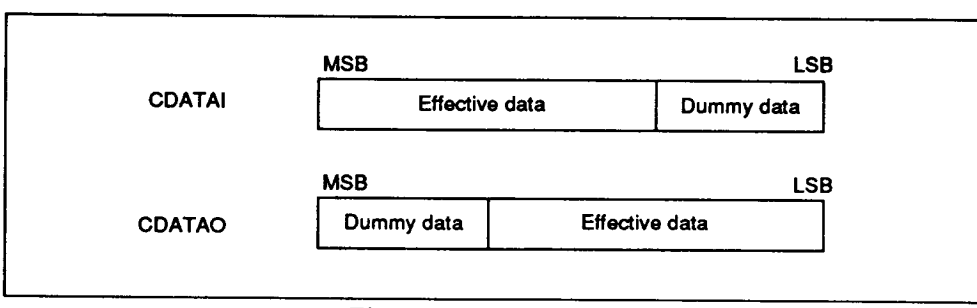


Figure 6 Transfer Format

Control data

Subcode data input/output and mode data input are specified with the format shown in figure 7. When transferring control data to the HD49211BFS signal processing LSI, CS must be "1". Also, having transferred CS="1", DOCTRL="1", and CLDT="OFF", another LSI will share the microprocessor port until the next FSYNC signal edge.

- **Selecting transfer data**

Transfer data is selected with the 3 bits of CLDT as shown in table 1.

Table 1 CLDT Data Specifications

CLDT	Name	Function	I/O			
2 1 0			Mode data RP			
			0	1	2	3
0 0 0	OFF	Don't Care	No Care	←	←	←
0 0 1	PCTL	Pack data output / Control data input	I	—	—	Don't Care
0 0 1	CBIT	Digital input / C bit data output	—	O	O	Don't Care
0 1 0	ITEM	Item table output	O	—	—	Don't Care
0 1 0	UBIT	Digital input / U-bit data output	—	O	O	Don't Care
0 1 1	PACK	Pack data I/O	O	I	I	I
1 0 0	MODE	Mode data input	I	I	I	I
1 0 1	PCM-ID	PCM-ID I/O	O	I	I	O
1 1 0	SUB-ID	SUB-ID I/O	O	I	I	I
1 1 1	TESTCK	Clock input for testing	I	I	I	I

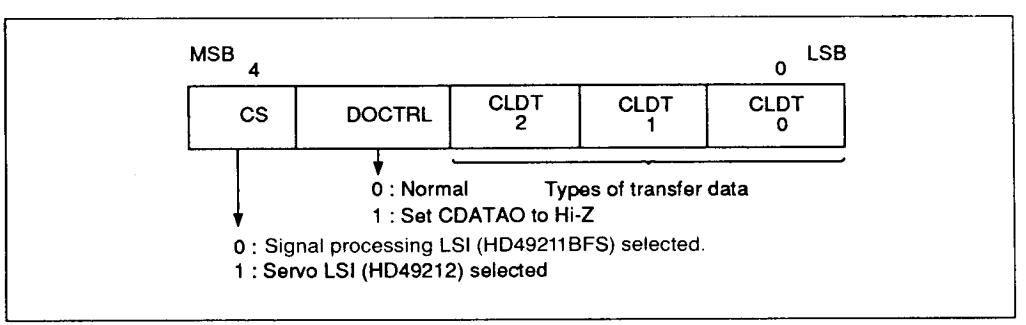


Figure 7 Control Data Format

- **Control data transfer timing**

(1) Mode data transfers

Figure 8 shows an example of a mode data transfer. Bring CTRL (pin 2) to "H" before transferring control data. Then, transfer CLDT="MODE" as control data, followed by 16 bits of mode data.

(2) Subcode data playback

Figure 9 shows an example of subcode data playback (mode data RP=0). Subcode data playback starts by reading the item table. The position of the pack storing the needed data is looked up, the pack is selected with PCTL, and then the pack is read.

More specifically, the CLDT="ITEM" control code is transferred, the item table is read, and the position of the pack storing the desired data is then determined by command. After CLDT="PCTL" is transferred, the pack to be read is specified according to the 6-bit PCTL. Finally, CLDT="PACK" is sent and the actual transfer of pack data begins.

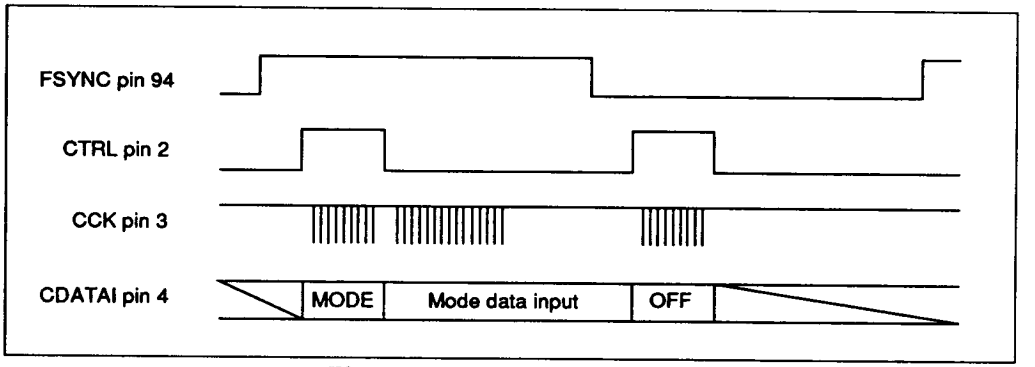


Figure 8 Mode Data Transfer

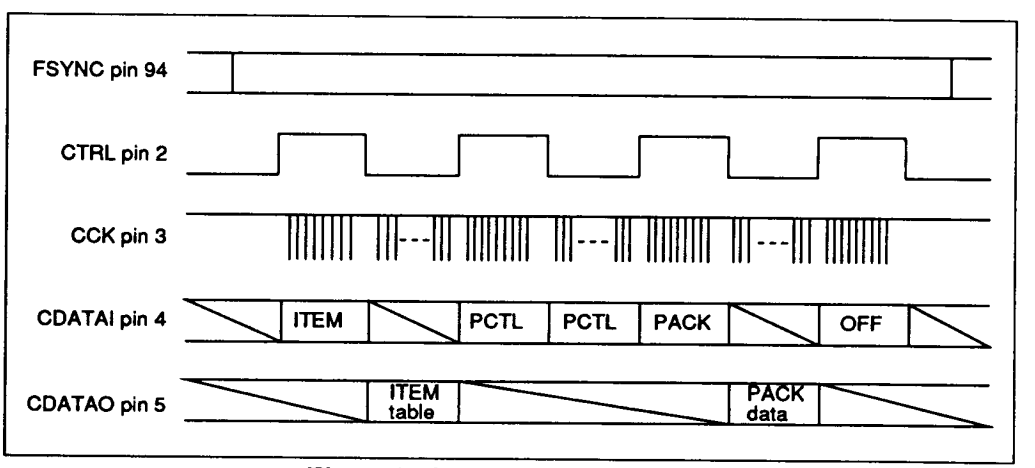


Figure 9 Subcode Data Playback

(3) Subcode data recording

Figure 10 shows an example of subcode data recording (mode data RP=2 or RP=3). The hardware will have previously set the pack data to all zeroes during recording. Input pack data is written in sequence at 16 packs per frame.
Data must be transferred every frame while recording pack data, but only the valid pack data has meaning.

- **MODE (Mode data)**

Mode data is the 16 bits that set the chip mode. To change the mode setting, new mode data is transferred.
The new setting becomes valid after the next rising edge of the FSYNC signal.
Bit 7 and 0 must be set to zero.

- **OFF**

Set this control code when there are no data communications between the signal processing LSI and the microprocessor, or when microprocessor access has ended as shown in figure 4.

- **ITEM (Item data table)**

This control code will output two blocks of item table pack data.

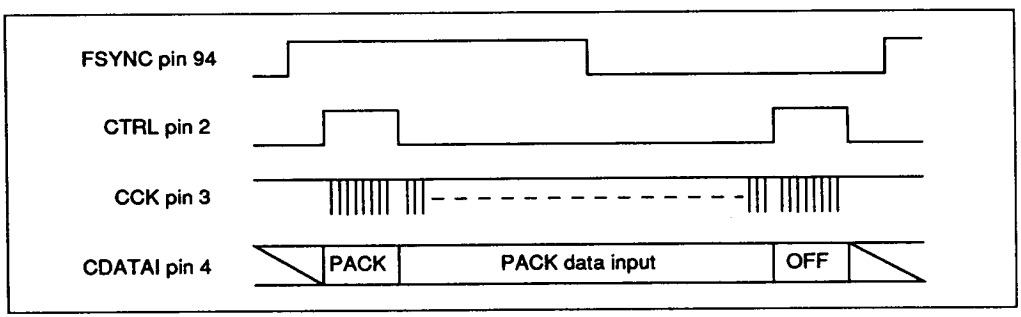


Figure 10 Subcode Data Recording

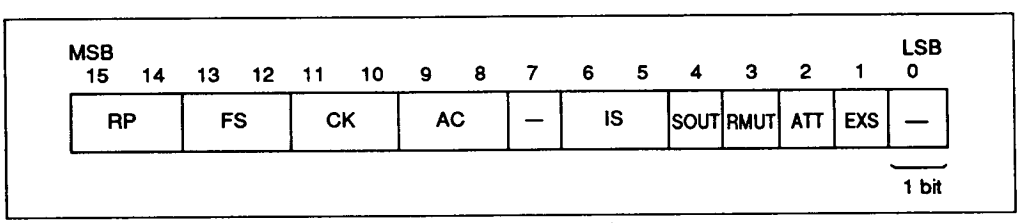


Figure 11 Mode data format

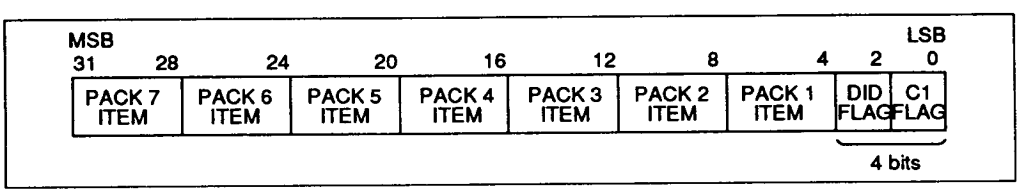


Figure 12 ITEM Table Format

C1 flag (C1 error correction result flag)
00 No correction
01 1 symbol corrected
10 2 symbols corrected
11 Correction impossible

DID flag
00 SUB-ID parity is ok, and DATA-ID=0
11 All other conditions

The relation between item table data and the type of data in the pack is shown in table 3.

Table 2 Mode Data Settings

Name	Function	Setting	Notes
RP	Recording/ playback switch	0 Playback	
		1 Monitor output for STOP/REC PAUSE, and lock verification of digital audio interface input	Chip mode is record, but record signal will not be output.
		2 Record	(Note 1)
		3 After-recording (PCM playback/subcode data record)	
FS	FS switch	0 48 kHz	(Note 1)
		1 44.1 kHz	
		2 32 kHz	
		3 Unused	
CK	Master clock switch	0 Internally generated 256 FS (384 FS if 32 k)	
		1 External clock input 256 FS (384 FS if 32 k)	
		2 Internally generated 512 FS (768 FS if 32 k)	
		3 External clock input 512 FS (768 FS if 32 k)	
AC	Playback operation switch	0 Normal playback	
		1 2/3-speed playback	Will playback areas with low error rates.
		2 Cue/Review	Will select and playback areas with low error rates, but phase velocity deviation will be within ±9.5% (Note 2)
		3 Approx. 200x-speed search	Drum revolution rate is 2000 rpm, but phase velocity deviation will be within ±9.5% (Note 2)
IS	Record data input switch	0 A/D input	HA12131MP, HA12132MP
		1 Serial input	
		2 Digital audio interface input	
		3 Unused	
SOUT	Digital audio interface control	0 Normal	Valid only when IS = 2 output and
		1 TX-through mode for other modes.	RP = 1 or 2. Set to zero.
RMUT	Record mute	0 Normal record	
		1 Record data all zeroes	No relation to monitor output.
ATT	Output attenuation	0 Normal output	
		1 Output data 12 dB lower	Valid also for monitor output during recording.
EXS	Frame synchronize control	0 Asynchronous	Will synchronize with frame sync in U-data during digital audio interface input.
		1 STRG synchronous STRG signal	Will synchronize to the (pin 93).

Notes: 1. Before starting recording (RP = 2), the stop mode (RP = 1) must be set for at least two frames. Also after changing FS, the stop mode must be set for at least two frames.
2. Phase velocity deviation is the deviation between the actual playback data and playback data taken at a standard data rate of 9.408 MHz.

The timing of references to two or more blocks of the item table is shown in figure 13.
With DATA-ID=0, the C1 flag will reference the item table's block pairs (0,0)B,(0,1)B,(1,0)B in sequence starting from block pair 8,9, and output them to the microprocessor. In this case, the C1 flag will skip the item table (1.1)B in its output.

Reference sequence: (8,9) → (A,B) → (C,D) → (E,F) → (0,1) → (2,3) → (4,5) → (6,7)

- **PCTL (Pack Control)**

This control code controls the output of pack data. For PCTL, packs which are to be read should have their corresponding bits be set to '1' and the others to '0'. Then during pack playback later, packs that have been set to '1' will be output in sequence.

Table 3 Relation of Pack Data with ITEM

ITEM	Data type	Notes
0 0 0 0	No data	PC1-PC7 are all 0.
0 0 0 1	Program time	Program no., index no., program time
0 0 1 0	Absolute time	Program no., index no., absolute time
0 0 1 1	Running time	Program no., index no., running time
0 1 0 0	TOC	TOC data
0 1 0 1	Date	Year, month, day, day of week, hour, minutes, seconds
0 1 1 0	Catalog	Catalog data
0 1 1 1	ISRC	International Standard Recording Code
1 0 0 0		
1 0 0 1		
1 0 1 0		
1 0 1 1	Reserved	—
1 1 0 0		
1 1 0 1		
1 1 1 0		
1 1 1 1		

- **PACK (Pack data)**

This control code indicates one pack of pack data.

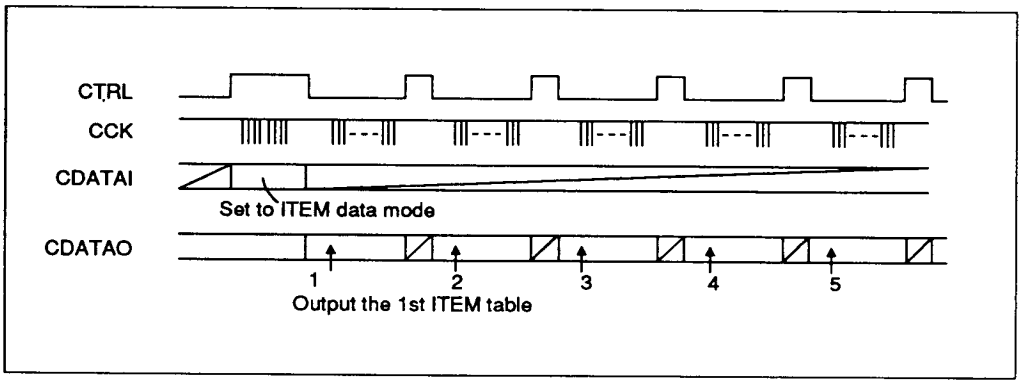


Figure 13 ITEM Table Read Timing

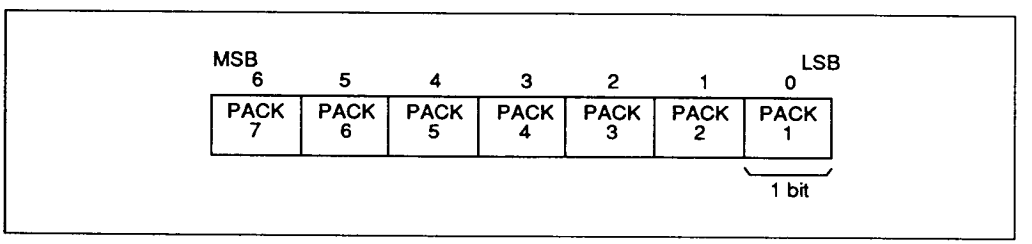


Figure 14 PCTL Format

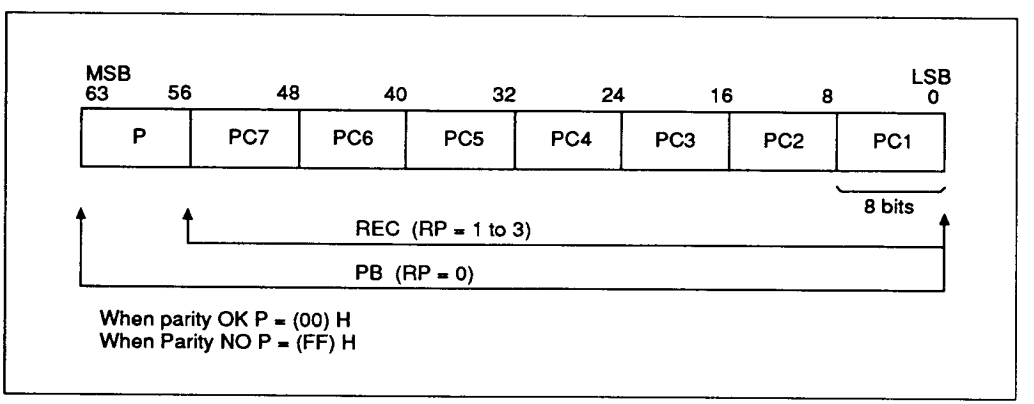
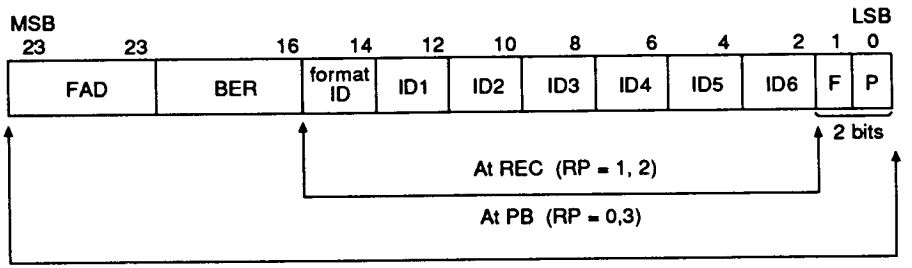


Figure 15 PACK Format

• **PCM-ID**

This control code is for inputting and outputting the PCM-ID, and for outputting the frame address and block error rate. When searching (mode data AC=3 and RP=0 or 3) the PCM-ID will not be played back. The HD49211BFS itself generates the frame address during recording (mode data RP=1 or 2), so the frame address cannot be specified. Also, do not make any accesses for 0.5 frames immediately after switching to playback (mode data RP=0) from any other mode (RP ≠ 0). Table 4 shows the contents of data in ID1-ID6.



Item	Playback operation	Notes
ID1 – ID6	Outputs data of one track that has been match-detected twice with parity ok.	Refer to figure 17.
P	0: Valid ID detected 1: Invalid ID detected	
FAD	Outputs data that has been match-detected from one track.	
F	1: Inconsistent FAD detected 0: All other cases	
BER	Single track block error rate	Refer to figure 18.

Figure 16 PCM-ID Format

Table 4 Contents of ID1-ID6

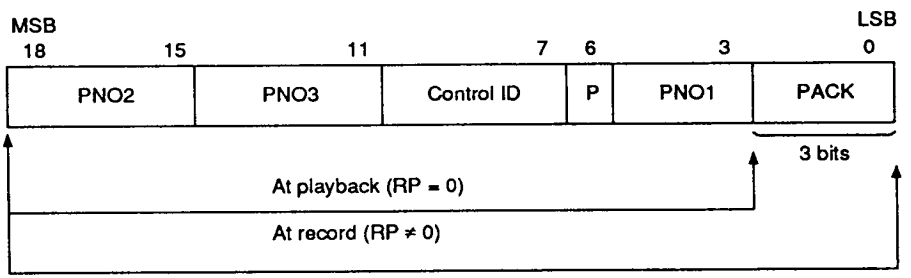
Name	Function	Setting	
ID1	Emphasis	0	Off
		1	50μ/15 μ
		2	Reserved
		3	
ID2	Sampling frequency	0	48 kHz
		1	44.1 kHz
		2	32 kHz
		3	Reserved
ID3	Channel number	0	2 channels
		1	4 channels
		2	Reserved
		3	
ID4	Sampling bits and format	0	16 bits straight-line
		1	12 bits non-straight-line
		2	Reserved
		3	
ID5	Track pitch	0	Normal track mode
		1	Wide track mode
		2	Reserved
		3	
ID6	Digital copy	0	Copying authorized
		1	Reserved
		2	Copying prohibited
		3	Reserved

Table 5 Relation of Error Number with BER (Block Error Rate)

BER	Error number	Block error rate
0	0–7	0.00–005
1	8–15	0.06–0.12
2	16–23	0.13–0.18
3	24–31	0.19–0.24
4	32–39	0.25–0.30
5	40–47	0.31–0.37
6	48–55	0.38–0.43
7	56–63	0.44–0.49
8	64–71	0.50–0.55
9	72–79	0.56–0.62
A	80–87	0.63–0.68
B	88–95	0.69–0.74
C	96–103	0.75–0.80
D	104–111	0.81–0.87
E	112–119	0.88–0.93
F	120–128	0.94–1.00

• **SUB-ID**

During recording (mode data RP ≠ 0), always write 0 into bit 6 "P".
During playback (mode data RP=0), bits 0-2 "PACK" will not be detected.
During searching (mode data AC=3), if Control-ID and PN0 of SUB-ID are not detected properly, bit 6 "P" will be set.
Also, do not make any accesses for 0.5 frames immediately after switching to playback (mode data RP=0) from any other mode (RP≠0).



Item	Description	Playback operation
PNO 1 – 3	Contains the program number in BCD, with the most significant digit in PN01, the middle in PN02, and the least in PN03.	Mode data AC≠3: For SUB1 or SUB2, outputs data that has been match-detected twice with parity ok. AC=3: Outputs data that has been match-detected against both PNO and control-ID, with parity OK. (Note 1)
Control ID	Each bit shows the existence of data or a flag setting. Bit 7:TOC ID Bit 8:Shortening ID Bit 9:Start ID Bit 10:Priority ID (PN0)	
P	0: Detection ok 1: Detection bad	Set to "1" if match-detection is bad. (Note 2)
PACK	Indicates pack number (0 – 7).	Does not detect

Notes: 1. During searching (AC = 3), checks that either control-ID matches four times or PNO matches twice within three FSYNC cycles.
2. When AC = 3, ;the P bit is set to 0 if both control-ID matches four times and PNO matches twice.

Figure 17 Contents of SUB-ID Formats

• **C-BIT**

This is the C-bit data output of the digital audio interface data input. For details please refer to the digital audio interface block.

• **U-BIT**

This is the U-bit data of the digital audio interface data input. For details please refer to the digital audio interface block.

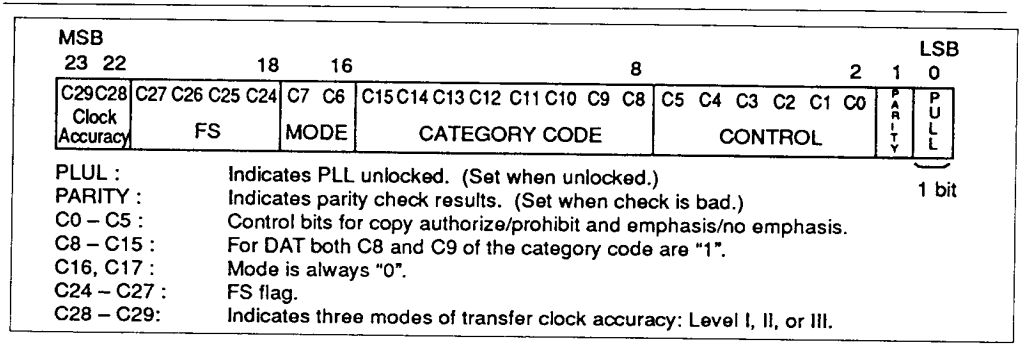


Figure 18 C-bit Format

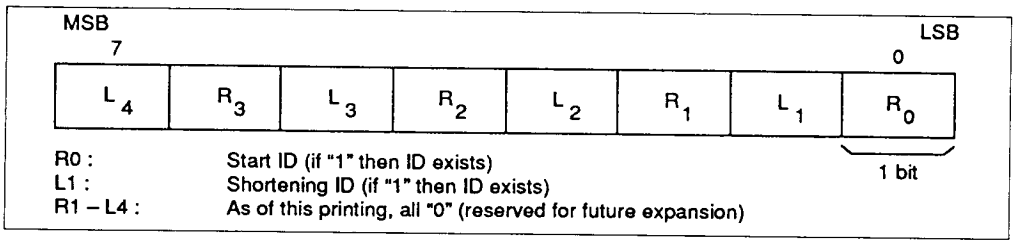


Figure 19 U-bit format

Level meter data output

Level meter data is output within half of the FSYNC signal period (15 ms). The largest absolute values of both the left and right channels will be output.

- **Overflow detect bit**

This bit is set when the 16-bit audio data is converted to an absolute value and excluding the upper bit, all 15 bits are "1".

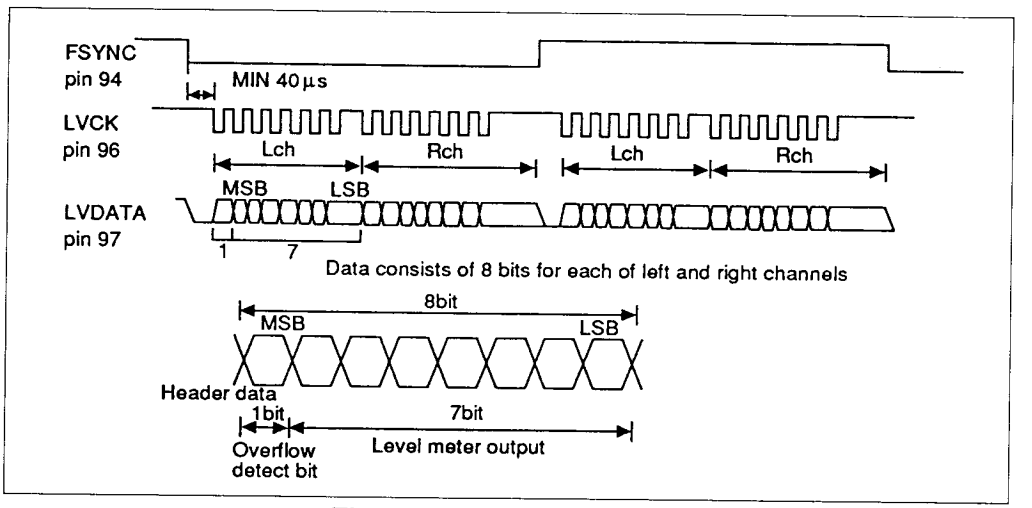


Figure 20 Level meter output

HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

Table 6 Levels of Level Meter Data

Level meter data	Level	Logical values			
7F	0	(0.00	—	−0.56	)
7E	−1	(−0.56	—	−1.16	)
7D	−2	(−1.16	—	−1.80	)
7C	−2	(−1.80	—	−2.50	)
7B	−3	(−2.50	—	−3.25	)
7A	−4	(−3.25	—	−4.08	)
79	−5	(−4.08	—	−5.00	)
78	−6	(−5.00	—	−6.02	)
77	−6	(−6.02	—	−6.58	)
76	−7	(−6.58	—	−7.18	)
75	−8	(−7.18	—	−7.82	)
74	−8	(−7.82	—	−8.52	)
73	−9	(−8.52	—	−9.28	)
72	−10	(−9.28	—	−10.10	)
71	−11	(−10.10	—	−11.02	)
70	−12	(−11.02	—	−12.04	)
6F	−12	(−12.04	—	−12.60	)
6E	−13	(−12.60	—	−13.20	)
6D	−14	(−13.20	—	−13.84	)
6C	−14	(−13.84	—	−14.54	)
6B	−15	(−14.54	—	−15.30	)
6A	−16	(−15.30	—	−16.12	)
69	−17	(−16.12	—	−17.04	)
68	−18	(−17.04	—	−18.06	)
67	−18	(−18.06	—	−18.62	)
66	−19	(−18.62	—	−19.22	)
65	−20	(−19.22	—	−19.87	)
64	−20	(−19.87	—	−20.56	)
63	−21	(−20.56	—	−21.32	)
62	−22	(−21.32	—	−22.14	)
61	−23	(−22.14	—	−23.06	)
60	−24	(−23.06	—	−24.08	)
5F	−24	(−24.08	—	−24.64	)
5E	−25	(−24.64	—	−25.24	)
5D	−26	(−25.24	—	−25.89	)
5C	−26	(−25.89	—	−26.58	)
5B	−27	(−26.58	—	−27.34	)
5A	−28	(−27.34	—	−28.16	)
59	−29	(−28.16	—	−29.08	)
58	−30	(−29.08	—	−30.10	)
57	−30	(−30.10	—	−30.66	)
56	−31	(−30.66	—	−31.26	)
55	−32	(−31.26	—	−31.91	)
54	−32	(−31.91	—	−32.60	)
53	−33	(−32.60	—	−33.36	)
52	−34	(−33.36	—	−34.19	)
51	−35	(−34.19	—	−35.10	)
50	−36	(−35.10	—	−36.12	)

Level meter data	Level	Logical values			
4F	−36	(−36.12	—	−36.68	)
4E	−37	(−36.68	—	−37.28	)
4D	−38	(−37.28	—	−37.93	)
4C	−38	(−37.93	—	−38.62	)
4B	−39	(−38.62	—	−39.38	)
4A	−40	(−39.38	—	−40.21	)
49	−41	(−40.21	—	−41.12	)
48	−42	(−41.12	—	−42.14	)
47	−42	(−42.14	—	−42.70	)
46	−43	(−42.70	—	−43.30	)
45	−44	(−43.30	—	−43.95	)
44	−44	(−43.95	—	−44.64	)
43	−45	(−44.64	—	−45.40	)
42	−46	(−45.40	—	−46.23	)
41	−47	(−46.23	—	−47.14	)
40	−48	(−47.14	—	−48.16	)
3F	−48	(−48.16	—	−48.73	)
3E	−49	(−48.73	—	−49.32	)
3D	−50	(−49.32	—	−49.97	)
3C	−50	(−49.97	—	−50.66	)
3B	−51	(−50.66	—	−51.42	)
3A	−52	(−51.42	—	−52.25	)
39	−53	(−52.25	—	−53.16	)
38	−54	(−53.16	—	−54.19	)
37	−54	(−54.19	—	−54.75	)
36	−55	(−54.75	—	−55.35	)
35	−56	(−55.35	—	−55.99	)
34	−56	(−55.99	—	−56.68	)
33	−57	(−56.68	—	−57.44	)
32	−58	(−57.44	—	−58.27	)
31	−59	(−58.27	—	−59.18	)
30	−60	(−59.18	—	−60.21	)
2F	−60	(−60.21	—	−60.77	)
2E	−61	(−60.77	—	−61.37	)
2D	−62	(−61.37	—	−62.01	)
2C	−62	(−62.01	—	−62.70	)
2B	−63	(−62.70	—	−63.46	)
2A	−64	(−63.46	—	−64.29	)
29	−65	(−64.29	—	−65.20	)
28	−66	(−65.20	—	−66.23	)
27	−66	(−66.23	—	−66.79	)
26	−67	(−66.79	—	−67.39	)
25	−68	(−67.39	—	−68.03	)
24	−68	(−68.03	—	−68.73	)
23	−69	(−68.73	—	−69.48	)
22	−70	(−69.48	—	−70.31	)
21	−71	(−70.31	—	−71.22	)
20	−72	(−71.22	—	−72.25	)
1E	−73	(−72.25	—	−73.41	)
1C	−74	(−73.41	—	−74.75	)
1A	−76	(−74.75	—	−76.33	)
18	−78	(−76.33	—	−78.27	)
14	−80	(−78.27	—	−80.77	)
10	−84	(−80.77	—	−84.29	)
08	−90	(−84.29	—		)

Record/Playback Block

Block Overview

This block switches between recording and playback and generates the appropriate timing.

Block Function

I/O Pins

- **PDATA (pin 20) and PDCK (pin 21)**

These are inputs for playback data and the playback data synchronizing clock from the data strobe circuit. Use of the HA12062AMP for the data strobe circuit is assumed.

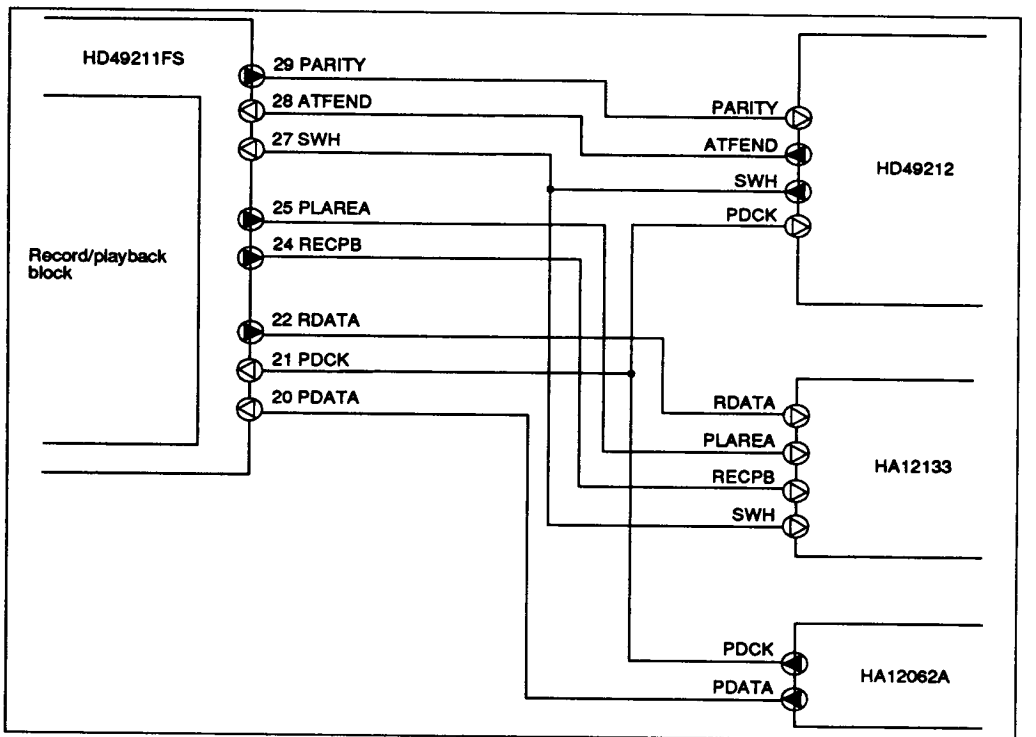


Figure 21 Record/Playback Block I/O Pins

Mode data	PDATA operation
RP= 0	Playback signal input
1	Don't care
2	Don't care
3	Playback signal input

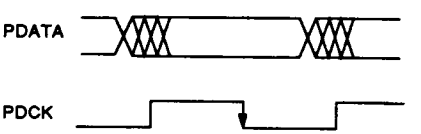


Figure 22 PDATA and PDCK timing

HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

- FCHI (pin 8)

This is the standard clock output of the record/playback block. Connect it to FCH (pin 7).

- PARITY (pin 29)

This pin outputs the parity check results during playback.

- RDATA (pin 22)

This pin outputs the record signal during recording (mode data RP=2 or 3).

- RECPB (pin 24)

This is the signal output indicating switching between record and playback

- PLAREA (pin 25)

This is the pilot signal area output during recording. It is used for controlling the recording current.

- SWH (pin 27)

This is reference signal input of the recording signal output position. The input comes from the servo LSI (HD49212).

- ATF END (pin 28)

This signal is used for determining the area position during playback (after-recording). Its input comes from the servo LSI (HD49212).

Table 7 Parity check results

Operating mode		Pin state
Mode data	Parity ok	H
RP=0 or 3	Parity bad	L
Mode data RP = 2		L

Table 8 RDATA Output Signal

Operating mode		Output data
Recording signal	Within area	Outputs record
	Out of area	Outputs 4.7 MHz
Playback		L

Note: The start of record signal output usesone frame after the mode change.

Table 9 RECPB Output Signal

Mode data	Output data
RP = 0,1	L
RP = 2	H
RP = 3	H: record L: playback

Table 10 PLAREA Output Signal

Mode data	Output signal
RP = 2	H: Within pilot signal area L: Out of pilot signal area
RP ≠ 2	L

Table 11 SWH Operation

Mode data	Operation
RP = 2	Determines reference position on rising edge.
RP ≠ 2	Don't care

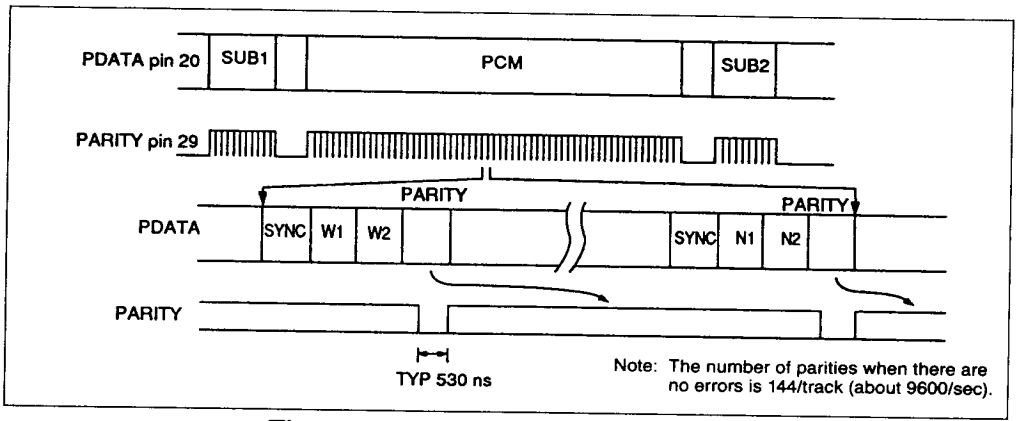


Figure 23 Parity Results Output Timing

Signal timing

- **Record/playback area margin**

Correct recording and playback are possible if the record and playback signals have deviations against FSYNC (pin 94) as shown below.

Table 12 Record/Playback Area Margin

PDATA 20 Pin	±45°	
RDATA 22 Pin	+55°	–45°

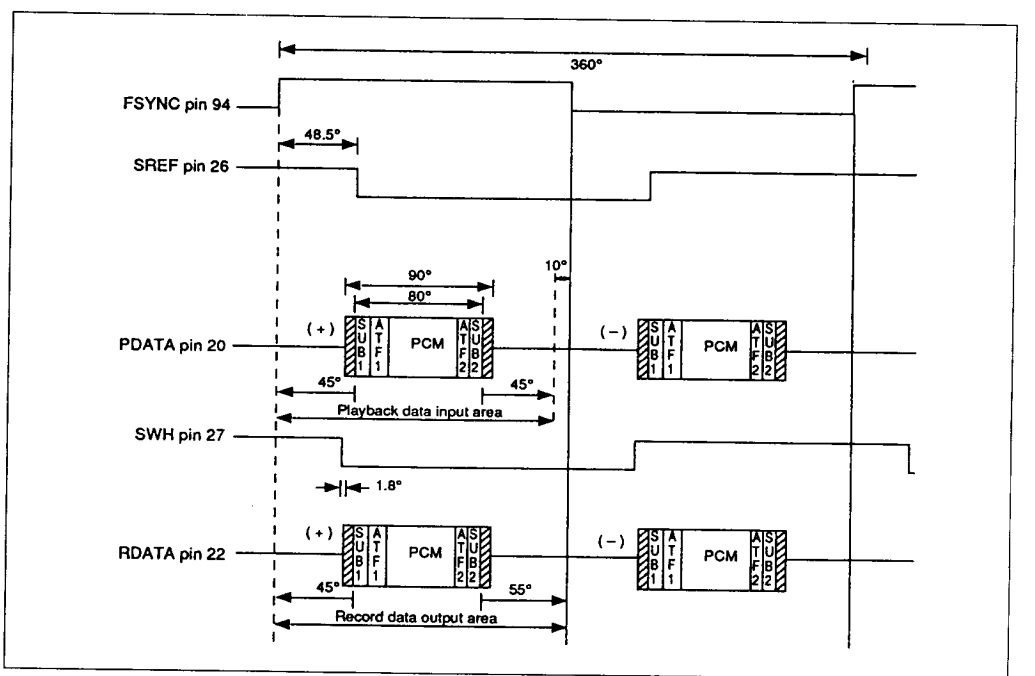


Figure 24 Input/Output Timing of Record/Playback Signals

HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

- **Subcode after-recording**

Subcode recording during after-recording (mode data RP=3) is performed with the timing of figure 25.

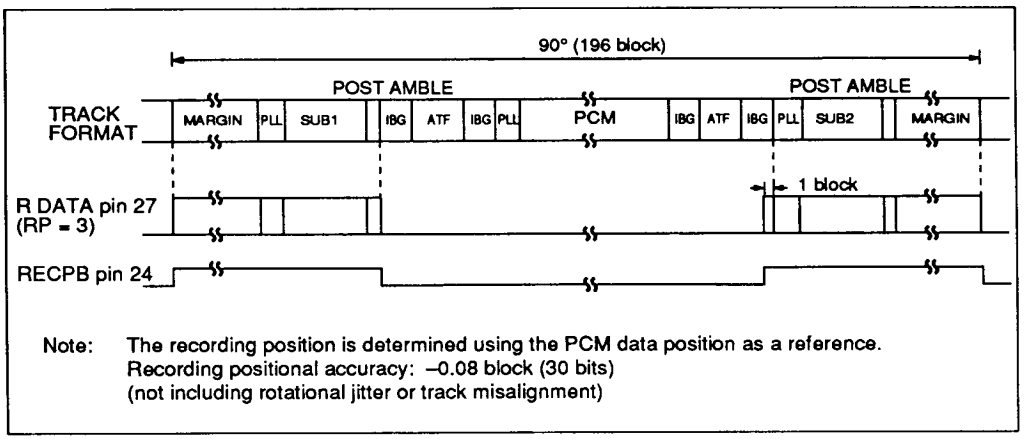


Figure 25 After-recording Timing

- **STOP mode (mode data RP=1)**

When recording, the record mode must be entered after one occurrence of the stop mode. The time required for the stop mode is at least two frames (60 ms).

Actual recording is shown in figure 26. PCM data is input starting 1/2 frame (15 ms) before switching from stop mode to record mode. One frame (30 ms) after that recording begins.

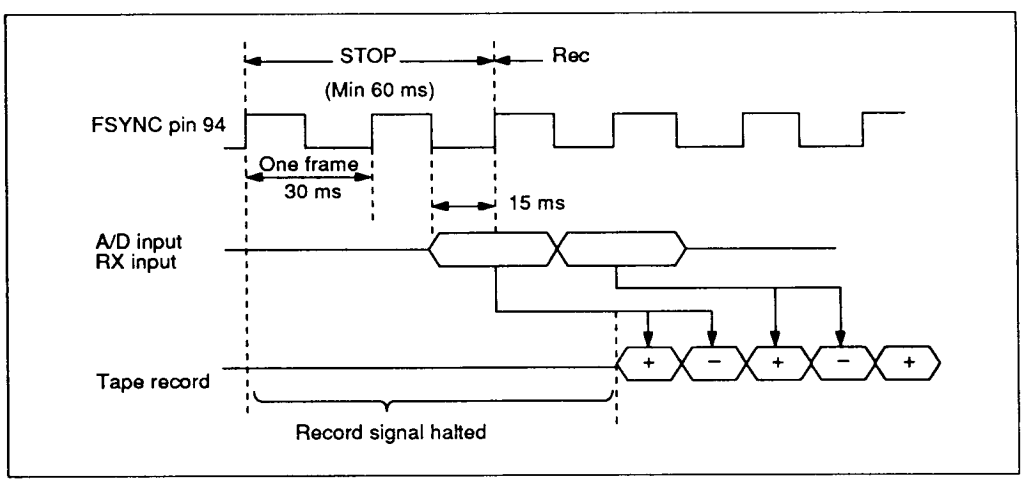


Figure 26 Input data recording Timing

- **PCM data, subcode, ID record/playback timing**

(1) REC (RP =2)

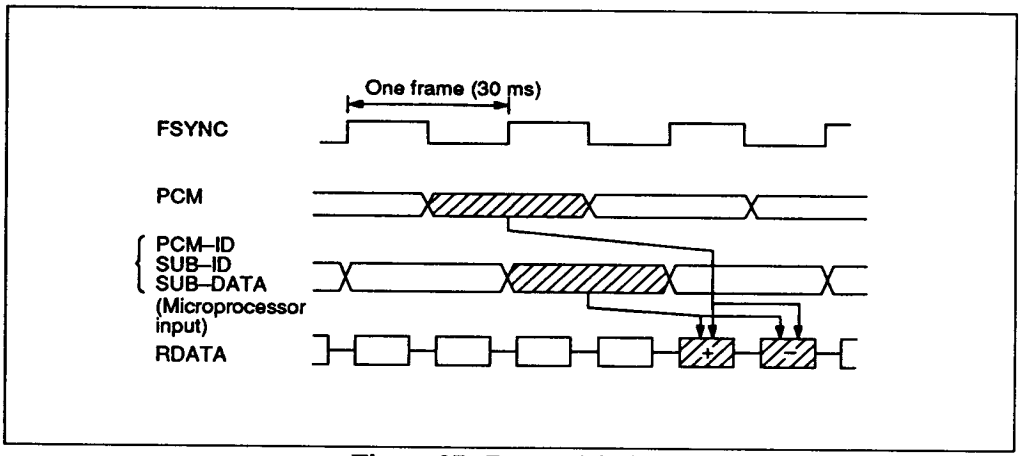


Figure 27 Record Timing

(2) PLAY (RP = 0)

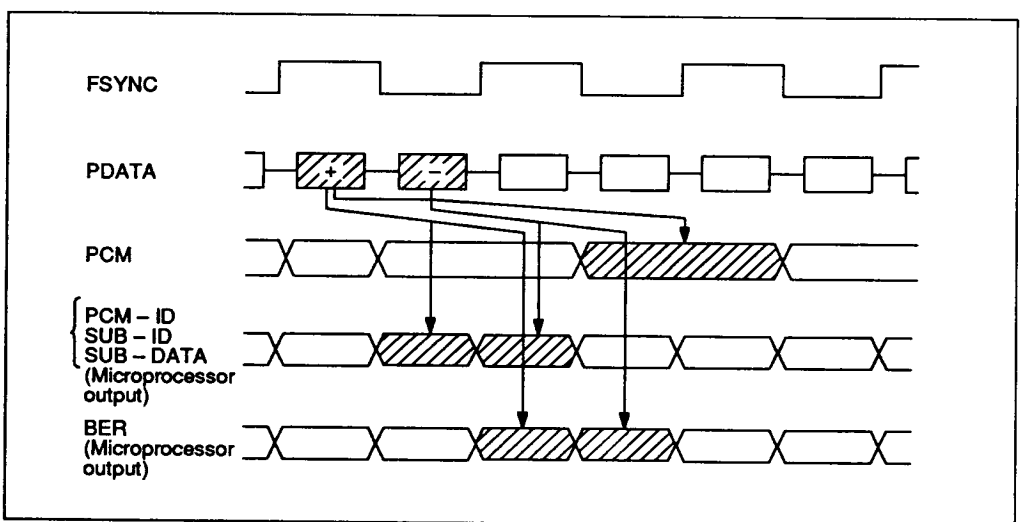


Figure 28 Playback Timing

(3) AFTER – RECORDER (RP =3)

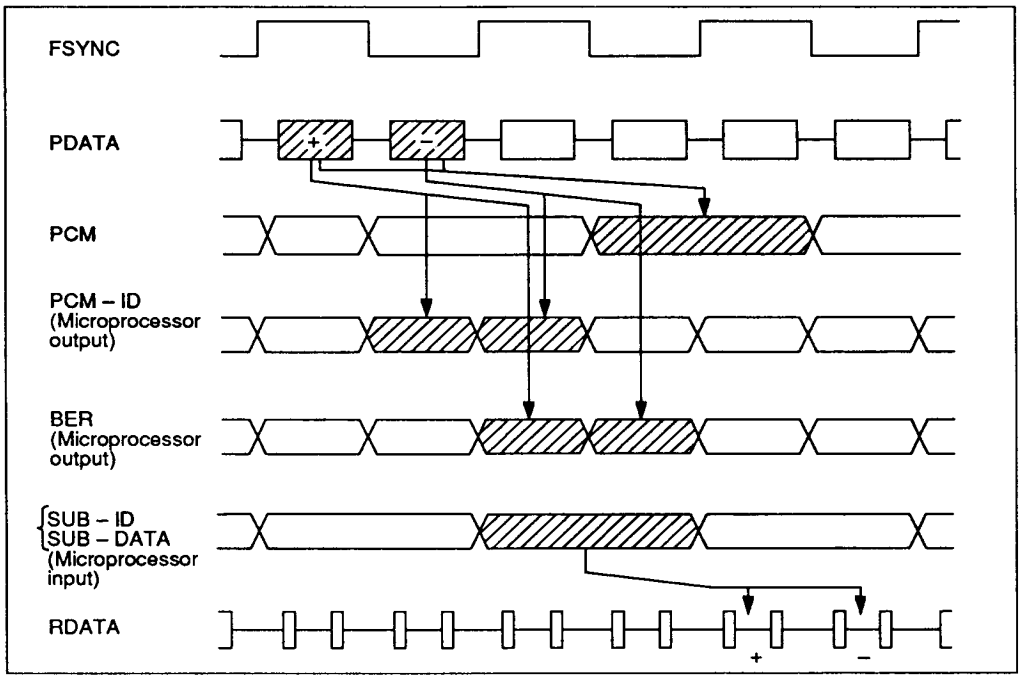


Figure 29 Post-score Timing

- **Variable-speed playback and high-speed search**

The settings for variable-speed playback and high-speed search depend on the state of mode data AC.

- **Output data table**

Table 14 shows the output data for each mode.

Table 13 Variable-Speed Playback and High-Speed Search Operations

Mode data AC	Tape speed	SYNC *2 maintenance	PCM-ID playback	SUB-ID playback	PCM DATA playback	SUB DATA playback
0	Normal playback	Normal	Normal	Normal	Normal	Normal
1	— ×3*1	↑	↑	↑	Area-select playback	↑
2	— ×30	OFF	↑	↑	↑	↑
3	— ×200	↑	Halted	All areas detected	Halted	All areas detected

Notes: 1. Reverse ×3 uses mode 2.
2. Checking for SYNC continuity.

Table 14 Output Data Table

OUTPUT	MODE DATA	RP=0	IS=0 RP=1	IS=0 2	IS=1 1	IS=1 2	IS=2 1	IS=2 2	RP=3
RDATA	PCM	—	—	A/D	—	SIN	—	RX	—
	PCM ID	—	—	Micro-processor	—	Micro-processor	—	Micro-processor	—
	SUB ID	—	—	Micro-processor	—	Micro-processor	—	Micro-processor	Microprocessor
	SUB DATA	—	—	Micro-processor	—	Micro-processor	—	Micro-processor	Microprocessor
D/A (INHL.R=H)	PB	—		—		RX		PB	
SOUT (INHL.R=L)		PB	A/D		SIN		RX		PB
TX (SOUT=0)	PCM	PB	A/D		SIN		RX		PB
	C-bit	PB	Microprocessor *		←		←		PB
	U-bit	PB	Microprocessor *		←		←		Microprocessor
	SUB DATA	—	—		—		—		—
TX (SOUT=1)	PCM	—	—		—		RX	through	—
	C-bit	—	—		—		RX	through	—
	U-bit	—	—		—		RX	through	—
	SUB DATA	—	—		—		RX	through	—
UDATA		—	—		—		RX	through	—
Micro-processor	PCM ID	PB	—		—		—		PB
	SUB ID	PB	—		—		—		—
	SUB DATA	PB	—		—		—		—
	U-bit	—	—		—		RX		—
	C-bit	—	—		—		RX		—

* Generated from microprocessor input ID data.

Interpolation Block

Block Overview

This block performs previous-value hold interpolation or average-value interpolation, according to the results of error correction. It also performs mute processing through the MUTE pin and during variable-speed playback.

Block Function

Interpolation processing

The following two types of interpolation are performed independently for the left and right channels:

(1) Previous-value hold interpolation

If two or more consecutive data errors exist, then the error-free value before the first data error will be output in place of each data error.

(2) Average-value interpolation

If only one data error exists, then the average value of the data immediately before and immediately after the error will be output instead.

Playback mute

The state of the MUTE pin can cause the playback output signal to mute. It can also mute the monitor signal during recording.

(1) During normal playback (mode data AC=0), zero-cross mute and feed mute are performed. When MUTE (pin 1) is brought to "H", mute processing will begin. Then the chip waits for a fixed time until the upper 8 bits of data become all "0" or all "1". When this data is detected, it and all subsequent data will be forced to all "0" (left and right channels independently). If this condition cannot be detected in the fixed time, then immediately after the time elapses a feed-out mute begins.

When MUTE is brought to "L" and mute is released, then only a feed-in mute will be performed.

(2) During variable-speed playback (mode data AC=1 or 2), feed mute only will be performed. Mute control is accomplished by O Ring MUTE (pin 1) on-chip with internal signals.

Record mute

Record muting is controlled by RMUT (3-bit mode data). When "H", the recording PCM signal will be muted. However, only zero-cross muting will be performed.

However, the monitor output is controlled by MUTE (pin 1) with no relation to RMUT.

Table 15 Mute Functions

MUTE pin	Function
"0"	Output the playback output signal (monitor signal)
"1"	Output all "0"

RAM Control Block

Block Overview

This block controls the RAM and generates addresses for reading and writing. A 256k-bit SRAM or pseudo-SRAM can be used.

Block Function

Figure 30 is an example of interfacing to an SRAM or pseudo-SRAM. Figure 31 shows read and write timing.

The use of the HM62256-8/10/12/15 SRAM or the HM65256B-12 pseudo-SRAM is recommended.

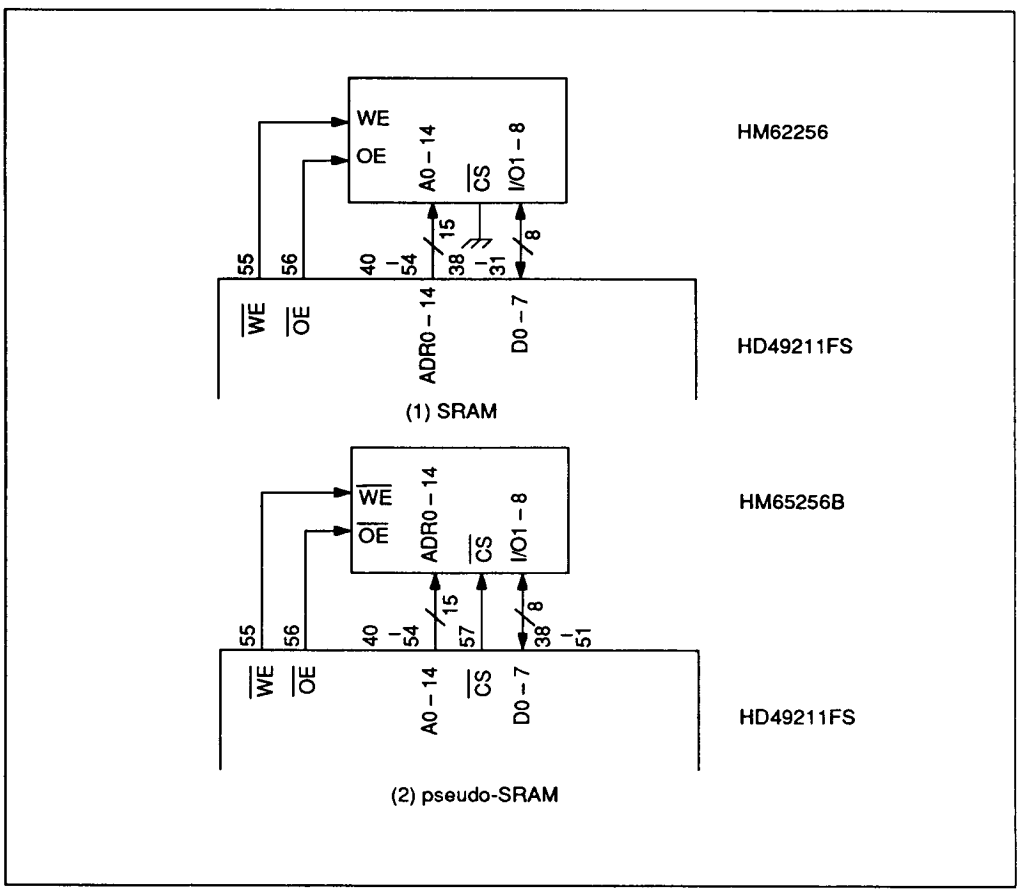
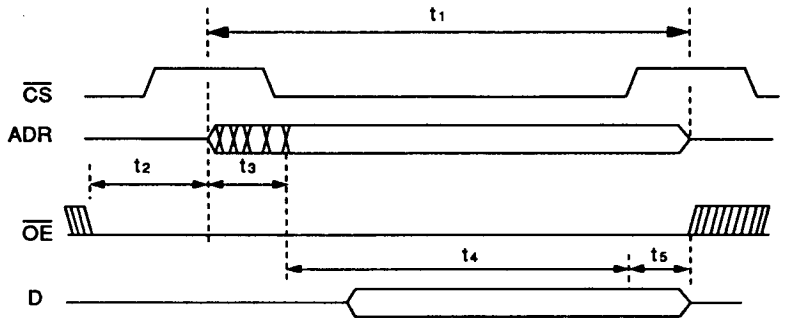
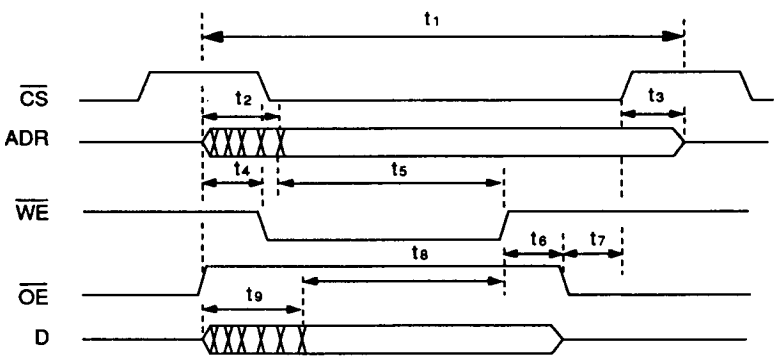


Figure 30 RAM Connection Diagram



(1) Read Timing

Symbol	Value	Unit	Symbol	Value	Unit
t1	320	ns	t4	255	ns
t2	80		t5	40	
t3	25				



(2) Write Timing

Symbol	Value	Unit	Symbol	Value	Unit
t1	320	ns	t6	40	ns
t2	25		t7	40	
t3	40		t8	165	
t4	20		t9	35	
t5	175				

Figure 31 RAM Timing

Timing Generation Block

Block Overview

This block consists of three types of crystal oscillator circuits as well as an external clock input.

Crystal oscillator circuits

OSC1: 12.288 MHz
This is 256 FS for a 48 kHz sampling frequency, 384 FS for a 32 kHz sampling frequency.
OSC2: 11.2896 MHz
This is 256 FS for a 44.1 kHz sampling frequency.
OSC3: 37.632 MHz

External clock input

When mode data CK = 1, the clock input from EXCK (pin 85) will become valid.

Block Function

Clock specifications

(1) OSC1, OSC2, EXCK

These are master clocks, which generate the main timing and FS-derived timing.

(2) OSC3

OSC3 is used as the clock for A/D-D/A control and RX modulation as well as for generating FCH (pin 7).

Mode settings

- **CK**

The mode data CK switches between OSC1, OSC2, and EXCK.

Table 16 Clock Specifications (1)

Clock	Frequencies	FS
OSC 1	12.288/24.576 MHz	48 k, 32 k
OSC 2	11.2896/22.5792 MHz	44.1 k
EXCK	12.288/24.576 HMz	48 k, 32 k
	11.2896/22.5792 MHz	44.1 k

Notes: 1. Operate each clock with a duty cycle as close to 50% as possible.
2. The Vth for the EXCK input is a TTL level.

Table 17 Clock Specifications (2)

Clock	Frequencies
OSC 3	37.632 MHz

Note: Operate the clock with a duty cycle as close to 50% as possible.

Table 18 Operation of Mode Data CK

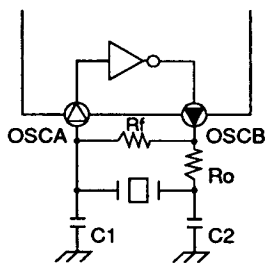
Mode setting		Operation			OSC 1	OCS 2	EXCK
	FS = 0	48 k		256 FS	[12 M]	×	—
CK = 1	1	44.1 k		256 FS	×	[11 M]	—
	2	32 k		384 FS	[12 M]	×	—
	FS = 0	48 k	EXCK input	256 FS	×	×	[12 M]
CK = 1	1	44.1 k	EXCK input	256 FS	×	×	[11 M]
	2	32 k	EXCK input	384 FS	×	×	[12 M]
	FS = 0	48 k		512 FS	[24 M]	×	—
CK = 2	1	44.1 k		512 FS	×	[22 M]	—
	2	32 k		768 FS	[24 M]	×	—
	FS = 0	48 k	EXCK input	512 FS	×	×	[24 M]
CK = 3	1	44.1 k	EXCK input	512 FS	×	×	[22 M]
	2	32 k	EXCK input	768 FS	×	×	[24 M]

[ ]: Oscillator frequency × : Oscillation halted —: Don't care

Oscillator circuit connections

Examples of external oscillator circuit connections are shown below for OSC1 – 3 using crystals from Kinseki, Ltd.

- **Fundamental frequency oscillator (OSC1 and OSC2)**

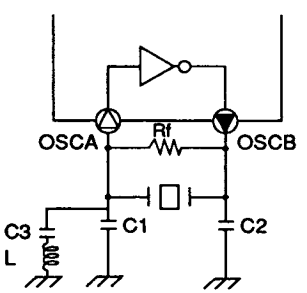


HC-49/u

Frequency	Rf	R0	C1	C2
11.2896 MHz	1 MΩ	680 Ω	18 pF	18 pF
12.288 MHz				

Figure 32 Fundamental Frequency Oscillator Circuit Example

- **Third high harmonic oscillator (OSC3)**



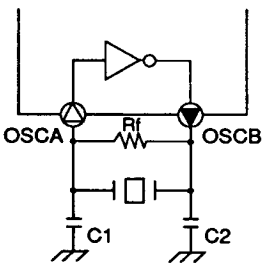
HC-49/u

Frequency	Rf	C1	C2	C3	L
37.632 MHz	1 MΩ	10 pF	10 pF	100 pF	3.3 µH

Figure 33 Third Harmonic Oscillator Circuit Example

Further examples of external oscillator circuit connections are shown below for OSC1-3 using crystals from Nippon Denpa Kogyo, Ltd.

- **Fundamental frequency oscillator (OSC1 and OSC2)**

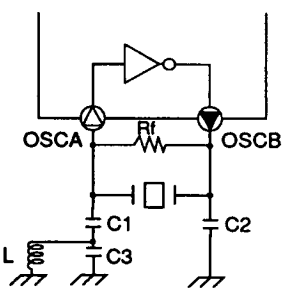


AT-51 LN-P-0002

Frequency	Rf	C1	C2
11.2896 MHz	1 MΩ	20 pF	20 pF
12.288 MHz			

Figure 34 Fundamental Frequency Oscillator Circuit Example

- **Third high harmonic oscillator (OSC3)**



NR-18 LN-X-0008J

Frequency	Rf	C1	C2	C3	L
37.632 MHz	1 MΩ	1000 pF	10 pF	22 pF	1 μH

Figure 35 Third Harmonic Oscillator Circuit Example

If inputting an external clock at TTL levels, connect as shown in figure 37.
When oscillation of OSC1 or OSC2 is halted, it will be shorted to a "L" level. If an external clock is then input note that no DC current will flow.

External clock preservation

When in external clock mode (mode data CK0=1) and EXCK (pin 85) is stopped, the crystal will automatically be made to oscillate, preventing the chip from ceasing operation.
While the preservation circuit is operating, the chip itself will not be operating correctly. When EXCK is not input, mode data must be set again, or else incorrect operation may result. Further, if EXCK is brought to a Hi-Z state, the protection circuit may also cause incorrect operation.

Table 19 MCK Output

Mode data		Output clock
CK	0	OSC 1 or OSC 2
	1	EXCK
	2	OSC 1 or OSC 2 × 1/2
	3	EXCK × 1/2

Output pins

- **MCK (pin 86)**

This pin outputs the master clock.

- **FCH (pin 7)**

This pin outputs the clock for FCHi (pin 8) and the servo LSI (HD49212).

Input pin

- **STRG (pin 73)**

This pin causes synchronization when mode data EXS=1.

Table 20 FCH Output Signal

Output	9.408 MHz (OSC 3 × 1/4)

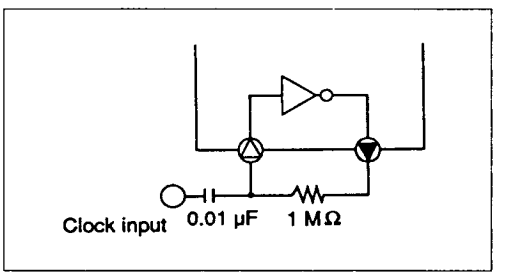


Figure 36 External Clock Input Circuit

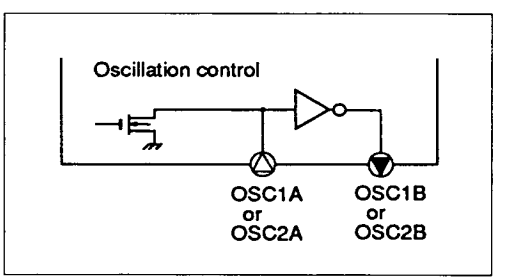


Figure 37 Clock Pin Internal Equivalent Circuit

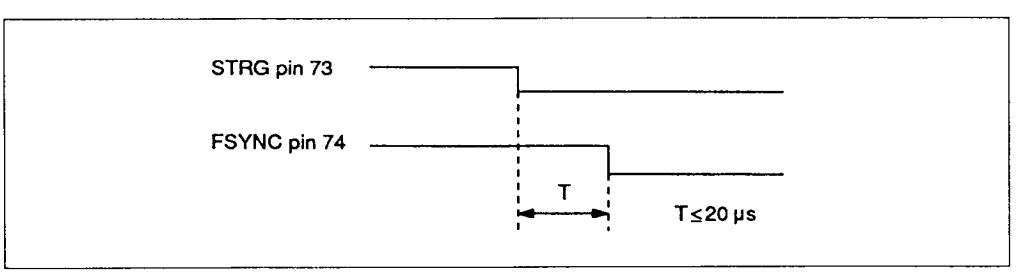


Figure 38 Relation Between STRG and FSYNC

Error Correction Block

Block Overview

This block performs standard DAT-format parity processing.
DAT parity codes use a Reed-Solomon coding method. First the 16-bit data of each cylinder revolution (30 ms) is divided into its upper and lower 8 bits. It is then formatted and interleaved. This block generates C1 and C2 parity and corrects errors in the interleaved data groups.

Block Function

Error correction functions

- **Special error correction method**

DAT uses a special 2-fold Reed-Solomon coding. Thus, this block generates C1 and C2 Reed-Solomon codes and appends them to data input from the A/D converter. C1 is actually 4 error correction symbols appended to 28 symbols of PCM data of 1 block, while C2 is 6 error correction symbols appended to 26 symbols of PCM data in a 4-block space.

- **Error correction processing.**

(1) C1 correction

Within the 28 symbols of one block, C1 corrects errors of up to 2 symbols in any arbitrary position. The correction is indicated by the setting of the C1 flag.

(2) C2 correction

Within 26 symbols extending over multiple blocks, C2 corrects errors of up to 2 symbols in any arbitrary position, or of up to 6 symbols if their positions are known.

Error correction monitor function

Error correction status can be monitored from FLAG (pin 18) during playback and after-recording.

- **FLAG (pin 18) I/O conditions**

(1) C1 correction of PCM or subcode data
.....Becomes "H" when error is detected.
(2) C2 correction of PCM data
.....Becomes "H" when error is detected.

- **Output timing**

Figure 39 shows FLAG output timing.

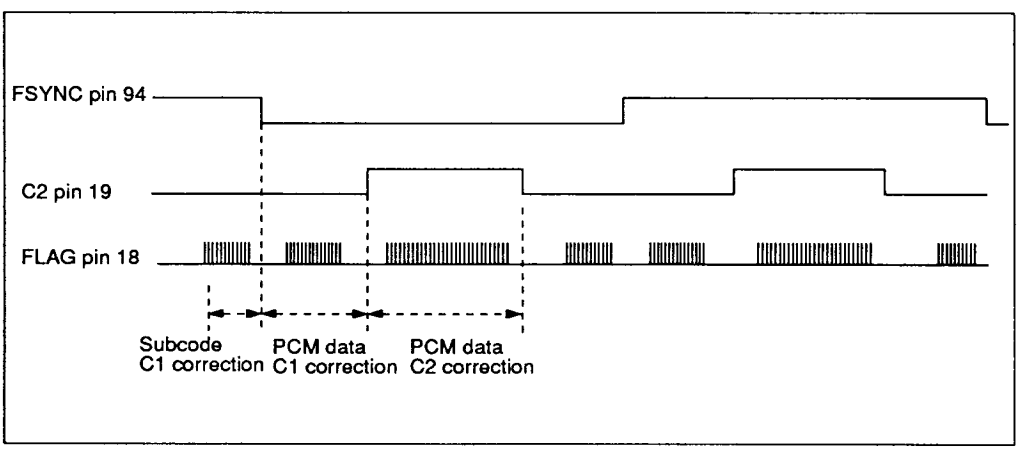


Figure 39 FLAG Output Timing

• **Application circuit**

The application circuit of figure 40 can detect C1 and C2 error correction status.

Furthermore, the block error rate can also be monitored by counting the occurrences of C2 errors and using the following formula:

$$\text{Block Error Rate} \cong \frac{N}{9600 \times T}$$

N : value of counter
T :count time (sec)

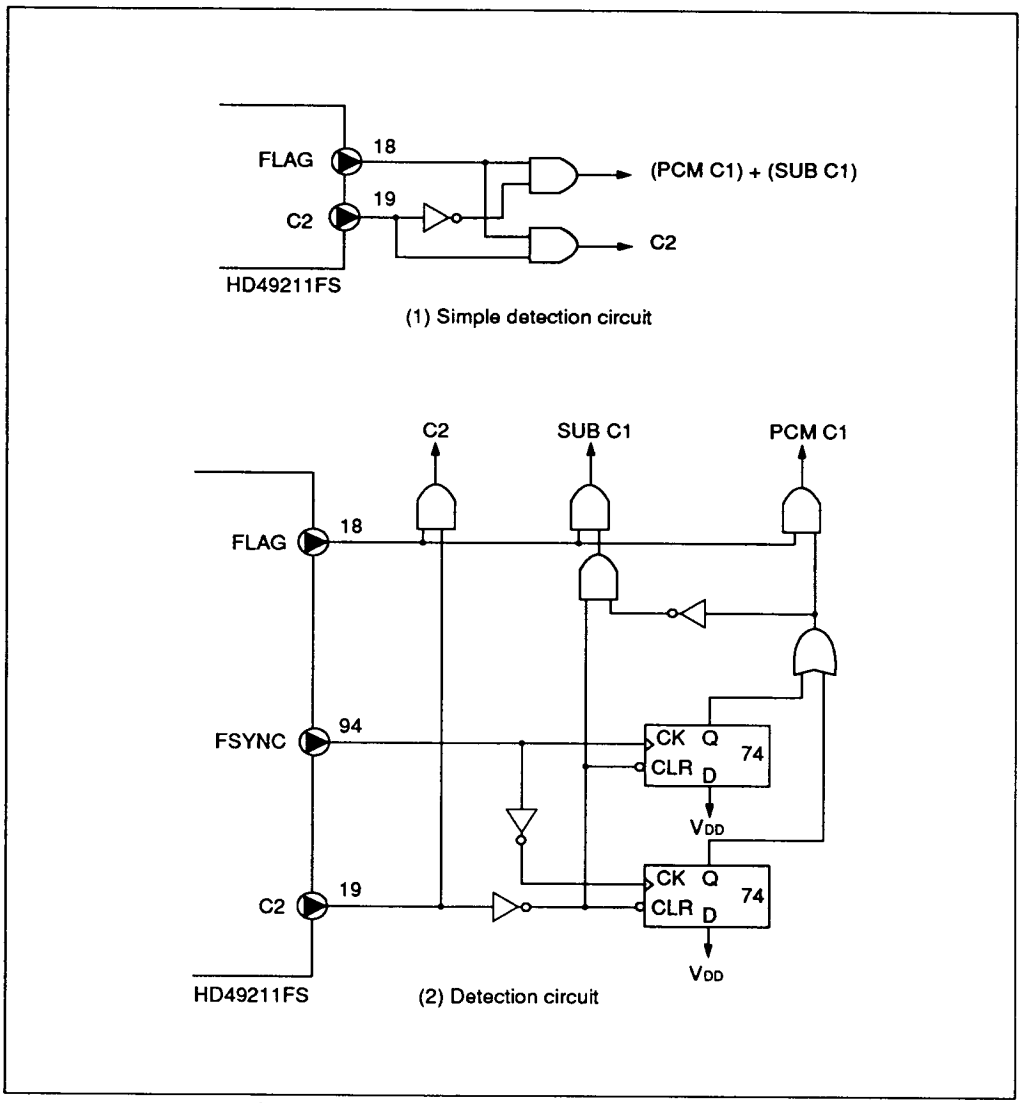


Figure 40 Error Correction Monitor Circuit

Digital Audio Interface Block

Block Overview

The digital audio interface is for transmitting PCM audio data, subcode data and all control signals between digital audio equipment over a single coaxial cable or optical fiber. This block implements a standard specified digital audio interface. Figure 41 shows the particular format of this chip.

Sub-frame format

Bi-phase modulation is used.

(1) Preamble

The preamble doubles as a leading, synchronizing signal and a sub-frame recognition signal. Left and right channels can be distinguished, as can the start of the block. Only the preamble does not use bi-phase modulation, but instead uses a special proprietary coding.

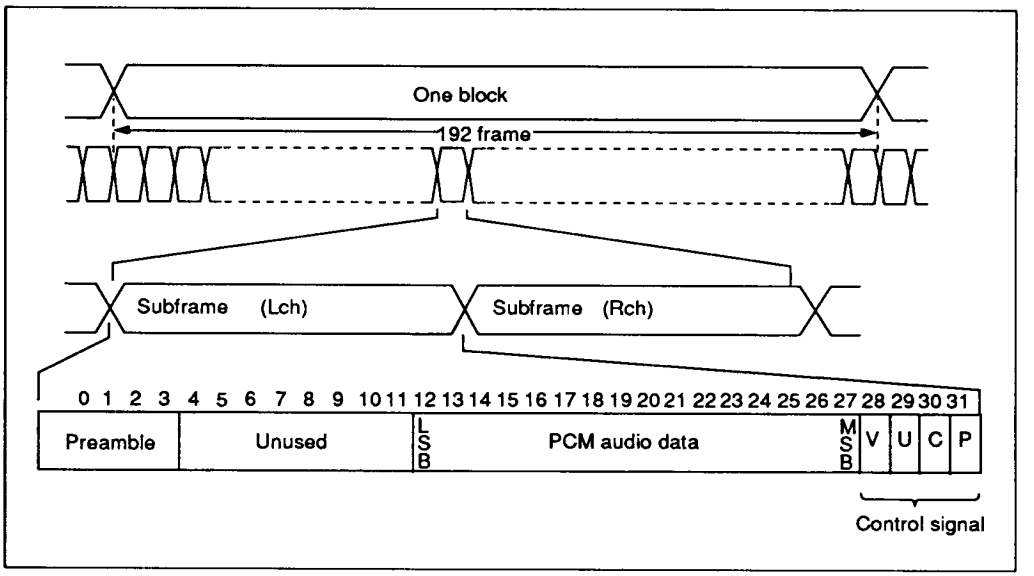


Figure 41 HD49211BFS Digital Audio Interface Signal Format

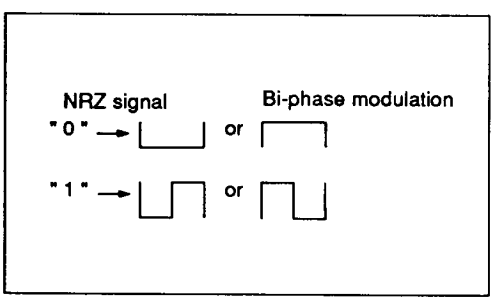


Figure 42 Bi-Phase Modulation

(2) PCM audio data

PCM audio data is transmitted LSB first.

(3) Control signals

(a) V (Valid flag)

Becomes "1" if the data of this sub-frame was interpolated.

(b) U (User data)

The meaning of the U-bit comes from the PCM audio data as shown in table 21.

Table 21 U-Bit Data Format

PCM audio data	Meaning of U-bit
L0	SYNC bit
R0	Start-ID bit
L1	Shortening-ID bit
Other	"0"

When mode data AC≠0, the start-ID and the shortening-ID will not be output. Therefore, when performing a skip, the microprocessor should send mode data AC≠0 only after sending the start-ID and shortening-ID and while FSYNC (pin 94) is "H".

(c) C

The format of channel status is shown in figure 44.

(i) Control

bit 0 = 0 : Public (home) use (Mode II)
bit 1 = 0 : Audio use
bit 2 = 0 : Digital copying prohibited
1 : Digital copying allowed
bit 3, 4 = 00 : No emphasis
10 : 50/15 µs emphasis
01 : Reserved
11 : Reserved
bit 5 = 0 : 2-channel audio
1 : Reserved (for 4-channel audio)

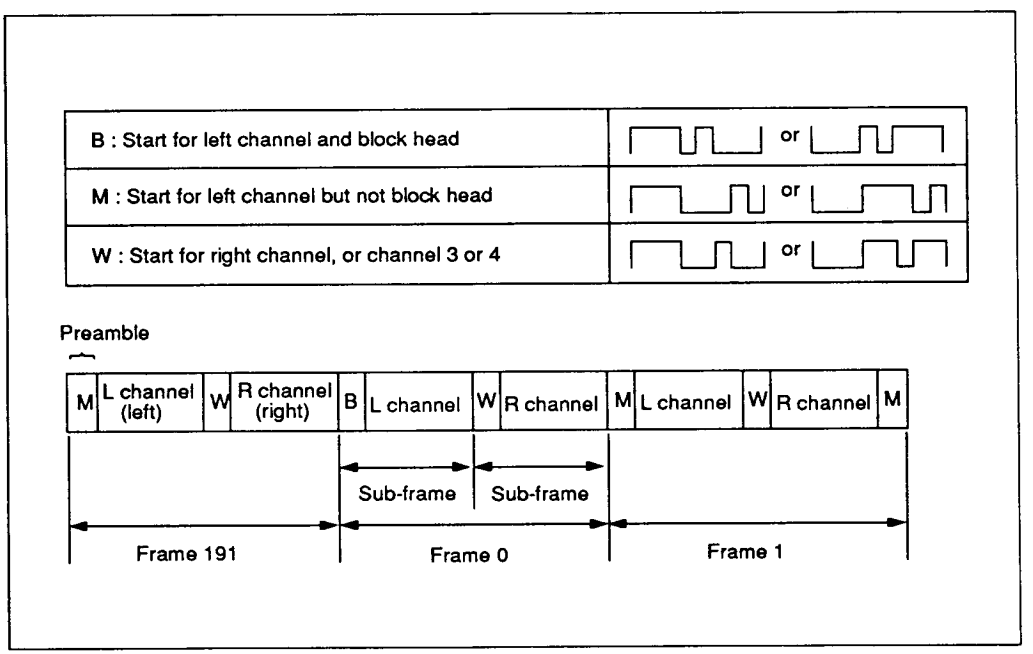


Figure 43 Preamble Format

(ii) Mode
bit 6, 7 = 00 : Mode 0

(iii) Category code
bit 8-15 = 11000000 : 2-channel digital audio tape recorder

(iv) Source number
bit 16-19 = 0000 : For future use

(v) Channel number
bit 20-23 = 1000 : Left channel of 2 channels
0100 : Right channel of 2 channels

Within the channel status bits, only the four bits of the channel number distinguish between left channel data and right channel data.

(vi) Sampling frequency
bit 24, 25 = 00 : 44.1 kHz
01 : 48 kHz
11 : 32 kHz
10 : Reserved

(vii) Sampling frequency accuracy
bit 28, 29 = 00 : Level II (allowable deviation = ±300 ppm)
10 : Level I (allowable deviation = ±50 ppm)

(d) P (Parity bit)

The parity bit is appended as the odd parity (number of 1's) in sub-frame slots 4-31.

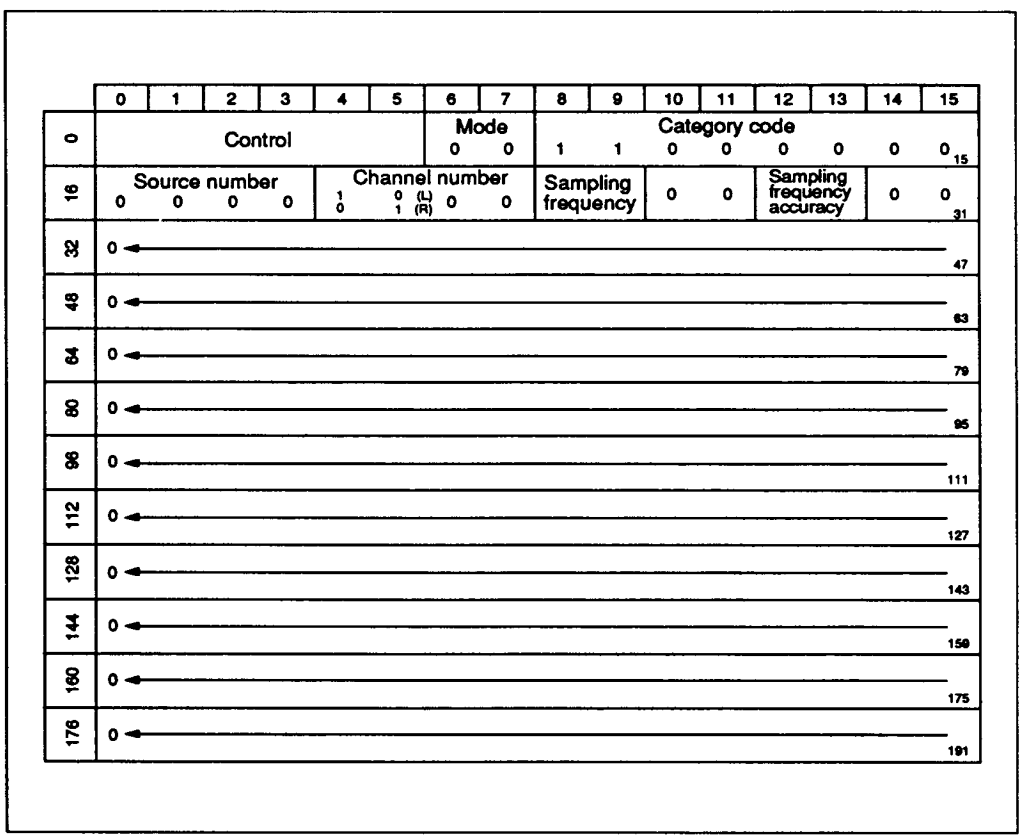


Figure 44 Channel Status Format

Block Function

TX (Digital audio interface output - pin 80)
The data output from TX changes between PCM audio data, C-bit, and U-bit depending on mode data RP and IS.

CKFID (Clock fidelity - pin 95)

This pin sets the sampling frequency accuracy of TX.

RX (Digital Audio Interface Input - pin 83)

This pin becomes valid as the digital audio interface input when mode data IS=2 and RP=1 or 2.

RXPLUL (RX PLL Unlock - pin 6)

This signal output indicates whether the PLL is locked or unlocked.

Table 22 Digital Audio Interface Output

	Mode data	RP=0	RP=1 or 2 (STOP or REC)			RP=3
Output		(PB)	IS=0	IS=1	IS=2	(AFREC)
TX	PCM audio data	PB	A/D	SIN	RX	PB
(SOUT=0)	C-bit	PB	Microprocessor	←	←	PB
	U-bit	PB	Microprocessor	←	←	Microprocessor
TX	PCM audio data	–	–	–	RX through	–
(SOUT=1)	C-bit	–	–	–	RX through	–
	U-bit	–	–	–	RX through	–

Table 23 Sampling Frequency Accuracy

CKFID= L	LEVEL I Allowable deviation = ±50 ppm
CKFID =H	LEVEL II Allowable deviation = ±300 ppm

Table 24 Digital Audio Interface Input

Audio data	PCM generation
Valid flag	Don't care
User data	Output to microprocessor
Channel status	Output to microprocessor
Parity	Output parity check results to microprocessor

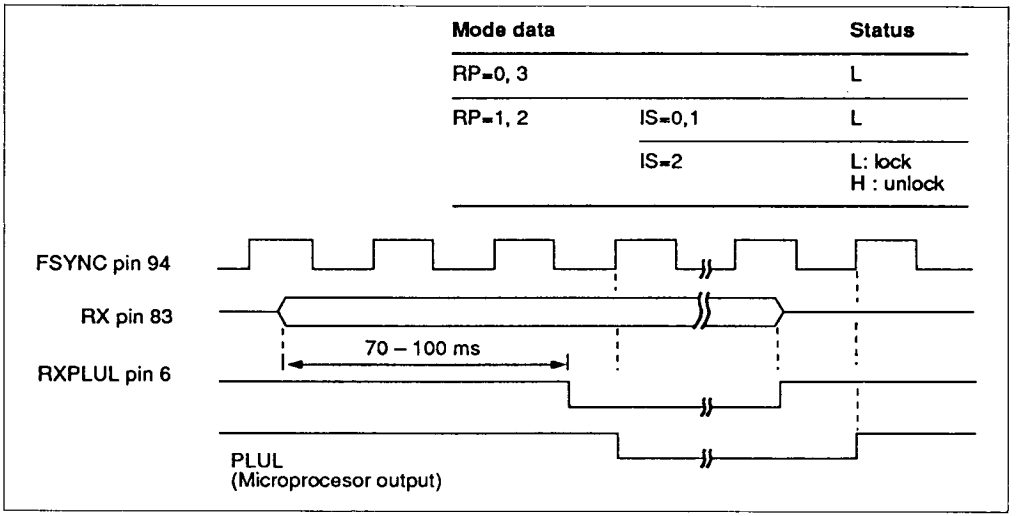


Figure 45 Relation Between Rx PPL and PLUL

PDO

Because the demodulation clock is a self-extracting type in the digital audio interface, the modulated signal requires a PLL to generate the master clock. The HD49211BFS uses an analog PLL with the preamble as its reference signal. Hardware up to the phase comparator is included on-chip.

Figure 46 shows an example of the external circuitry required.

As shown in figure 46, an active full-integrating low-pass filter should be used. R1, R2, and C1 determine the loop timing characteristics, while C2 prevents transients. R4 and C3 serve to filter out high-frequency noise, so the time constant derived from C1 and R2 must be sufficiently small.

The use of a VCO such as the TTL IC 74LS624, for which oscillation frequency is directly proportional to the control voltage, is assumed. If C4 is 47 pF then the oscillation will be approximately 12 MHz (FC ≅ 2.5 V).

In addition, the Vcc to the low-pass filter and the LS624 must be adequately protected from noise with an LC filter, EMI filter, or other protection.

PLL lock/unlock detect

The demodulation PLL must be locked on the input digital audio interface signal. The HD49211FS provides both the dedicated pin RXPLUL (pin 6) and the start of C-bit data transmitted to the microprocessor (PLUL) as a flag to indicate PLL lock/unlock status. The microprocessor can then determine lock/unlock status from either RXPLUL or the flag to change the mode data (FS, etc.) and to control operation in an optimal manner. This is important because control of the entire system comes from the microprocessor.

Figure 47 shows an example of microprocessor control.

PLUL operates in the stop and record modes as described below:

(1) Stop (record pause) mode (mode data RP=1)

When the PLL is unlocked, PLUL becomes "H". About 70 ms (Fs = 48 kHz) or 100 ms (Fs = 32 kHz) after locking, it will then become "L".

PLL locking can be performed only in stop mode, so if the PLL becomes unlocked then temporarily enter stop mode to lock it again.

(2) Record mode (mode data RP=2)

After the PLL locks, if it unlocks even once PLUL will output "H". When this happens during recording an abnormal event has occurred. In order to prevent erroneous recording on the tape,

PCM audio data is then internally forced to all "0". In theses cases, put the HD49211FS in stop mode and lock the PLL again.

Note: When the sync pattern B, M, or W is detected 16 times consecutively, the PLL is considered locked.

RXPLUL pin conditions for unlock "H"

The HD49211BFS determines on-chip that the PLL is unlocked using the conditions below:

1. One sub-frame is transmitted to RX without the preamble sync B, M, or W.
2. The parity bit is not included in the conditions for PLL unlock.

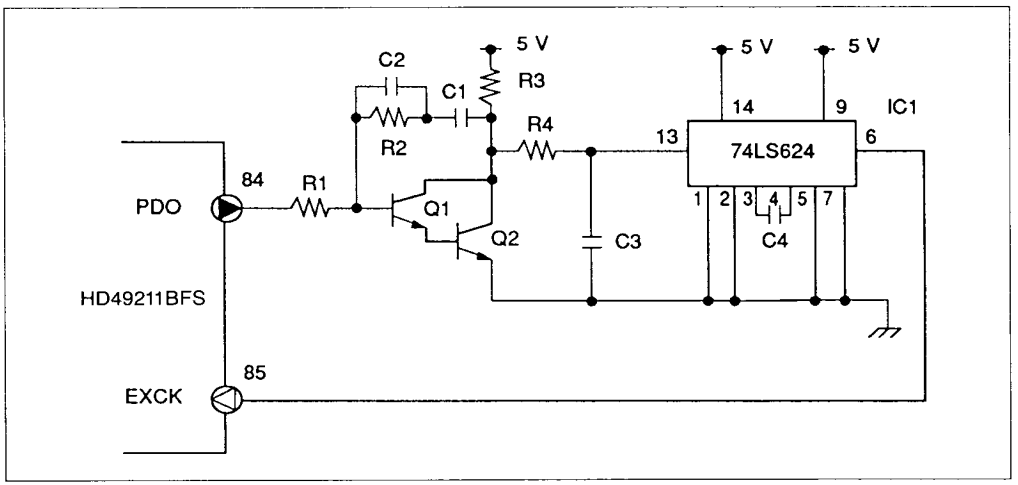


Figure 46 Example of External Circuitry

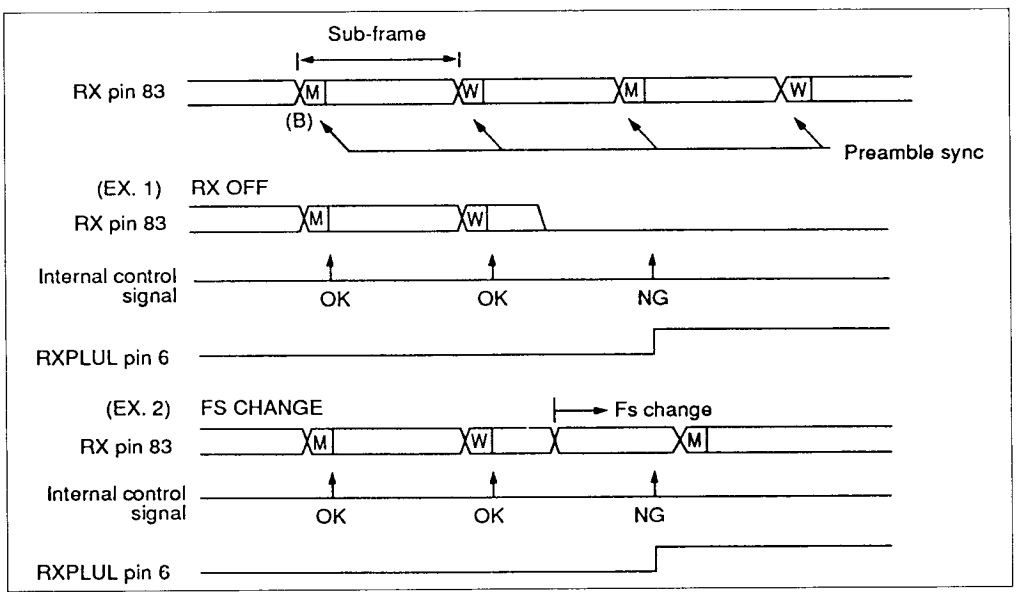
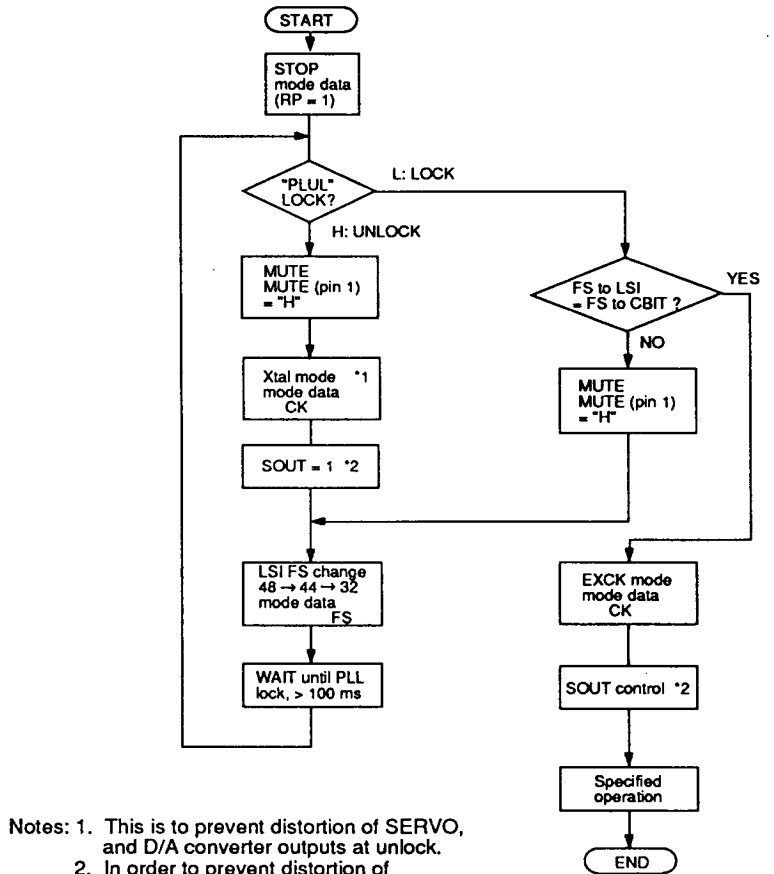


Figure 47 RXPLUL Pin Unlock Conditions



Notes: 1. This is to prevent distortion of SERVO, and D/A converter outputs at unlock.
2. In order to prevent distortion of connected D/A converter and FS detection of the DAT during FS change, set TX to RX throughput.

Figure 48 Digital Audio Interface Lock Detection Control Example

Input receiver and output driver circuits

Transmission circuits for the digital audio interface are defined to have an impedance of 75 Ω and a voltage level of 1 V at the transmit end, and an impedance of 75 Ω and a voltage level of 0.5 V at the receive end. Since this rules out a direct connection to the HD49211BFS, an input receiver circuit and output driver circuit are used. Figure 49 shows an example.

External Synchronization

Table 25 shows synchronization methods for the input conditions below.

Table 25 External Synchronization Modes

Input condition				Synchronization method		
Mode data EXS	RP	IS	RX category code	MPX synchronization	Frame synchronization	Notes
0	0, 3	–	–	×	Free	1
	1, 2	0, 1	–	×	Free	1
		2	Non-DAT	○	Free	1
			DAT	○	RX	2
1	0, 3	–	–	×	Free	1
	1	0, 1	–	×	STRG	1, 3
		2	–	○	STRG	3
	2	0, 1	–	×	Free	1
		2	–	○	Free	1, 4

Notes: 1. When frame synchronization is "free" and external synchronization is desired, after one RX frame or STRG frame synchronization, a mode change will provide external synchronization.
2. If the category code is DAT and the U-bit is not input as "1" (non-standard), then neither MPX or RX frame synchronization will occur and abnormal operation will result.
3. STRG synchronization can be performed only in stop mode.
4. With EXS=1, RP=2, and IS=2, MPX synchronization will occur independently of STRG.

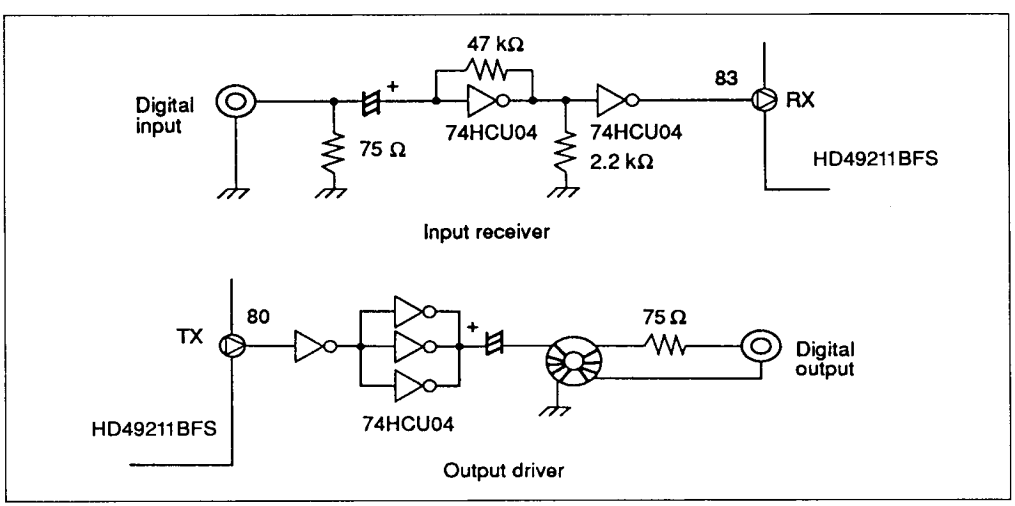


Figure 49 Input Receiver and Output Driver Examples

Notes on usage

(1) For the following mode changes, signal timing and data for the TX output will be abnormal for up to two frames.

i) Play/after-recording ´ Record/stop (RP=0 or 3 ↔ RP=1 or 2)
i) FS change (FS=a → FS=b)
iii) Master clock change (CK=a → CK=b)

Since this may cause abnormal operation on the receiving side, the TX signal should be gated externally.

(2) For the RX input (mode data IS=2) during stop/record, EXCK must be input. Even if CK=0 (master clock = X'tal), improper operation may occur.

(3) For the RX input (mode data IS=2, EXS=0) during stop/record, if the category of the RX signal is DAT, then synchronization will occur with SYNC in the U-bit. Accordingly, if the RX category changes to DAT from GENERAL or another category, synchronization will occur even while recording, so chip timing will become misaligned.

To prevent this, set EXS=1 during record (mode data RP=2).

(4) During playback (mode data RP=0), if the U-bit or C-bit playback data in the TX output is no good then the previous values will be preserved. Accordingly, if the tape is halted in a particular section, such as the start ID or shortening ID then its status will be preserved. To return this to zero, set the mode AC≠0 (U-bit only valid).

(5) At power-on, always reset $\overline{\text{MRST}}$ (pin 9) to "L" once.

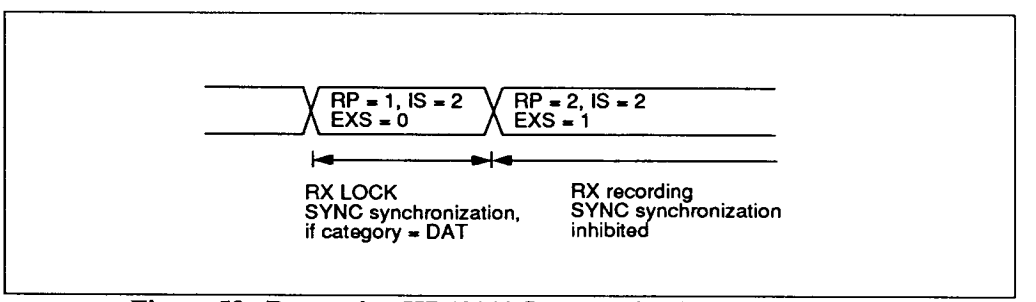


Figure 50 Preventing HD49211 Synchronization Misalignment

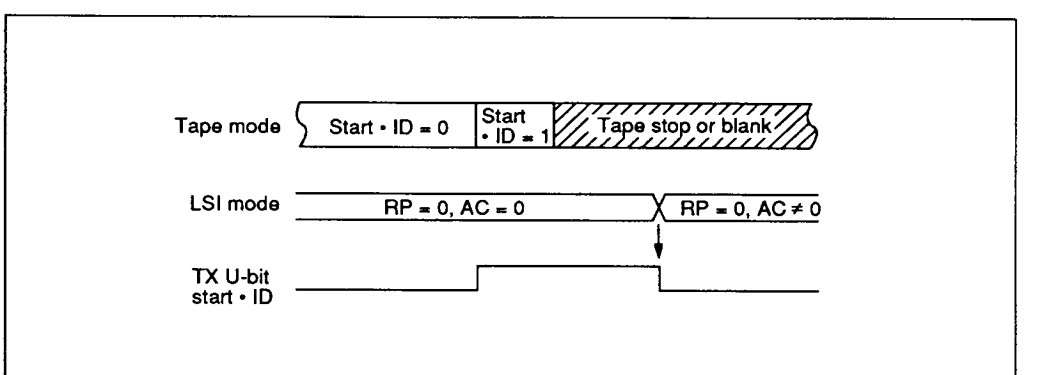


Figure 51 TX U-bit When Tape Suddenly Halts

A/D-D/A Control Block

Block Overview

This block controls the A/D converter and the D/A converter. It works with serial input/output so digital filtering can be used.

- **A/D converter control**

This section consists of control logic for a 3-stage cascaded integrating A/D converter, an A/D converter interface, and a serial input. The HA12132MP and HA12132MP can be used for the A/D converter, allowing low power consumption, low-cost A/D conversion.

Also, when both INHL and INHR are "L" and mode data IS=1, serial input mode is entered and digital filtering can be used.

- **D/A converter control**

This section consists of control logic for a 3-stage parallel integrating D/A converter, a D/A converter interface, and a serial output. The HA12131MP, HA12132MP, and HA12108MP can be used for the D/A converter, allowing low power consumption, low-cost D/A conversion.

Also, when both INHL and INHR are "L", serial data is output from SOUT (pin 71).

Block Function

I/O pins

If either or both INHL and INHR are brought to "L", then SHR, SHL, DCR, DCL, MODE, ADSR, and ADSL become respectively SOUT, BCK, FS2, FS4, EF DAOUT, and RXPLUL.

MODE (Pin 76): When both INHL and INHR are "H", mode switching for the HA12131MP and HA12132 MP can be used as described below:

H : A/D mode
L : D/A mode

If only one of INHL and INHR is "H", then MODE is "H". If both are "L", then the pin becomes the EF output.

Table 26 I/O Pin Functions

Pin name	Pin no.	Function
INHR	58	Control input for halting A/D right channel operation
INHL	59	Control input for halting A/D left channel operation
COMP 1 – 3	62 – 60	A/D comparator inputs
CSW 1 – 3	66 – 68	Control input for A/D-D/A current source
OFS	69	Control input for D/A offset circuit
SHR (SOUT)	71	D/A right channel sample-hold output (serial output)
SHL (BCK)	72	D/A left channel sample-hold output (BCK output)
MPX	73	I/O left/right status output
DCR (FS2)	74	D/A right channel discharge output (FS x 2 output)
DCL (FS4)	75	D/A left channel discharge output (FS x 4 output)
MODE (EF)	76	A/D-D/A switching output (EF: interpolation flag output)

I/O Pin Functions (cont)

ADSR (DAOUT)	77	A/D right channel PWM output for servo (DAOUT monitor)
ADSL (RX PLUL)	78	A/D left channel PWM output for servo (RXPLUL monitor)
SIN	79	Serial input

MPX (pin 73) : When "H", CSW1 – 3 and OFS for the left channel will be output.

The following signals are output when both INHR (pin 58) and INHL (pin 59) are "L".

BCK (pin 72) : Bit synchronizing clock output
FS4 (pin 75) : 4 × Fs clock output
FS2 (pin 74) : 2 × Fs clock output
SOUT (pin 71) : Serial data output. Outputs synchronized on falling edge of BCK.
EF (pin 76) : Indicates interpolation of SOUT data. "H" when data was interpolated.
SIN (pin 79) : Serial data input. Latches input on rising edge of BCK.

Note: If EF is counted, the ratio of uncorrectable errors can be calculated.

$$\text{Uncorrectable error ratio} = \frac{\text{EF count}}{25 \times \text{fs [Hz]} \times \text{T [sec]}} \text{ per word}$$

$$\cong \frac{\text{EF count}}{45 \times \text{fs [Hz]} \times \text{T [sec]}} \text{ per symbol}$$

T = EF count time

Table 27 INHL, INHR Modes

Mode	I/O	Appropriate hardware
INHL = INHR = H	A/D and D/A	HA12131, HA12132, etc.
INHL = INHR = L	Serial input	External A/D, digital filter
	Serial output	External D/A, digital filter

Pin Functions

1) INHR (pin 58) = "H", INHL (pin 59) = "H"

Table 28 Pin Functions for INHR = "H", INHL = "H"

Pin name	Mode data	RP = 0 or 3	RP = 1 or 2		
			IS = 0	IS = 1	IS = 2
Mode D/A output	A/D input	Playback uses*1	Record DA output	Prohibited	Record RX input,
COMP 1 – 3	(I)	Don't care	AD COMP	Don't care	←
CSW 1 – 3	(O)	D/A CSW	A/D CSW	D/A CSW	←
OFS	(O)	D/A OFS	L	D/A OFS	←
DCL	(O)	D/A DCL	L	D/A DCL	←
DCR	(O)	D/A DCR	L	D/A DCR	←
SHL	(O)	D/A CSW	H	D/A SHL	←
SHR	(O)	D/A SHR	H	D/A SHR	←
MODE	(O)	L	H	L	L
MPX	(O)	MPX	←	←	←
SIN	(I)	Don't care	←	DATA IN	Don't care
ADSL	(O)	Duty 50 % (8 × FS)	ADSL	←	Duty 50%
ADSR	(O)	Duty 50 % (8 × FS)	ADSR	←	Duty 50%

2) INHR = "L", INHL = "L"

Table 29 Pin Functions for INHR = "L", INHL = "L"

Pin name	Mode data	RP = 0 or 3	RP = 1 or 2		
			IS = 0	IS = 1	IS = 2
Mode		Playback SOUT output	Record A/D input, SOUT output	Record SIN input, SOUT output	Record RX input, SOUT output
COMP 1 – 3	(I)	Don't care	A/D COMP	Don't care	←
CSW 1 – 3	(O)	(D/A CSW)	A/D CSW	(D/A CSW)	←
OFS	(O)	(D/A OFS)	L	(D/A OFS)	←
DCL	(O)	FS x 4 output	←	←	←
DCR	(O)	FS x 2 output	←	←	←
SHL	(O)	BCK output	←	←	←
SHR	(O)	SOUT output	←	←	←
MODE	(O)	EF output	L	←	←
MPX	(O)	MPX	←	←	←
SIN	(I)	Don't care	←	DATA IN	Don't care
ADSL	(O)	Duty 50 %	ADSL	←	Duty 50%
ADSR	(O)	Duty 50 %	ADSR	←	Duty 50%

3) INHR = "L", INHL = "H"

Table 30 Pin Functions for INHR = "L", INHL = "H"

	Mode data	RP = 0 or 3	RP = 1 or 2		
Pin name			**IS = 0**	**IS = 1**	**IS = 2**
Mode		**Playback** SOUT output (use prohibited)	**Record** A/D input, SOUT output (Left channel operation only)	**Record** SIN input, SOUT output (Left channel data only)	**Record** RX input, SOUT output
COMP 1 – 3	(I)	Don't care	A/D COMP	Don't care	←
CSW 1 – 3	(O)	(D/A CSW)	A/D CSW	(D/A CSW)	←
OFS	(O)	(D/A OFS)	L	(D/A OFS)	←
DCL	(O)	FS x 4 output	←	←	←
DCR	(O)	FS x 2 output	←	←	←
SHL	(O)	BCK output	←	←	←
SHR	(O)	SOUT output	←	←	←
MODE	(O)	H	←	←	←
MPX	(O)	MPX	←	←	←
SIN	(I)	Don't care	←	DATA IN Lch	Don't care
ADSL	(O)	Duty 50 %	←	←	←
ADSR	(O)	Duty 50 %	←	←	←

4) INHR = "H", INHL = "L"

Table 31 Pin Functions for INHR = "H", INHL = "L"

Pin name	Mode data	RP = 0 or 3	RP = 1 or 2		
			IS = 0	IS = 1	IS = 2
Mode		Playback SOUT output (use prohibited)	Record A/D input, SOUT output (Left channel operation only)	Record SIN input, SOUT output (Left channel data only)	Record RX input, SOUT output
COMP 1 – 3	(I)	Don't care	A/D COMP	Don't care	←
CSW 1 – 3	(O)	(D/A CSW)	A/D CSW	(D/A CSW)	←
OFS	(O)	(D/A OFS)	L	(D/A OFS)	←
DCL	(O)	FS x 4 output	←	←	←
DCR	(O)	FS x 2 output	←	←	←
SHL	(O)	BCK output	←	←	←
SHR	(O)	SOUT output	←	←	←
MODE	(O)	H	←	←	←
MPX	(O)	MPX	←	←	←
SIN	(I)	Don't care	←	DATA IN Rch	Don't care
ADSL	(O)	Duty 50%	←	←	←
ADSR	(O)	Duty 50%	←	←	←

A/D converter control outputs

HA12131 or HA12132 are assumed.

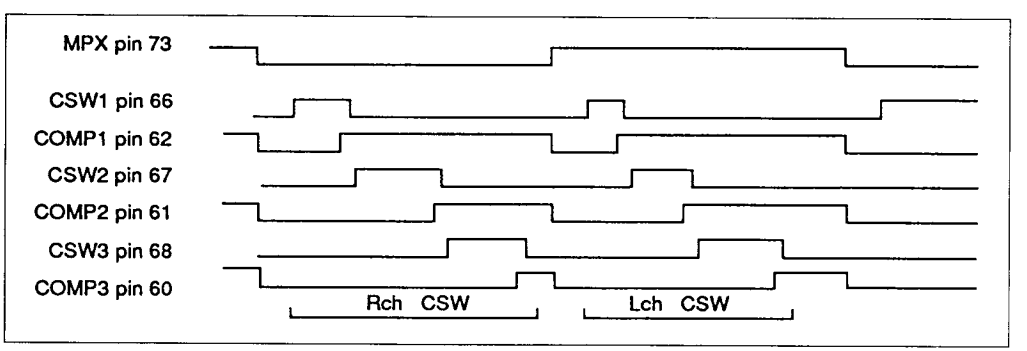


Figure 52 A/D Control Signal Timing

Serial data I/O

Serial data is output when INHL=INHR="L".
Serial data input is valid when mode data IS=1.

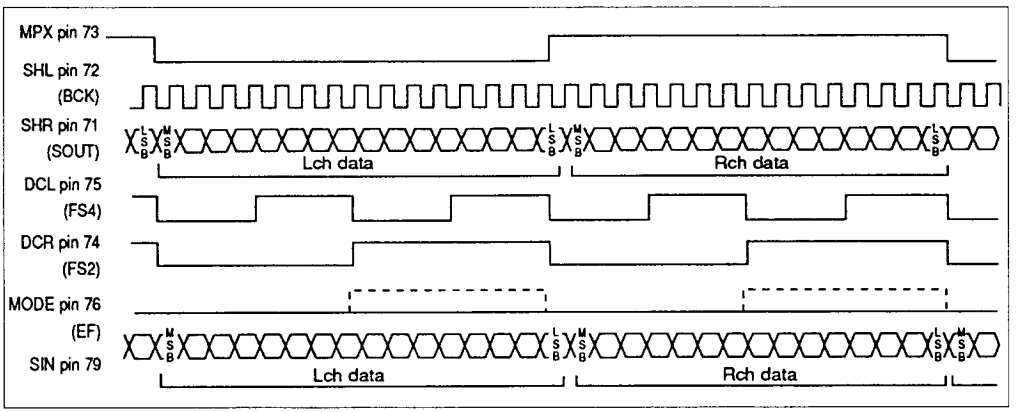


Figure 53 Serial Data I/O Timing

A/D converter offset servo signal outputs ADSR (pin 77) and ADSL (pin 78)

In order to cancel the A/D converter offset, the upper 3 bits from the 16-bit audio data of both left and right channels are used to change the duty of the output signal.

(1) Operating modes

Table 32 A/D Converter Offset Servo Signal Output Modes

RP IS	0 PLAY	1 STOP	2 REC	3 AFRPC
0	OFF	ON	ON	OFF
1	OFF	ON	ON	OFF
2	OFF	OFF	OFF	OFF

ON: OPERATING
OFF: DUTY 50% (8FS OUTPUT)

When abjusting the A/D cpmverter, make INGL≠INHR and put the chip in OFF mode.

(2) Output formats

PCM.DATA (upper 3 bits)			OUTPUT DUTY
0	1	1	0/8
0	1	0	1/8
0	0	1	2/8
0	0	0	3/8
1	1	1	5/8
1	1	0	6/8
1	0	1	7/8
1	0	0	8/8

M
S
B

(15) (14) (13)

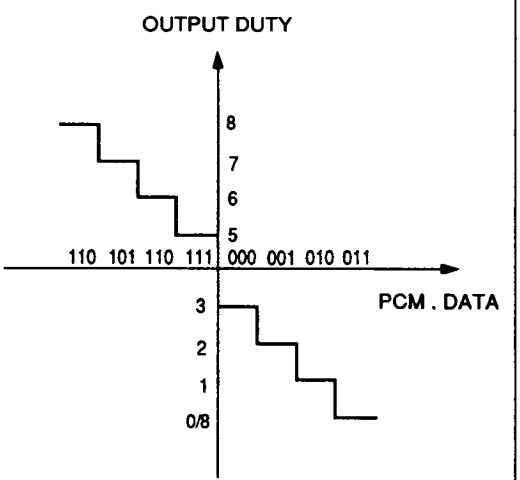


Figure 54 A/D Converter Offset Servo Signal Output Format

(3) Timing

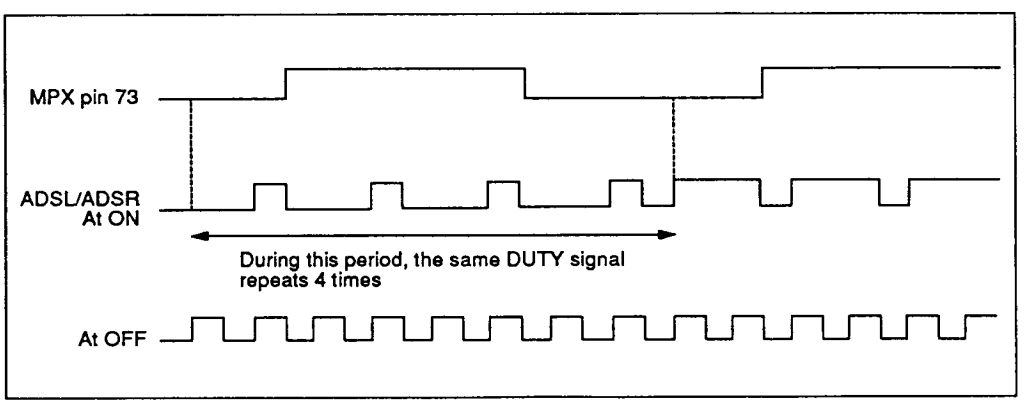


Figure 55 A/D Converter Offset Servo Signal Output Timing

External interface

Examples of the A/D-D/A converter and digital filter interface are shown in figures 56 – 58.

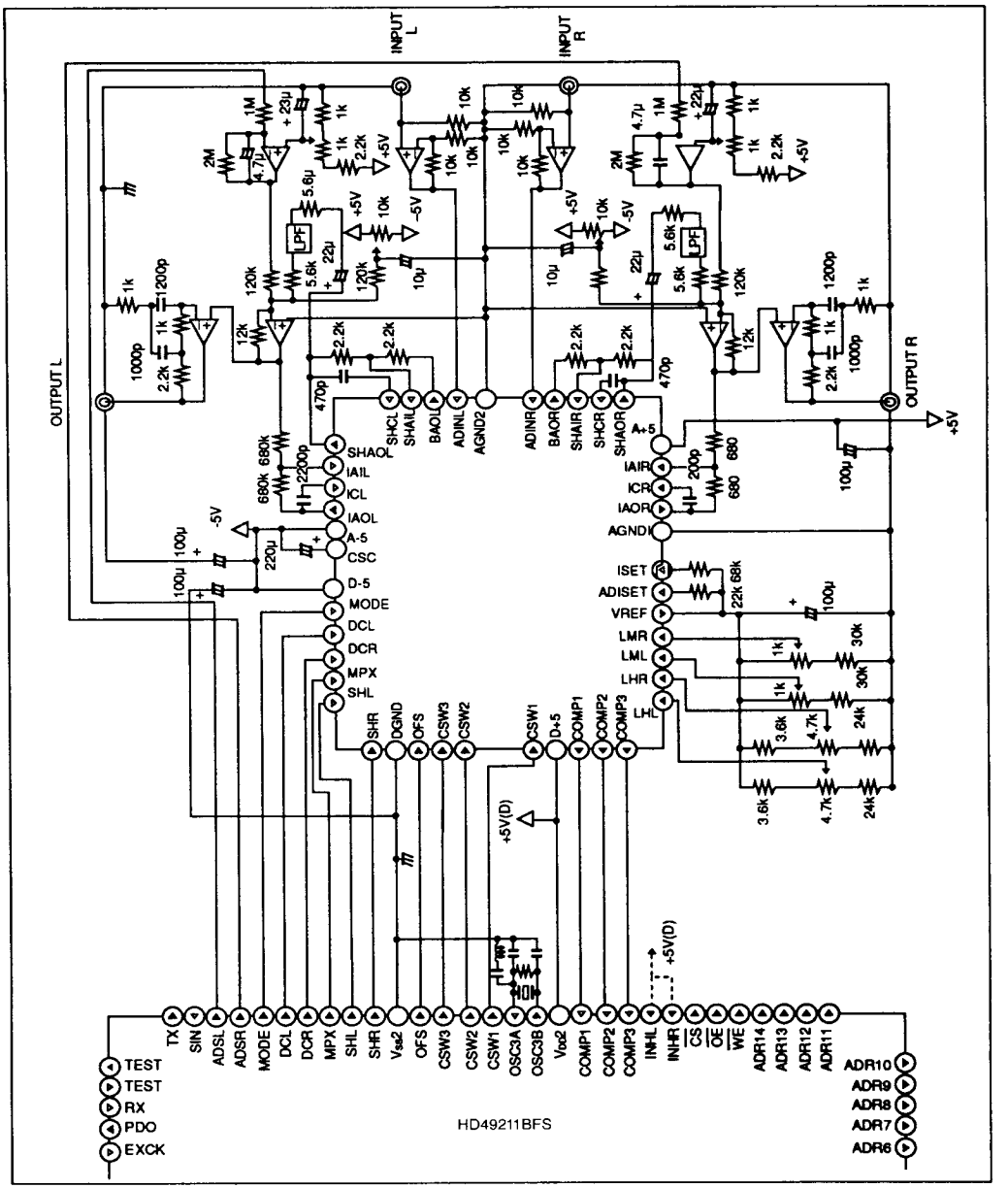


Figure 56 HA12131 Interface Example

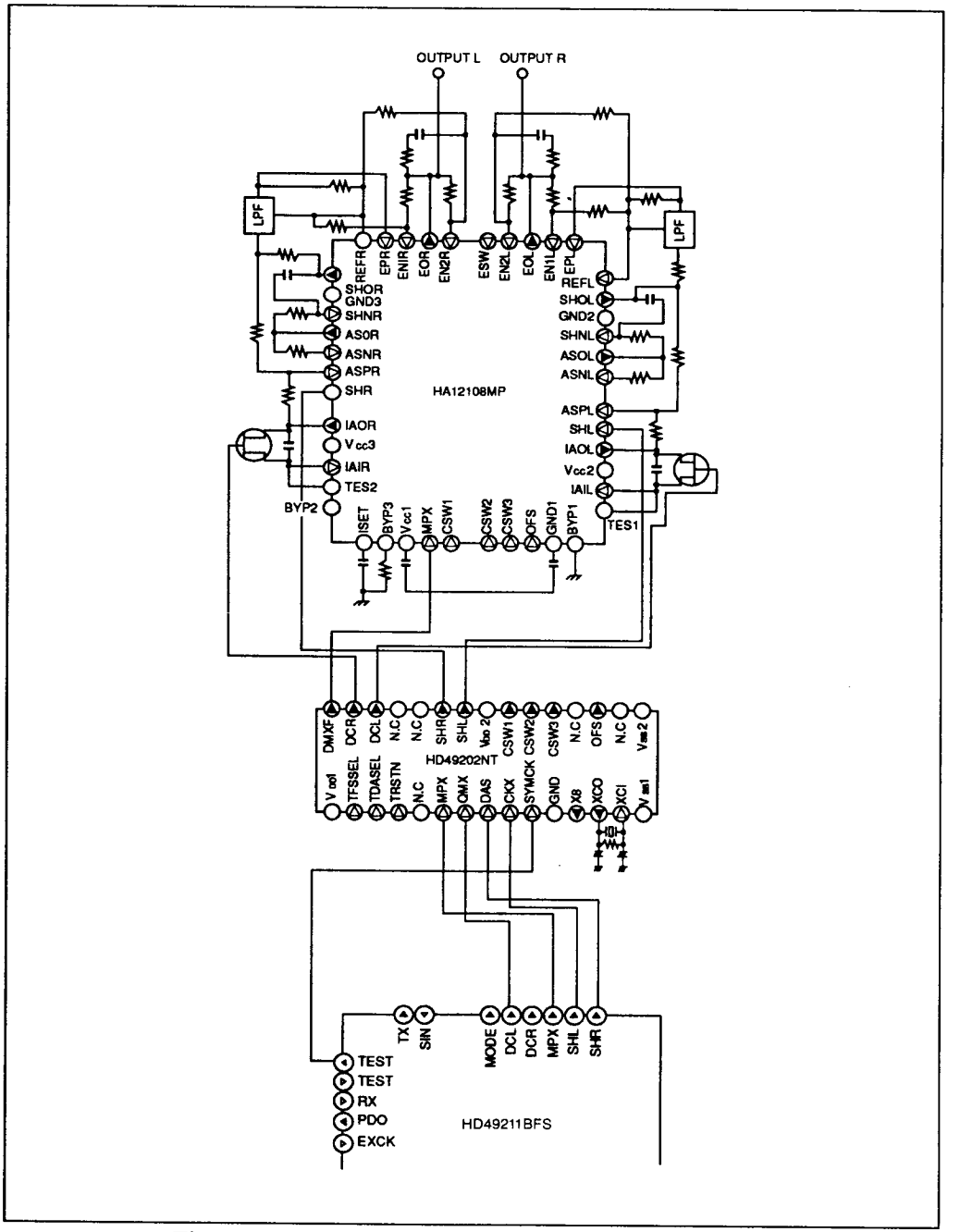


Figure 57 HD49202/HA12108 MP Interface Example

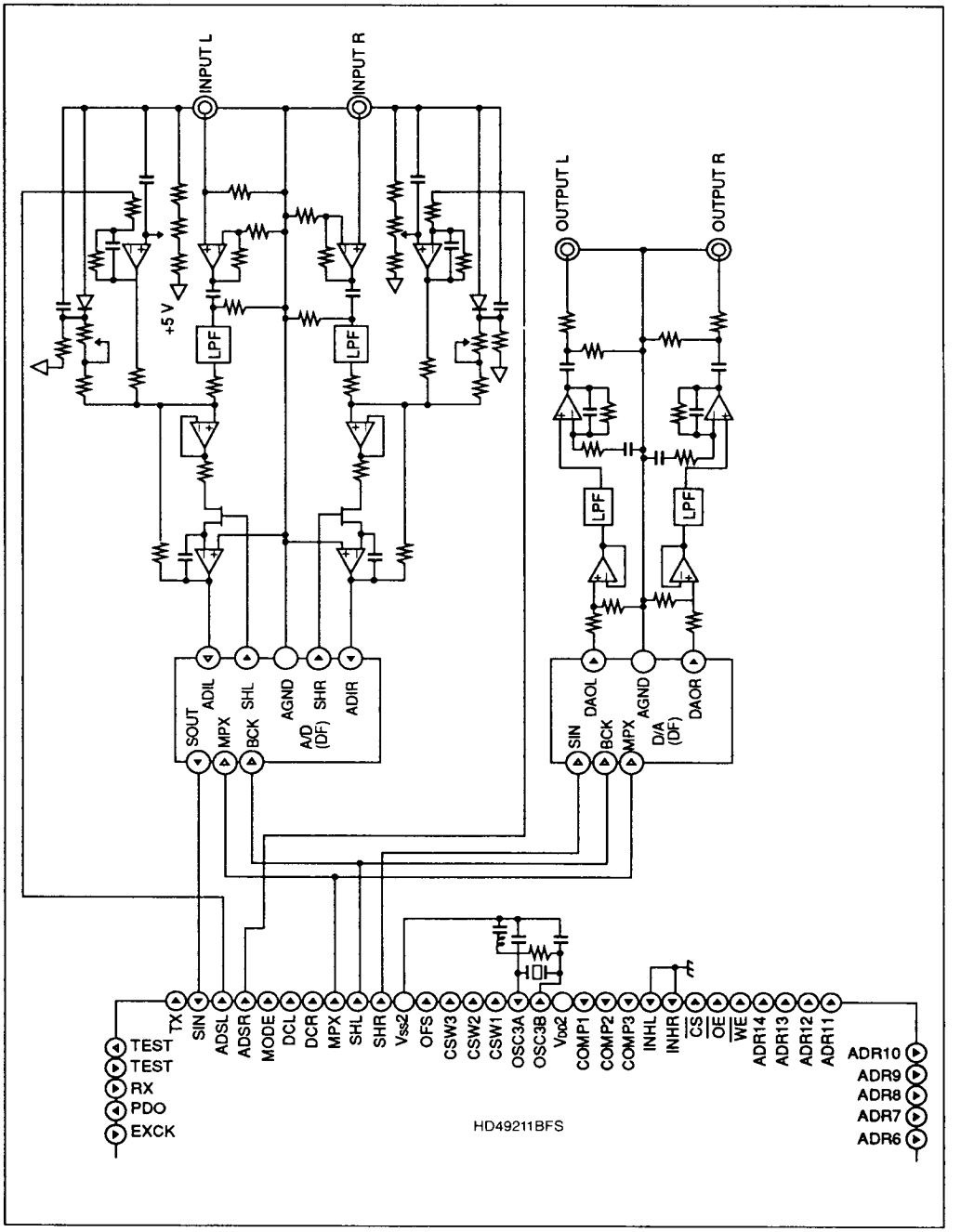


Figure 58 Serial mode A/D-D/A Interface Example

I/O Pin Functions (cont)

ADSR (DAOUT)	77	A/D right channel PWM output for servo (DAOUT monitor)
ADSL (RX PLUL)	78	A/D left channel PWM output for servo (RXPLUL monitor)
SIN	79	Serial input

MPX (pin 73) : When "H", CSW1 – 3 and OFS for the left channel will be output.

The following signals are output when both INHR (pin 58) and INHL (pin 59) are "L".

BCK (pin 72) : Bit synchronizing clock output
FS4 (pin 75) : 4 × Fs clock output
FS2 (pin 74) : 2 × Fs clock output
SOUT (pin 71) : Serial data output. Outputs synchronized on falling edge of BCK.
EF (pin 76) : Indicates interpolation of SOUT data. "H" when data was interpolated.
SIN (pin 79) : Serial data input. Latches input on rising edge of BCK.

Note: If EF is counted, the ratio of uncorrectable errors can be calculated.

$$\text{Uncorrectable error ratio} = \frac{\text{EF count}}{25 \times \text{fs [Hz]} \times \text{T [sec]}} \text{ per word}$$

$$\cong \frac{\text{EF count}}{45 \times \text{fs [Hz]} \times \text{T [sec]}} \text{ per symbol}$$

T = EF count time

Table 27 INHL, INHR Modes

Mode	I/O	Appropriate hardware
INHL = INHR = H	A/D and D/A	HA12131, HA12132, etc.
INHL = INHR = L	Serial input	External A/D, digital filter
	Serial output	External D/A, digital filter

System Interface Example

Below is an example of an interface between the HD49211BFS and its support LSI chips.