HMC724LC3C

14 Gbps FAST RISE TIME 1:2 FANOUT BUFFER

Typical Applications

The HMC724LC3C is ideal for:

- 16 G Fiber Channel
- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 14 Gbps
- Clock Buffering up to 14 GHz

Features

Inputs Terminated Internally to 50 Ohms

Differential Inputs are DC Coupled

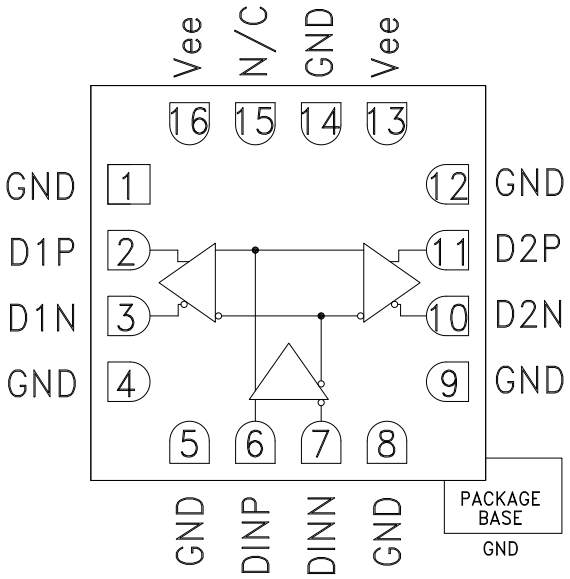
Propagation Delay: 110 ps

Fast Rise and Fall Times: 19 / 18 ps

Power Dissipation: 300 mW

16 Lead Ceramic 3x3 mm SMT Package: 9 mm^2

Functional Diagram



General Description

The HMC724LC3C is a 1:2 Fanout Buffer designed to support data transmission rates up to 14 Gbps, and clock frequencies as high as 14 GHz. All differential inputs and outputs are DC coupled and terminated on chip with 50 Ohm resistors to ground. The outputs may be used in either single ended or differential modes, and should be AC or DC coupled into 50 Ohm resistors connected to ground.

All differential inputs to the HMC724LC3C are CML and terminated on-chip with 50 Ohms to the positive supply, GND, and may be DC or AC coupled. The differential CMI outputs are source terminated to to 50 Ohms and may also be AC or DC coupled. Outputs can be connected directly to a 50 Ohm ground-terminated system or drive devices with CML logic input. The HMC724LC3C operates from a single -3.3 V supply and is available in ROHS-compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25 °C, Vee = -3.3 V

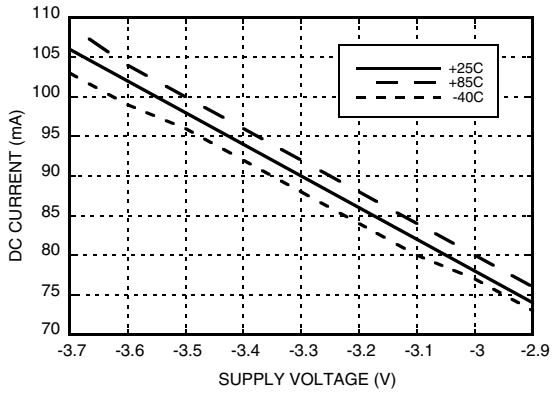
Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		-3.6	-3.3	-3.0	V
Power Supply Current			90		mA
Maximum Data Rate			14		Gbps
Maximum Clock Rate			14		GHz
Input Voltage Range		-1.5		0.5	V
Input Differential Range		0.1		2.0	Vp-p
Input Return Loss	Frequency <14 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		550		mVp-p
	Differential, peak-to-peak		1100		mVp-p
Output High Voltage			-10		mV
Output Low Voltage			-560		mV
Output Rise / Fall Time	Single-Ended, 20% - 80%		19 / 18		ps

Electrical Specifications (continued)

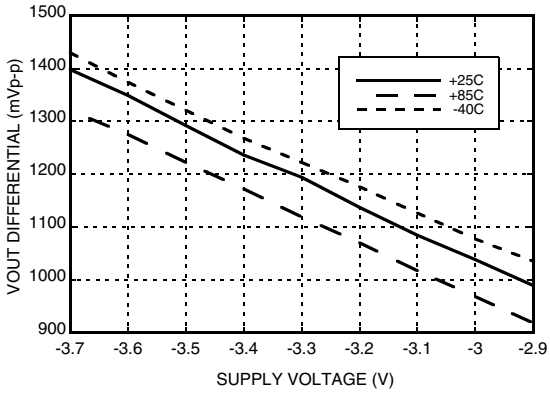
Parameter	Conditions	Min.	Typ.	Max	Units
Output Return Loss	Frequency <14 GHz		10		dB
Small Signal Gain			27		dB
Random Jitter J_R	rms		0.2		ps rms
Deterministic Jitter, J_D	δ - δ, 2^{15}-1 PRBS input [1]		2	6	ps
Propagation Delay, td			110		ps
D1 to D2 Data Skew, t_{SKEW}			<2		ps

[1] Deterministic jitter measured at 13 GHz with a 300 mVp-p, 2^{15}-1 PRBS input sequence.

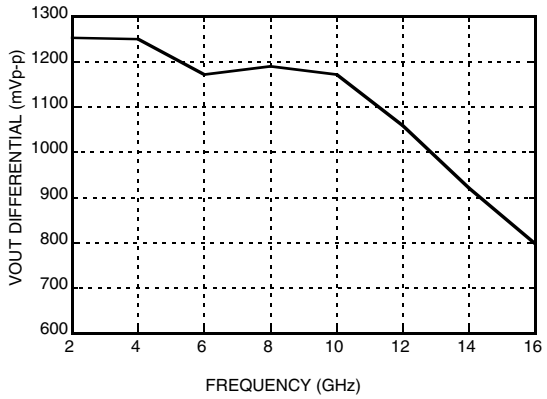
DC Current vs. Supply Voltage [1]



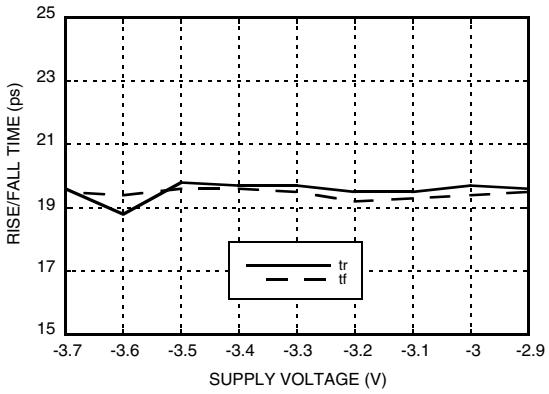
Output Differential Voltage vs. Supply Voltage [2]



Output Differential Voltage vs. Frequency [3]

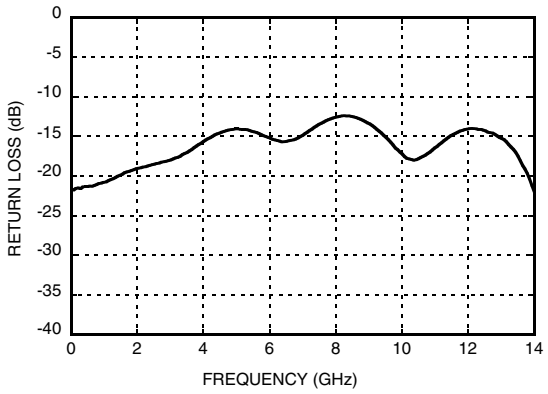


Rise / Fall Time vs. Supply [1]

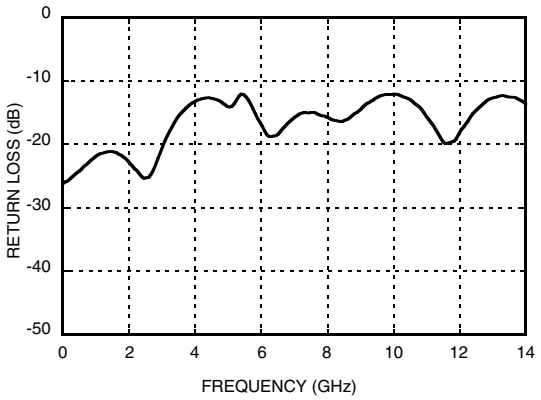


[1] Data rate = 13 Gbps [2] Frequency = 10 GHz [3] Vee = 3.3 V

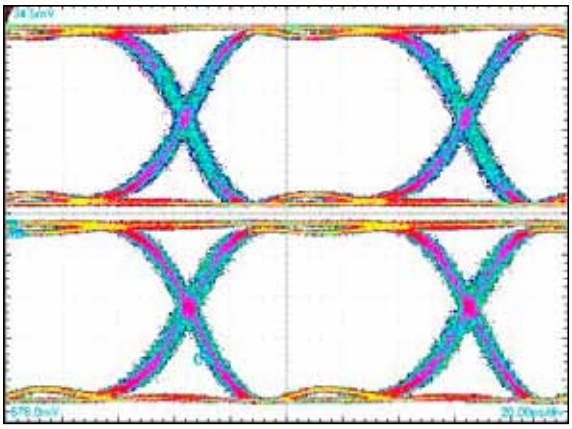
Output Return Loss vs. Frequency



Input Return Loss vs. Frequency

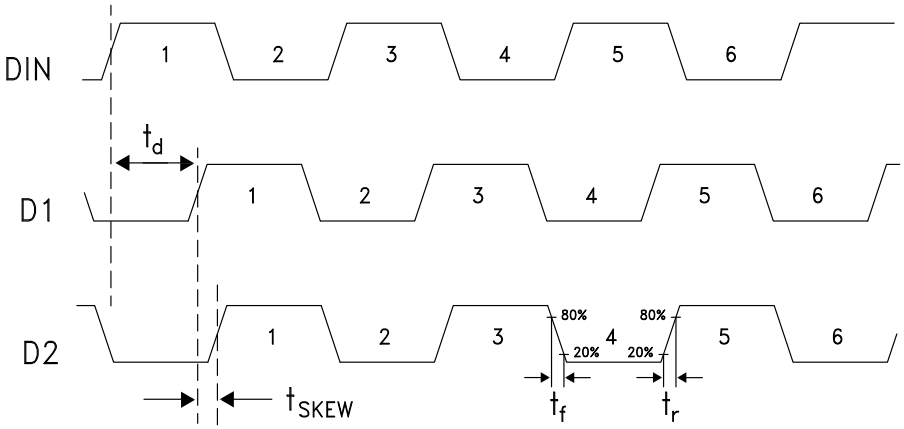


Eye Diagram



[1] Test Conditions:
Pattern generated with an Agilent N4903A Serial BERT.
Eye Diagram presented on a Tektronix CSA 8000.
Device input = 10 Gbps PN code, Vin = 300 mVp-p differential.
Both output channels shown.

Timing Diagram

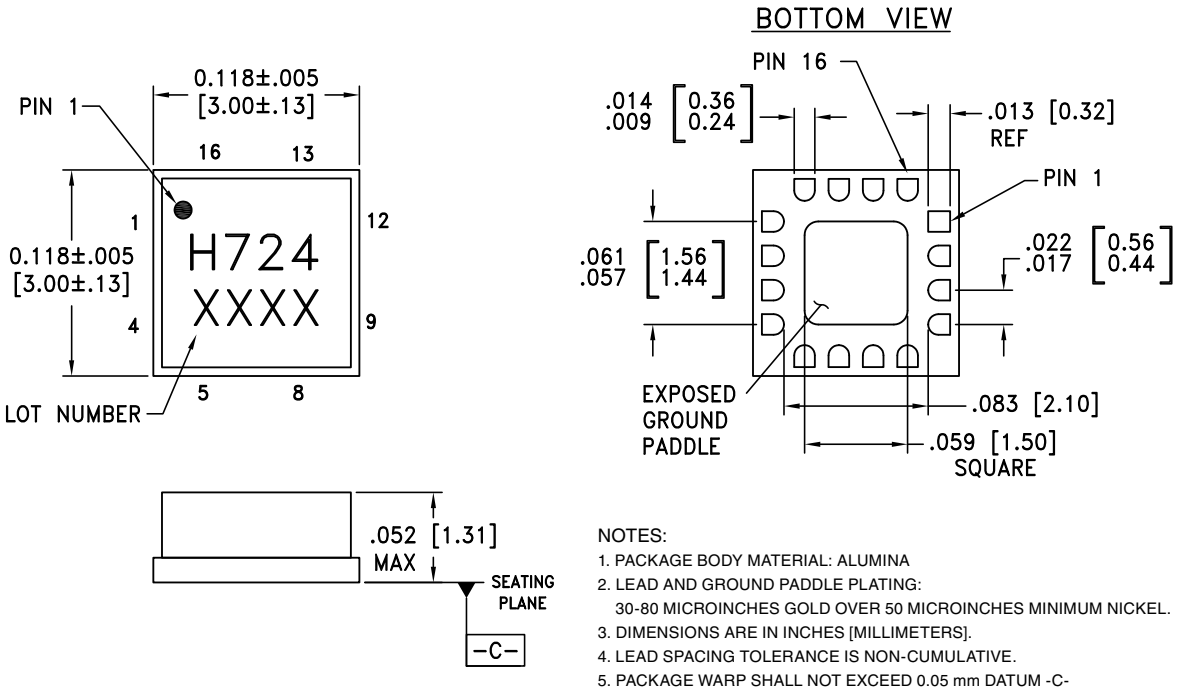


Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75 V to +0.5 V
Input Signals	-2 V to +0.5 V
Output Signals	-1.5 V to +1 V
Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C)	0.68 W
Thermal Resistance ($R_{th\ j\text{-}p}$) Worst case junction to package paddle	59 °C/W
Maximum Junction Temperature	125 °C
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C

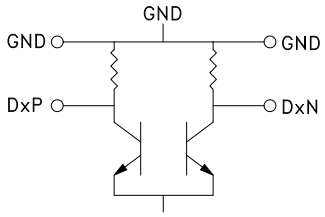
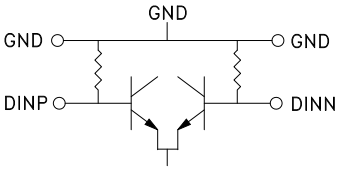
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



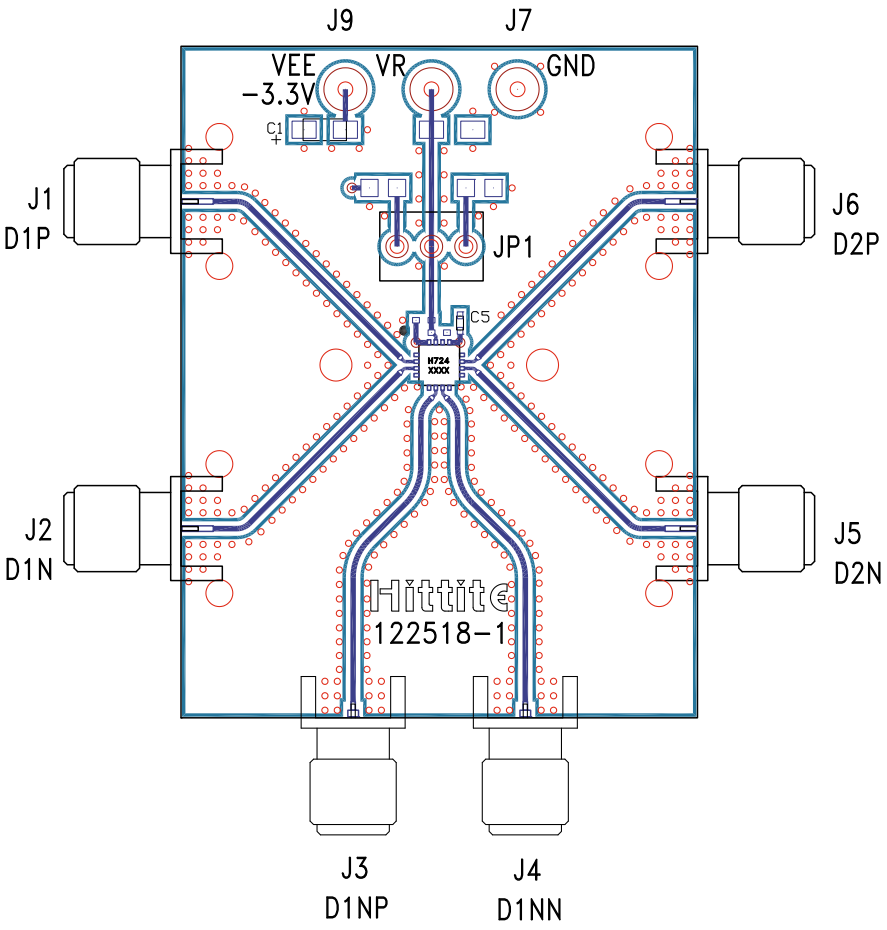
NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO GND.

Pin Descriptions [1]

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3 10, 11	D1P, D1N D2N, D2P	Differential Data Inputs, Current Mode Logic (CML) referenced to positive supply.	
6, 7	DINP, DINN	Differential Data Outputs, Current Mode Logic (CML) referenced to positive supply.	
13, 16	Vee	Negative Supply	
14, Package Base	GND	Supply Ground	
15	N/C	No Connection required. This pin may be connected to RF/DC ground without affecting performance.	

[1] Contact HMC for alternate pinouts

Evaluation PCB



List of Materials for Evaluation PCB 122520 [1]

Item	Description
J1 - J6	PCB Mount SMA RF Connectors
J7, J9	DC Pin
C1	4.7 µF Capacitor, Tantalum
C5	100 pF, Capacitor 0402 Pkg.
U1	HMC724LC3C High Speed Logic, Fanout Buffer
PCB [2]	122518 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed packaged base should be connected to GND. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit