DOCUMENT NUMBER AND REVISION

VL-FS-MGLS19264-07 REV. C

(MGLS19264-HT-LED03)

DOCUMENT TITLE:

SPECIFICATION OF LCD MODULE TYPE

MODEL NUMBER: MGLS19264-07

DEPARTMENT	NAME	SIGNATURE	DATE
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DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM	TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
	A	2000.09.19	First Release	PHILIP CHENG	K.P.Ho
A	B	2001.08.20	Item 1 was updated: 1.) (Whole document) Description of the module was changed from " MGLS-19264-HT-LED03" to "MGLS-19264-HT-LED03 OR MGLS-19264-HT-G-HV-LED3G."	PHILIP CHENG	Michael Tse
B	C	2004.02.25	Item 1 was updated: (Based on Test Specification: VL-TS-MGLS19264-XX, REV. F, 2003 .09.20). 1.) (Page 5, Figure 1) Module Specification was changed from Rev. 0 to Rev. 1. 2.) (Page 8, Table 5) Supply voltage (LCD), Supply Current (Logic & LCD), and Supply Current (LCD) & VLED were updated.	HELEN HE	YU HAO

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Specification
of
LCD Module Type
Item No.: MGLS19264-07

1. General Description

- 192x 64 dot STN Positive Yellow Transflective Dot Matrix LCD module.
- Viewing direction: 6 O'clock.
- Driving scheme: 1:64 multiplexed drive, 1/9 bias.
- 'Hitachi' HD61202UFS flat pack or equivalent LCD column drivers.
- 'Hitachi' HD61203UFS flat pack or equivalent LCD segment driver.
- Yellow-green LED03 backlight

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	100.0(W) x 60.0(H) x 13.0(D)MAX.	mm
Viewing area	84.0(W) x 31.0(H)	mm
Active area	78.67(W) x 26.19(H)	mm
Display format	192(Horizontal) x 64 (Vertical)	dots
Dot size	0.36(W) x 0.36(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch	0.41(W) x 0.41(H)	mm
Weight:	TBD	grams

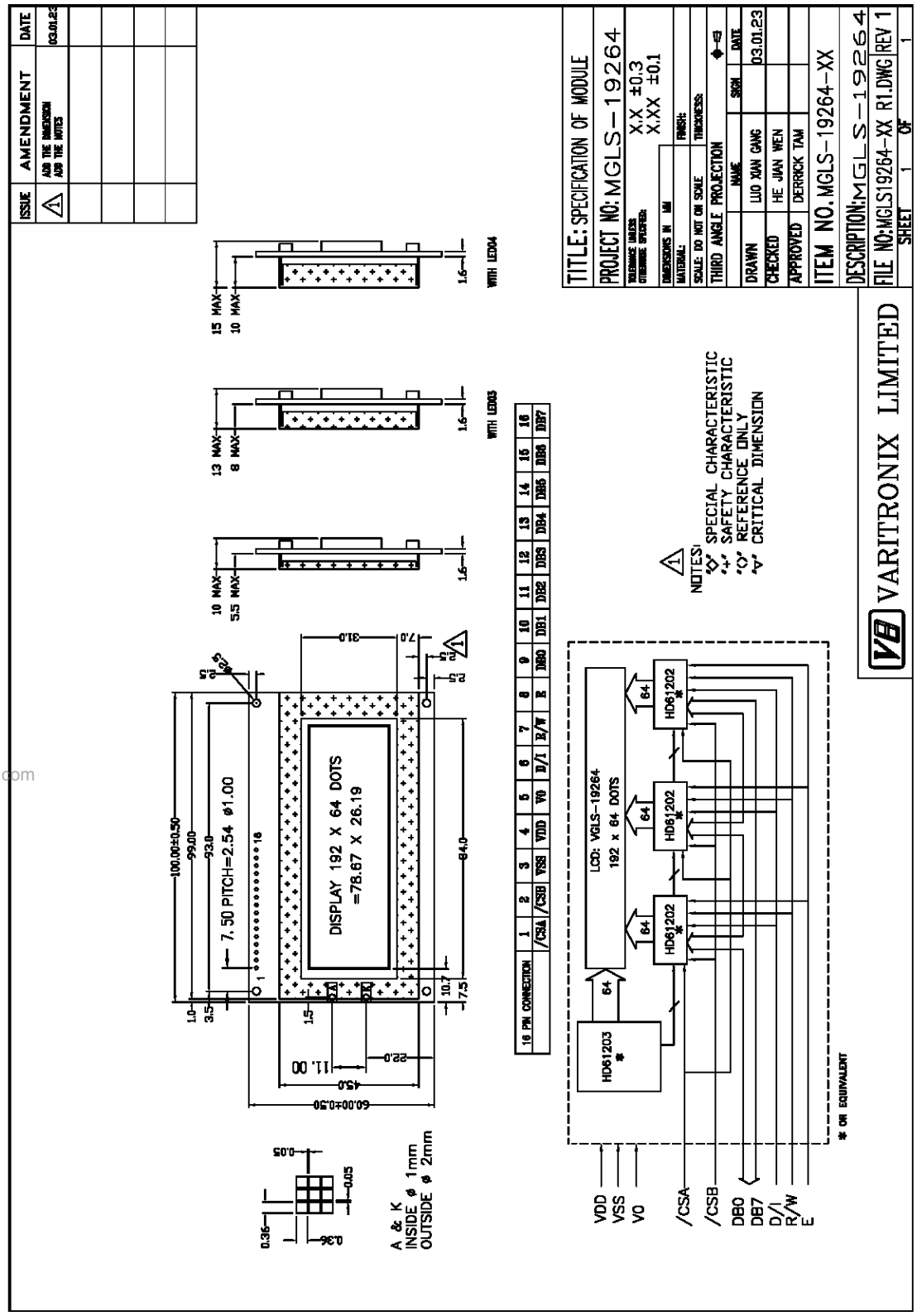

Figure 1: Module Specification

3. Interface signals

Table 2

Pin No.	Symbol	Description
1	/CSA	Chip selection A: In order to interface data for input or output.
2	/CSB	Chip selection B: In order to interface data for input or output.
3	VSS	Ground
4	VDD	Power supply for logic (+5V)
5	V0	Power supply for LCD driver
6	D/I	Data or instruction select input D/I=High: Display RAM data on D0-D7. D/I=Low: Display instruction data on D0-D7.
7	R/W	Read/Write control signal input pin. R/W = High: CPU to read data appearing at DB0 to DB7. R/W = Low: Data of DB0 to DB7 is latched at the falling edge of E.
8	E	Chip Enable. E = High: Read data appears at DB0 to DB7 as E is at high level. E = Low: Write data of DB0 to DB7 is latched at the fall of E.
9	DB0	Data input/output (LSB).
10	DB1	Data input/output.
11	DB2	Data input/output.
12	DB3	Data input/output.
13	DB4	Data input/output.
14	DB5	Data input/output.
15	DB6	Data input/output.
16	DB7	Data input/output (MSB).
-	A	Anode of optional LED backlight.
-	K	Cathode of optional LED backlight.

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings(Ta = 25 ºC)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD–VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD =VDD–V0	-0.3	+17.0	V
Input voltage	Vin	-0.3	VDD+0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to GND = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD –VSS		4.75	5.00	5.25	V
Supply voltage (LCD)	VLCD =VDD –V0	VDD = 5V, Note (1)	14.5	15.0	15.5	V
Input signal voltage (Note 2)	V_{IH}	"High" level, Note (2)	2.0	-	VDD	V
	V_{IL}	"Low" level, Note (2)	0	-	0.8	V
Supply Current (Logic & LCD)	IDD	Character mode, VDD = 5V	-	3.8	5.7	mA
		Checker board mode, VDD = 5V	-	4.0	6.0	mA
Supply Current (LCD)	I0	Character mode, VDD = 5V, Note (1)	-	3.3	5.0	mA
		Checker board mode, VDD = 5V	-	3.5	5.3	mA
Supply voltage of yellow-green LED03 backlight	VLED03	Forward current =140mA Number of LED dies =28	3.9	4.1	4.3	V

Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Note (2): Applies to /CSA, /CSB, E, R/W, DB0~DB7.

5.2 Timing Specifications

At Ta = -20 °C to +70 °C, VDD = +5V±5%, VSS = 0V.

Refer to Fig. 2 & 3, the bus timing diagram.

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
E cycle time	t_{CYC}	1000	-	-	ns
E High Level Width	P_{WEH}	450	-	-	ns
E Low Level Width	P_{WEL}	450	-	-	ns
E Rise Time	tr	-	-	25	ns
E Fall Time	tf	-	-	25	ns
Address Setup Time	t_{AS}	140	-	-	ns
Address Hold Time	t_{AH}	10	-	-	ns
Data Setup Time	t_{DSW}	200	-	-	ns
Data Delay Time	t_{DDR}	-	-	320	ns
Data Hold Time (Write)	t_{DHW}	10	-	-	ns
Data Hold Time (Read)	t_{DHR}	20	-	-	ns

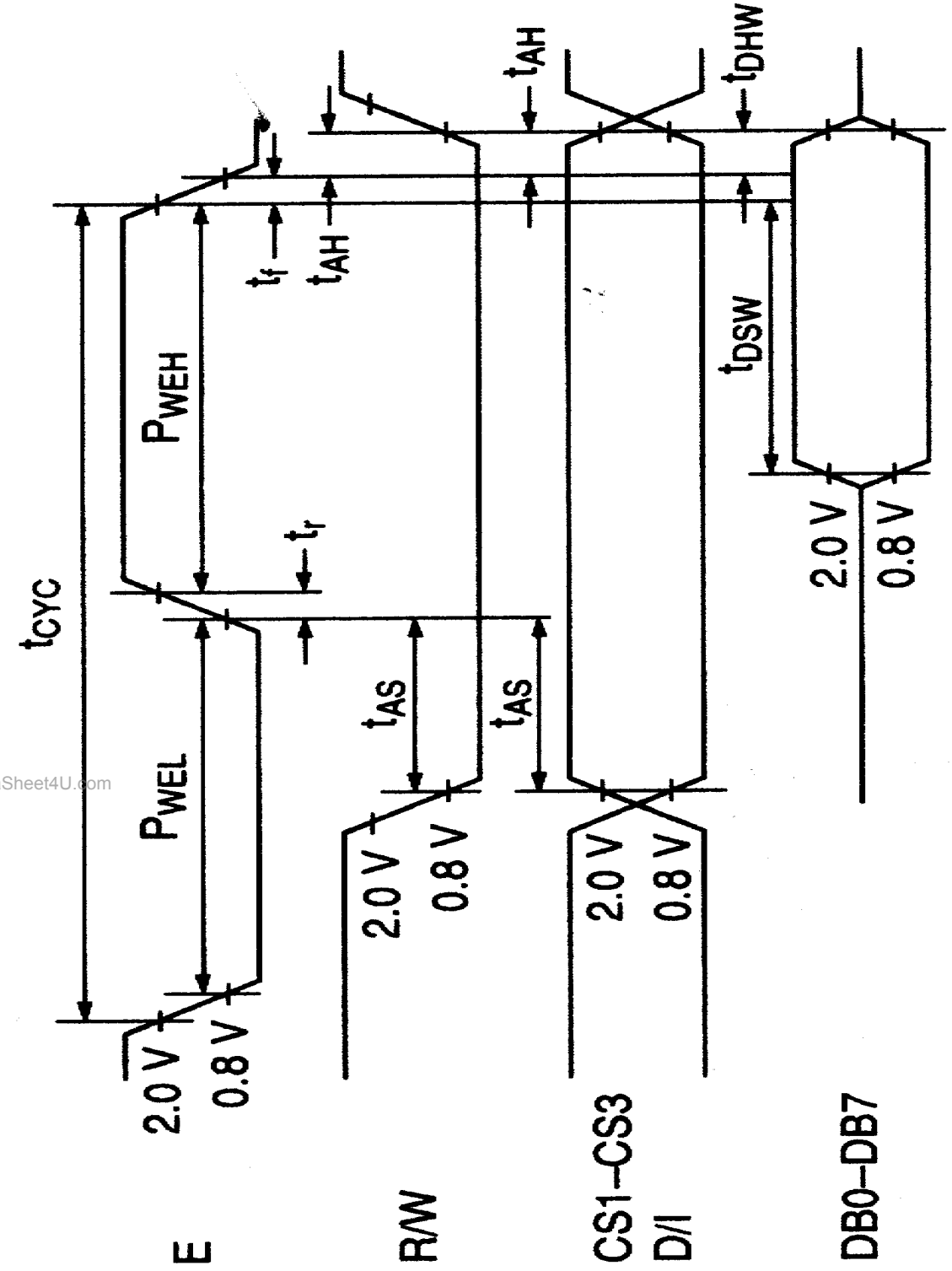

Figure 2: MPU Write Timing

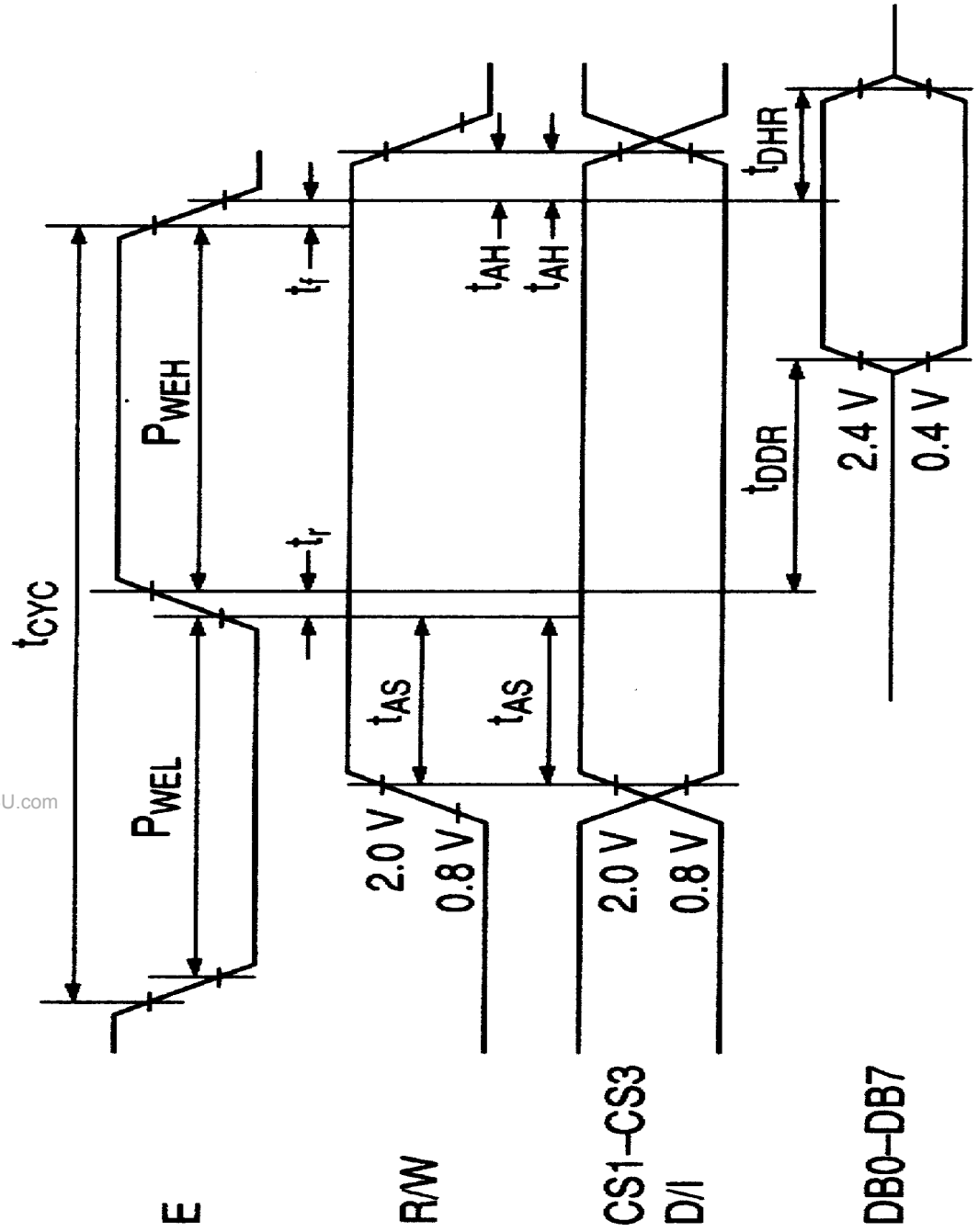

Figure 3: MPU Read Timing

5.3 Timing Diagram of VDD Against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.

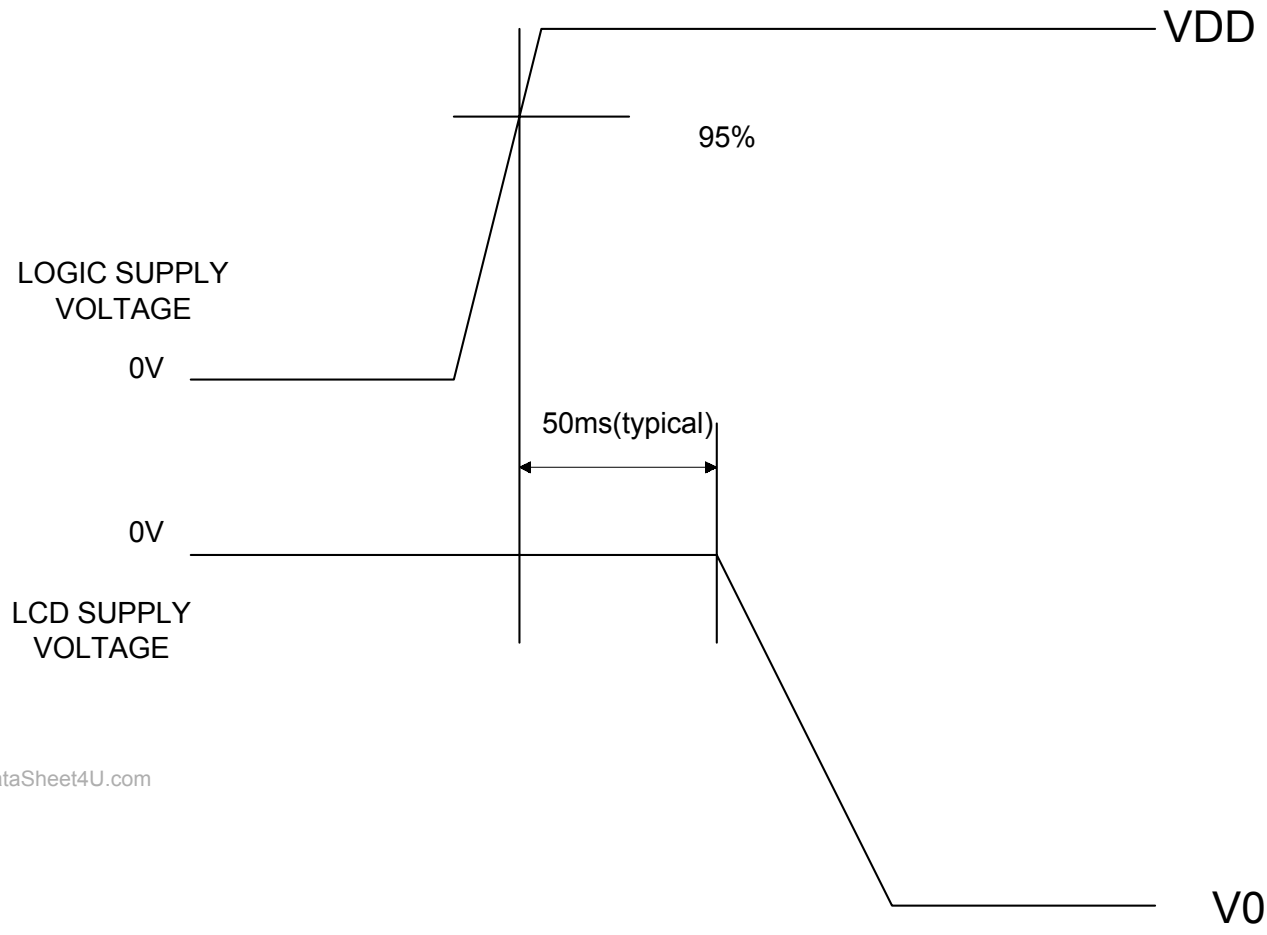

Figure 4: Timing Diagram of VDD Against V0.

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