DS3RTA P and N Rail Device
DS-3 Line Interface
TXC™-02002

PRELIMINARY DATA SHEET

FEATURES

- Provides all functionality required to terminate a DS-3 signal:
  - Clock recovery and filter
  - All line equalization
  - LOS/LOC detection and AIS generation
  - P and N rail NRZ I/O
- Satisfies jitter tolerance requirements on the DS-3 inputs
- Transmits and receives at the STS-1 rate (51.84 MHz) as well as the DS-3 rate (44.736 MHz)
- Provides two DS-3 loopbacks:
  - Receive to transmit (digital)
  - Transmit to receive (analog, no RX amplifiers)
- Meets all applicable ANSI/Bellcore standards:
  - T1.102, 107, 404
  - TR-TSY-000009
- CMOS for low power and enhanced reliability

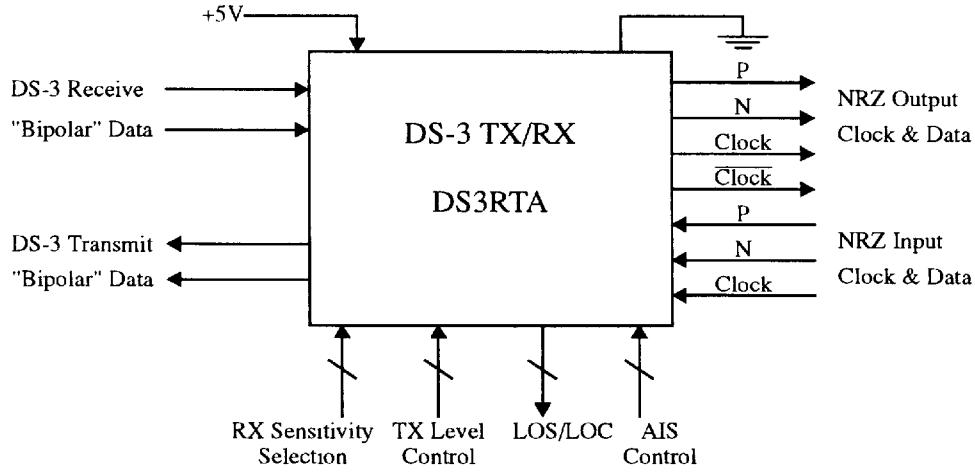
DESCRIPTION

The DS3RTA is similar in function with the DS3RT (TXC-02001). The DS3RTA features P and N rail I/O on the NRZ terminal side of the device. The P and N data outputs correspond exactly to the received DS-3 line data, and the P and N data inputs cause corresponding pulses on the DS-3 line output without regard to line coding.

The DS3RTA efficiently replaces traditional means of receiving and transmitting DS-3 signals, and is especially useful for retrofit applications. It also may be used to transmit and receive SONET STS-1 signals on cable. The DS3RTA accepts a wide receive range of signals, and it has a unique built-in transversal filter for output pulse shaping. Line compensation is reduced to a simple output level setting using a hardware strap. On-chip filter and clock recovery circuits eliminate normally required external components. A built-in framed AIS generator may be enabled in the transmit direction with or without the transmit loss of clock.

APPLICATIONS

- Single board M13 multiplexer
- I/O for DS-3 or SONET DSX
- Fractional T3
- DCS and EDSX
- CSU/DSU



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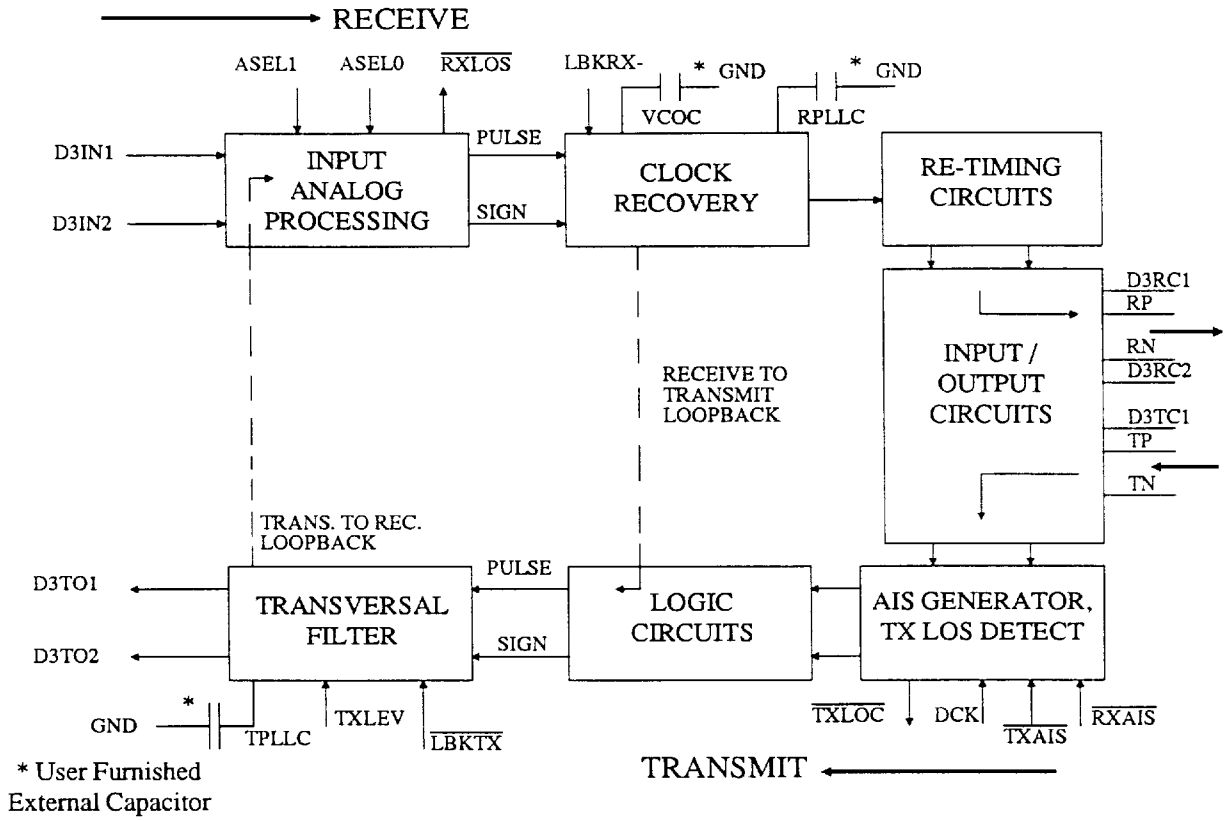
DS3RTA BLOCK DIAGRAM



□ BLOCK DIAGRAM DESCRIPTION

The DS3RTA accepts a wide range of signals, and it has two control leads to adjust the input sensitivity: ASEL0 and ASEL1. The Input Analog Processing block also has built-in thresholds for the detection of ones and zeros on the DS-3 line input. The clock recovery contains a phase-locked loop with substantial digital logic for the clock recovery algorithm.

The receive side of the DS3RTA recovers clock from the B3ZS encoded input signal. The average time to recover clock from the onset of received data is 1 millisecond with the recommended components connected to RPLCC and VCOC. Proper recovery depends only on the amplitude of the received pulses and the setting of the ASEL1 and ASEL2 leads. There is ample overlap of receive sensitivities to ease the selection of ASEL1 and ASEL2 (see the Control Function Table).

If the DS3RTA detects more than 128 zeros from the cable input, then $\overline{\text{RXLOS}}$ becomes valid.

The P and N rail signals on the receive side of the DS3RTA are clocked NRZ duplicates of the B3ZS encoded DS-3 line input signals.

On the transmit side, the NRZ clock and P and N data are examined for loss of clock. If there is loss of clock for about 500 clock cycles then the $\overline{\text{TXLOC}}$ lead goes to ground, and this lead may be connected to the $\overline{\text{TXAIS}}$ lead so that AIS is sent automatically on $\overline{\text{TXLOC}}$ going low. Alternatively, the $\overline{\text{TXAIS}}$ lead may be taken to ground independently to generate a DS-3 AIS or blue signal.

The signals from this block feed a unique built-in transversal filter for output pulse shaping. Line compensation is reduced to a simple output level setting using a hardware strap, TXLEV. The DS-3 line signal corresponds exactly to the clocked NRZ P and N rail input to the DS3RTA.

The resulting output waveform is such that no external compensation networks are required to meet the requirements at the cross connect, regardless of the distance between it and the DS3RTA. The plots on pages 8 and 9 show the pulse shapes at the cross connect for three different cable lengths.

CONTROL FUNCTION TABLE

CONTROL	STATE	FUNCTION
$\overline{\text{LBKRX}}$	Open Gnd.	Loopback disabled, NRZ to NRZ Loopback enabled, NRZ to NRZ
$\overline{\text{LBKTX}}$	Open Gnd.	Loopback disabled, bipolar to bipolar Loopback enabled, bipolar to bipolar
ASEL1, ASLE0	Gnd., Open Open, Gnd. Open, Open Gnd., Gnd.	NOT USED 150 to 360 mv peak input 400 mv to 1 v. peak input 200 to 570 mv input
TXLEV	Open Gnd.	High level transmit Low level transmit
$\overline{\text{TXAIS}}$	Open Gnd.	Transmit AIS disabled Transmit AIS enabled

□ OPERATING CONDITIONS

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} 7V
Input voltage, V_I . . . . . V_{DD}
Operating free-air temperature range , T_A . . . . . -0°C to 70°C
Storage temperature range, T_S . . . . . -65°C to 150°C

Functional Operating Range

V_{DD} = 5 +/- 5%; V_{SS} = 0 (ground) supply voltage
T_A = -0°C to 70°C operating free-air temperature range

INPUT PARAMETERS

PARAMETER	MIN	MAX	UNIT
V_{IH} High-level input voltage	2	V_{DD}+.5	V
V_{IL} Low-level input voltage	V_{SS}-.5	0.8	V
I_{IH} High-level input current		-50	µA
I_{IL} Low-level input current		50	µA
C_{IN} input pin capacitance		10	pF

OUTPUT PARAMETERS

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	V_{DD}=4.75 TO 5.25 V	2.4	V_{DD}-.5	V
V_{OL}	V_{DD}=5.25V	V_{SS}	0.4	V
I_{OH}*	V_{OH} = V_{DD} - .5 V	-1	4	mA
I_{OL}*	V_{OL} = 0.4 V	-2		mA
C_{OUT}			25	pF

* DS-3 NRZ clock and data outputs: I_{OH} Min = -4 mA and I_{OL} Min = 8 mA.

Power Dissipation

At V_{DD} = 5.25 volts and all ports active, I_{DD} Max = 95 milliamps. The maximum power is 500 milliwatts. The nominal power dissipation is 400 milliwatts.

Analog DS-3 Line I/O

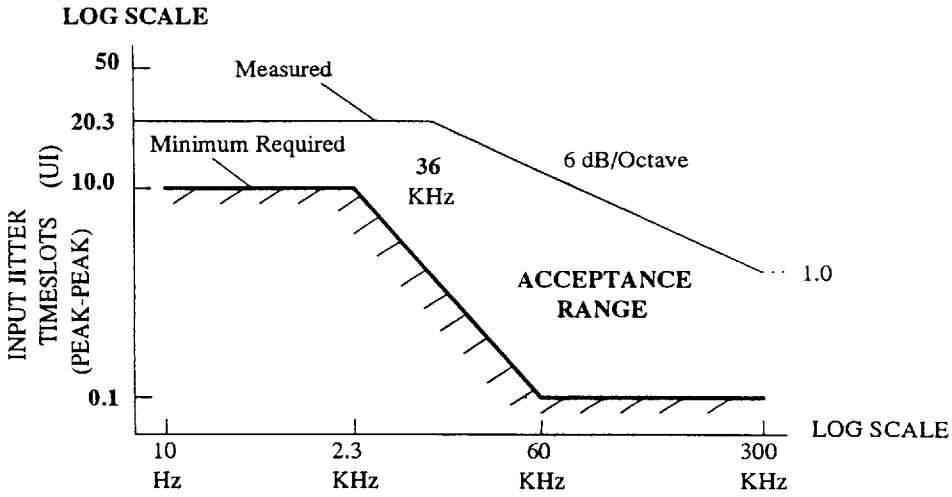
ANALOG INPUT AND OUTPUT PARAMETERS

PARAMETER	MAX	MIN	UNIT
Peak input DS3	1.0	0.15	V
Peak output DS3 (TXLVL open)	1.3	1.1	V*
Peak output DS3 (TXLVL gnd.)	0.95	0.85	V*
Input impedance	7200	4800	Ohms
Output 2nd harmonic (all 1s code)	-30		dB
Frequency range	52	40	MHz

* In order to meet these output voltage levels, the output of the DS3RTA must be loaded with no more than 10 kohms in parallel with 2 pF. See application note TXC-02002-AXXX-AN for details.

DS-3 B3ZS Jitter Tolerance

DS3RTA JITTER TOLERANCE



DS3RTA JITTER ACCOMMODATION CHARACTERISTIC

This jitter tolerance curve applies at the line input of the DS3RTA (pin 29, DS3IN1). The DS3RTA recovers clock, and outputs P and N rail data and clock in the presence of the pictured input jitter characteristic.

With the selected values of components on pin 7, VCOC, the jitter transfer through the DS3RTA is unity or 0 dB and is independent of the frequency of the jitter. Please refer to the DS3RTA Application Note, TXC-02002-AXXX-AN, for component details.

□ TIMING CHARACTERISTICS

DS3RTA TIMING PARAMETERS

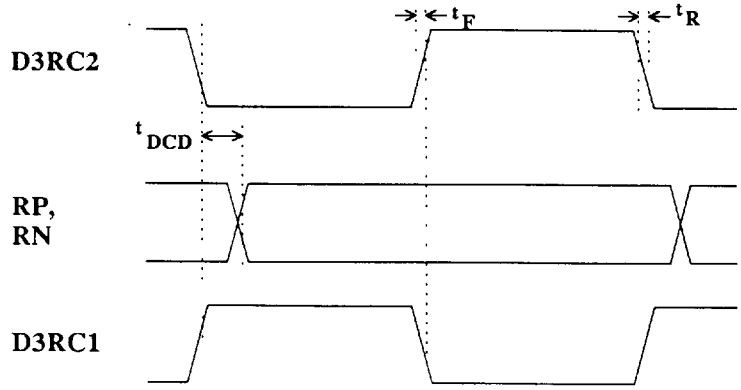
PARAMETER	I/O, CONDITION	MIN	NOM	MAX	UNIT
t_{DCD}, Delay*	Clock high to data change, out	0.6		3	ns
t_{SDC}, Setup	Data to clock low, in	5.5			ns
t_{HCD}, Hold	Data stable after clock low, in	8.5			ns
t_F	Clock fall time		2.5		ns
t_R	Clock rise time		3.5		ns
t_{CYC3}	Nominal DS-3 ck. cycle time		22.35		ns

* With respect to D3RC2, the positive edge reference

A voltage waveform is defined as "high" when it last exceeds VOH or VIH, as appropriate. Likewise, a voltage waveform is defined as "low" when it last goes below VOL or VIL. Timing intervals are defined as the time difference between the crossing of the voltage values on the same or different waveforms.

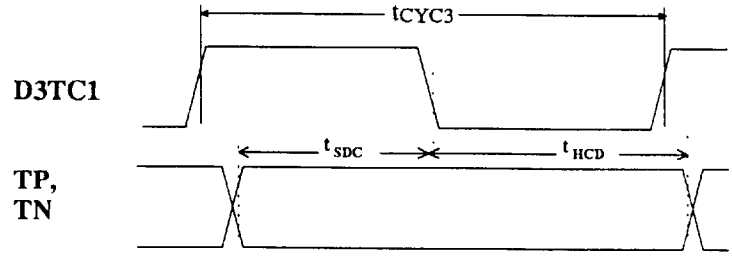
Timing Diagrams

DS-3 OUTPUT TIMING



This figure illustrates the propagation delay of the data on the RP and RN pins with respect to the two clocks, D3RC1 and D3RC2. The only difference between the clocks is that one is the inverse of the other.

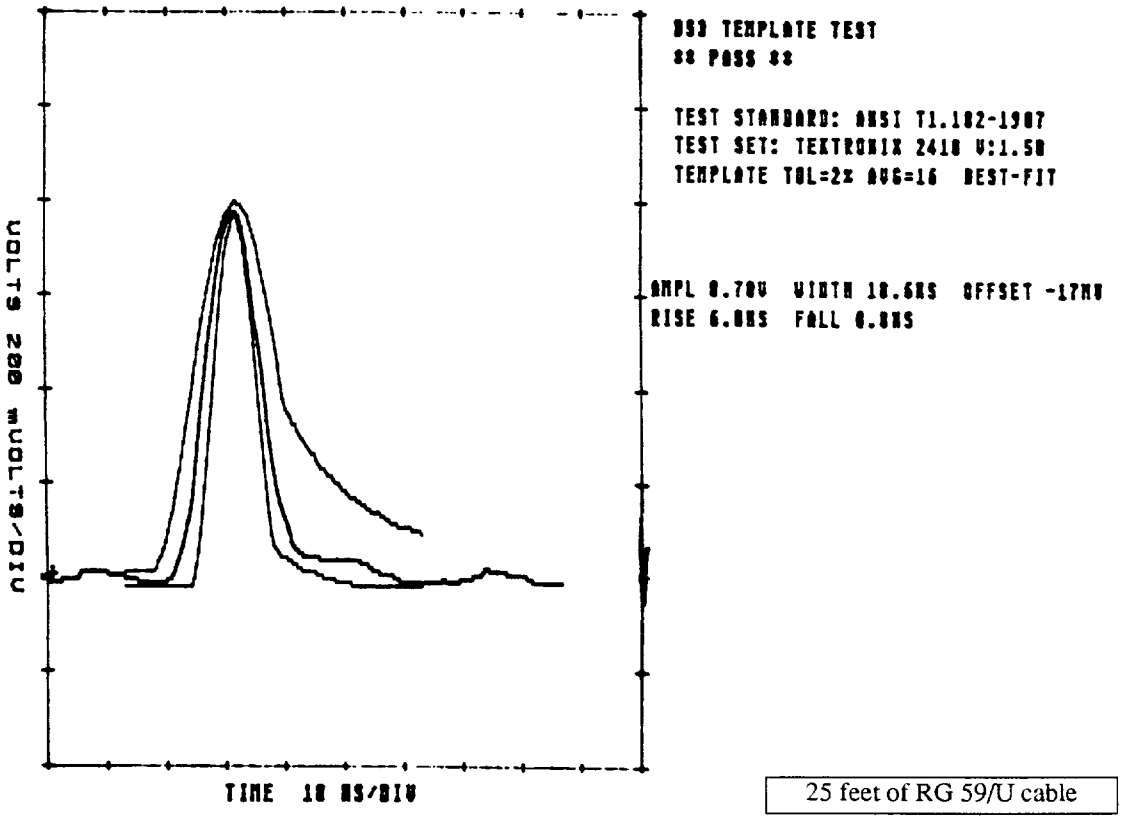
DS-3 INPUT TIMING



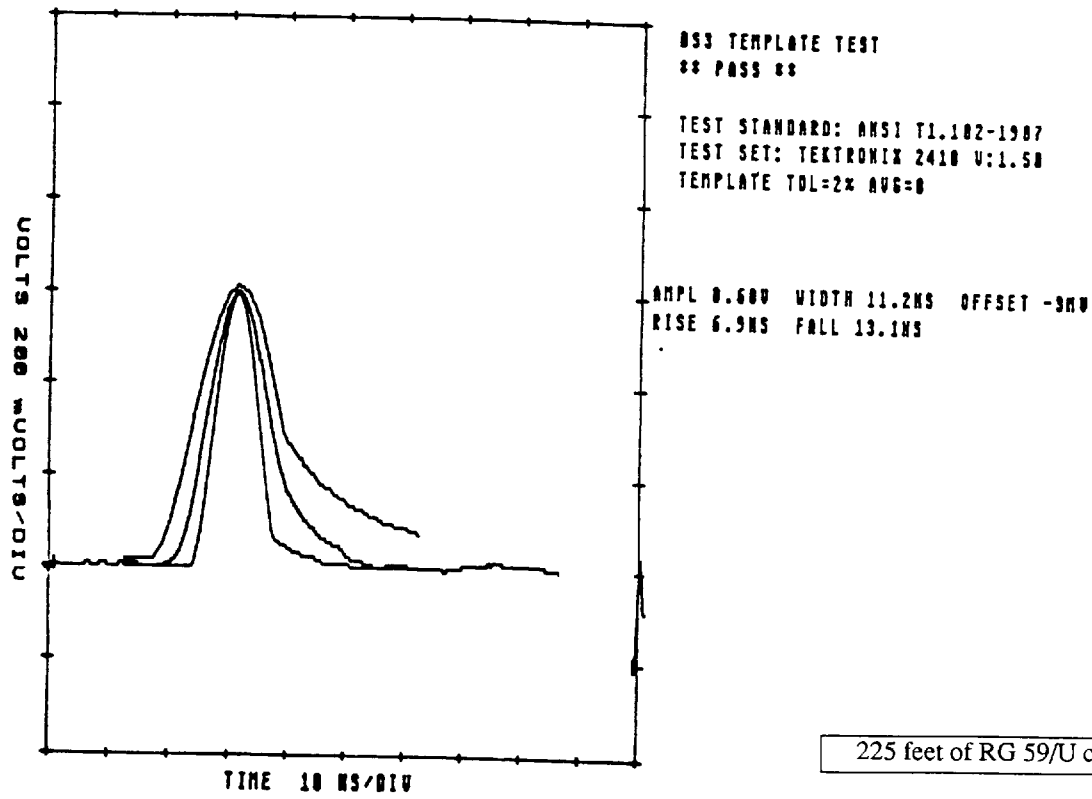
This figure illustrates the DS-3 transmit signal that is on the TP and TN leads of the DS3RTA. The times illustrated in this figure and the figure for the RX data are not necessarily to scale. The values for t_{SCD} and t_{HCD} are given in the timing parameters table. The clock cycle time is nominally 22.35 nanoseconds and both receive and transmit clocks have a duty cycle of 50 +/- 5 %.

PHOTOGRAPHS OF TRANSMITTED WAVEFORM DS3RTA WITH BUFFER AMPLIFIER AND TRANSFORMER

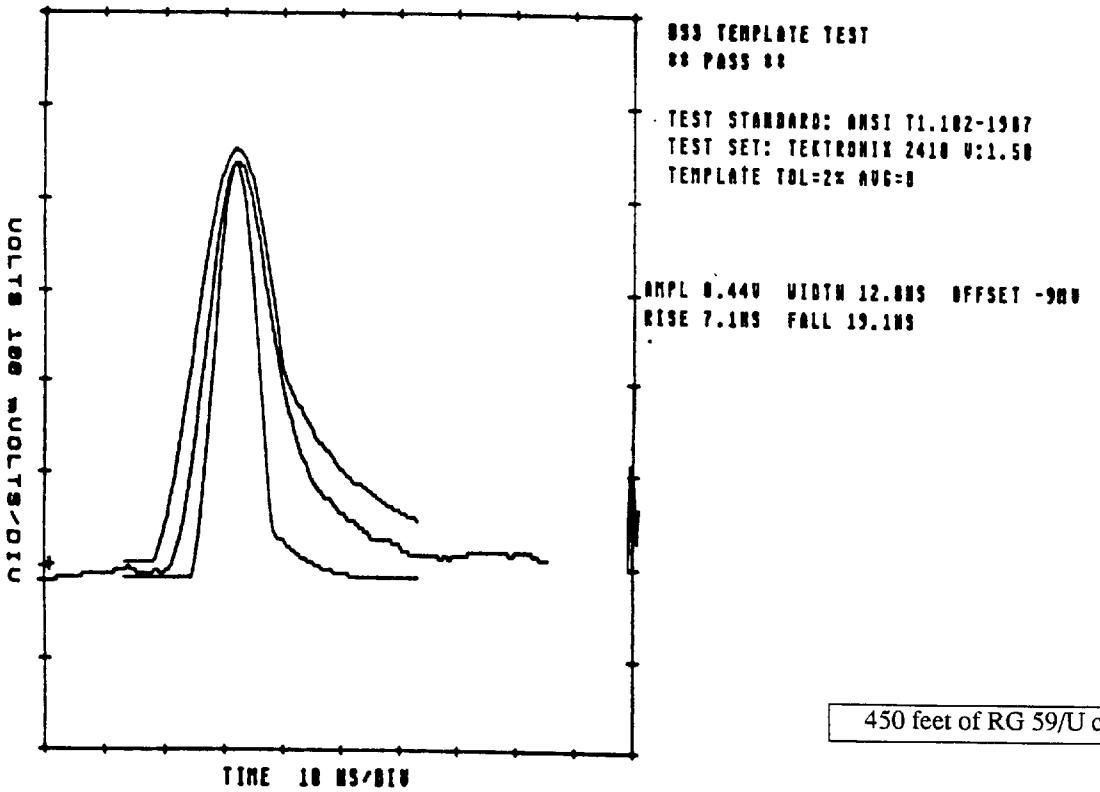
These plots (pages 8 and 9) were made from a Tektronics 2410 Digital Interface Test System using a 2% tolerance on the DS-3 mask given in ANSI T1.102-1987. ANSI has adopted a 3% tolerance on the DS-3 waveform mask. The DS3RTA requires no external build out, and its transmit waveform meets the mask at all lengths up to 450 feet, as required.



The peak amplitude of the pulse at the output of 25 feet of cable is 700 millivolts. The DS3RTA had the TXLEV lead (pin 35) at ground for the low level output (about 770 millivolts). The ANSI requirement at the DSX ranges from 850 to 360 millivolts. The observed amplitudes are within the required range for all cable lengths.



225 feet of RG 59/U cable



450 feet of RG 59/U cable

□ PIN DEFINITION

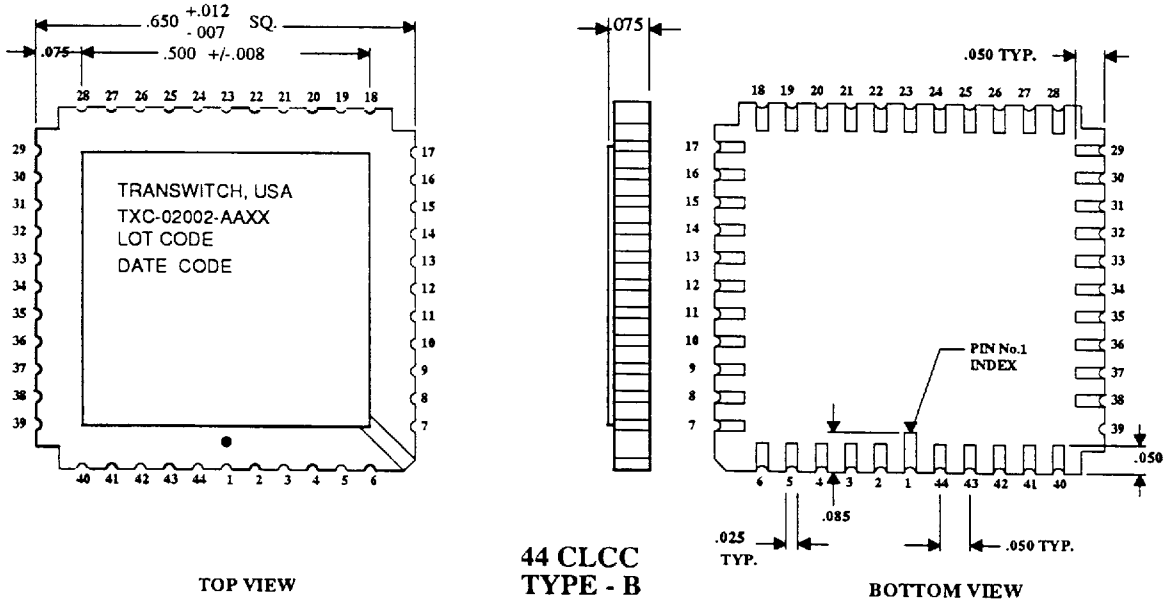
DS3RTA PIN I/O AND FUNCTION

NAME	I/O	PIN NO.	FUNCTION
AVDDT		37	5-volt supply voltage, +/- 5%, analog transmit
AVDDR		23	" " " analog receive
DVDDT		42	" " " digital transmit
DVDDR		10	" " " digital receive
AGNDR		31	Vss or ground, 0 volts reference, analog receive
AGNDR1		16	" " " analog receive (PLL)
AGNDT		36	" " " analog transmit
DGNDR		11, 44	" " " digital receive
DGNDT		6, 8	" " " digital transmit
$\overline{\text{TXLOC}}$	O	2	Ground-true indication of TX loss of clock
VCOC		7	External capacitor connection
DCK	I	9	DS-3 external clock for AIS and loss of clock
RN	O	12	N-rail received data output
RP	O	13	P-rail received data output
D3RC1	O	14	Negative edge clock for output data
DS3C2	O	15	Positive edge clock for output data
RPLLC		17	External capacitor connection
$\overline{\text{RXLOS}}$	O	20	Ground-true indication of receive loss of signal
$\overline{\text{LBKRX}}$	I	24	Strap to ground to loop back RX to TX
$\overline{\text{LBKTX}}$	I	25	Strap to ground to loop back TX to RX
ASEL0	I	26	Receive gain control LSB
ASEL1	I	27	Receive gain control MSB
D3IN1	I	29	DS3 line input (1 of 2)
D3IN2	I	30	DS3 line input (2 of 2)
TPLLC		32	External capacitor connection
D3TO2	O	33	DS3 line output (2 of 2)
D3TO1	O	34	DS3 line output (1 of 2)
TXLEV	I	35	Line transmit level control
D3TC1	I	38	Clock input for transmit P and N rail data
TP	I	40	P-rail transmit data input
TN	I	41	N-rail transmit data input
$\overline{\text{TXAIS}}$	I	43	Strap to ground to enable transmit AIS
N.C.		1,3,4,5,18,19, 21,22,28,39	Connect to GND

□ PACKAGING

Both ceramic and plastic packages are available for the DS3RTA. as illustrated below. The ceramic package has 44-pins (Type B) with pads for surface mounting. A similar plastic package (Type C) is illustrated below. These and other packaging options are available on request from TranSwitch. The TranSwitch family of DS-3 devices operates over the full commercial temperature range of -0°C to 70°C. Burn-in is a customer option.

CERAMIC 44-PIN LEADLESS CHIP CARRIER DRAWING

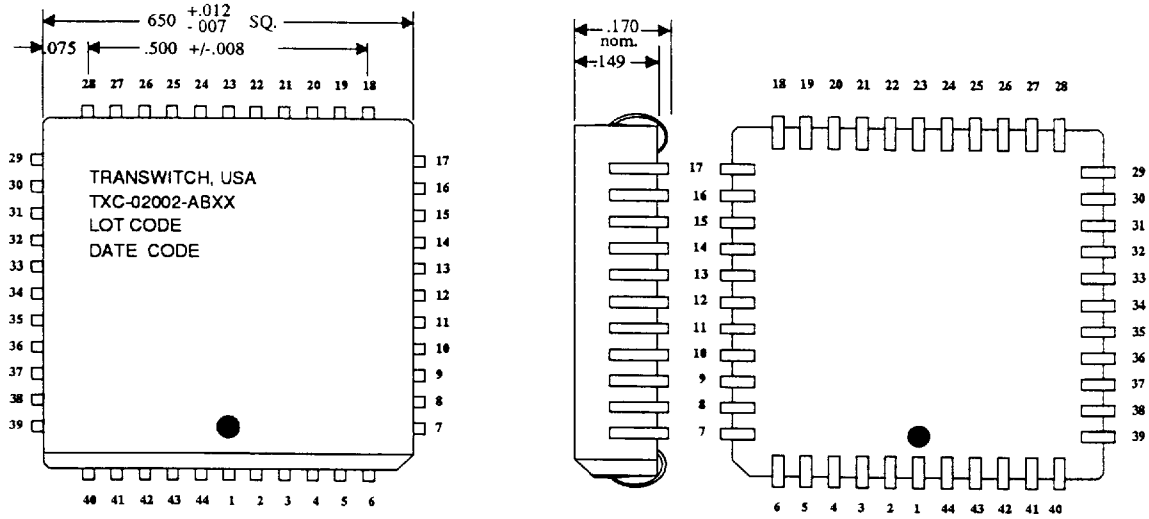


TOP VIEW

44 CLCC
TYPE - B

BOTTOM VIEW

PLASTIC 44-PIN LEADED CHIP CARRIER DRAWING



TOP VIEW

44 PLCC
TYPE - C

BOTTOM VIEW

☐ ORDERING INFORMATION

TXC-02002-ACPL	Plastic 44-Pin Leaded Chip Carrier, 0°C to +70°C
TXC-02002-ACCN	Ceramic 44-Pin Leadless Chip Carrier, 0°C to +70°C

Future: -40°C to +85°C version is planned.

☐ FURTHER INFORMATION

Application information for the DS3RTA is available in TXC-02002-AXXX-AN

☐ RELATED PRODUCTS

- TXC-02001-AXXX DS3RT
  Similar to the DS3RTA, but contains the B3ZS codec and provides NRZ clock and data on the terminal side I/O. It also includes an error estimate output based on coding violations to indicate a 10^{-6} bit error rate. It also includes a raw coding violation output pulse when a coding violation occurs in the received DS-3 data pattern.
- TXC-02003-AXXX DS3RX
  Similar to the DS3RT (TXC-02001), but has the DS-3 receive function only.