

DUAL 4-BIT LATCH



The HEF4508B is a dual 4-bit latch, which consists of two identical independent 4-bit latches with separate strobe (ST), master reset (MR), output-enable input ($\overline{EO}$) and 3-state outputs (O).

With the ST input in the HIGH state, the data on the D inputs appear at the corresponding outputs provided $\overline{EO}$ is LOW. Changing the ST input to the LOW state locks the data into the latch. A HIGH on the reset line forces the outputs to a LOW level regardless of the state of the ST input. The 3-state outputs are controlled by the output-enable input. A HIGH on $\overline{EO}$ causes the outputs to assume a high impedance OFF-state regardless of other input conditions. This allows the outputs to interface directly with bus orientated systems. When $\overline{EO}$ is LOW the contents of the latches are available at the outputs.

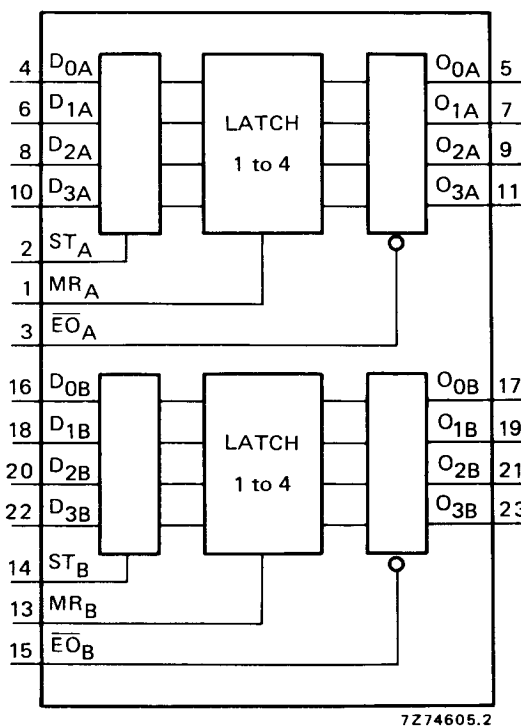


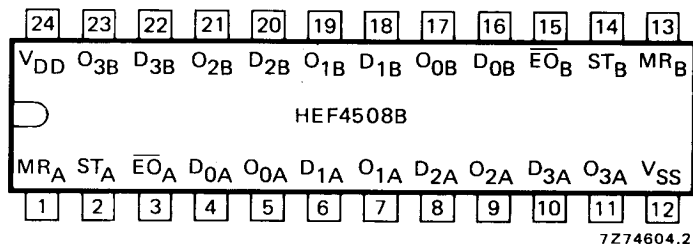
Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications





7Z74604.2

Fig. 2 Pinning diagram.

HEF4508BP : 24-lead DIL; plastic (SOT-101A).

HEF4508BD: 24-lead DIL; ceramic (cerdip) (SOT-94).

HEF4508BT: 24-lead mini-pack; plastic
(SO-24; SOT-137A).

PINNING

D0A to D3A, D03 to D3B data inputs

ST_A, ST_B strobe inputs

MR_A, MR_B master reset inputs

EO_A, EO_B output enable inputs

O0A to O3A, O0B to O3B 3-state outputs

FUNCTION TABLE

inputs				output
MR	ST	EO	D _n	O _n
L	H	L	H	H
L	H	L	L	L
L	L	L	X	latched
H	X	L	X	L
X	X	H	X	Z

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

Z = high impedance OFF state

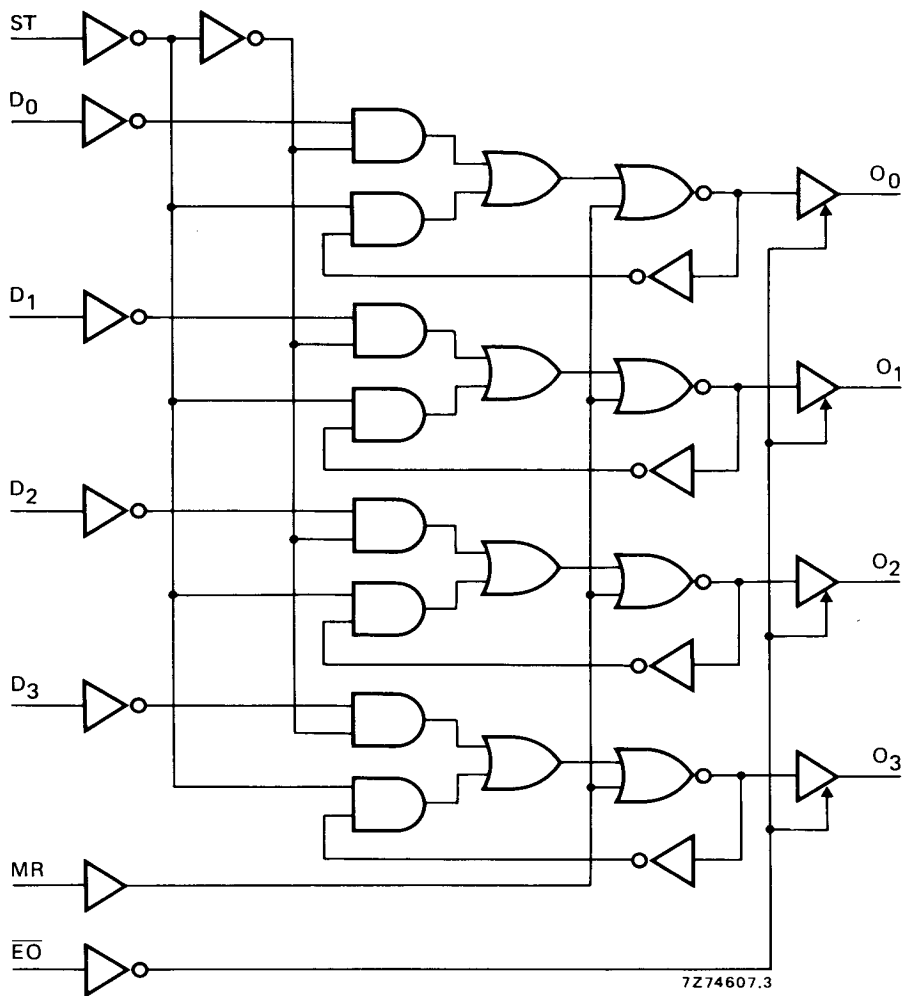


Fig. 3 Logic diagram (one 4-bit latch).

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$; see also waveforms Fig. 4.

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays							
ST → O _n HIGH to LOW	5	t _{PHL}		115	230	ns	88 ns + (0,55 ns/pF) C _L
	10			50	100	ns	39 ns + (0,23 ns/pF) C _L
	15			35	70	ns	27 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		115	230	ns	88 ns + (0,55 ns/pF) C _L
	10			50	100	ns	39 ns + (0,23 ns/pF) C _L
	15			35	70	ns	27 ns + (0,16 ns/pF) C _L
D _n → O _n HIGH to LOW	5	t _{PHL}		95	190	ns	68 ns + (0,55 ns/pF) C _L
	10			40	80	ns	29 ns + (0,23 ns/pF) C _L
	15			30	60	ns	22 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		95	190	ns	68 ns + (0,55 ns/pF) C _L
	10			40	80	ns	29 ns + (0,23 ns/pF) C _L
	15			30	60	ns	22 ns + (0,16 ns/pF) C _L
MR → O _n HIGH to LOW	5	t _{PHL}		100	200	ns	73 ns + (0,55 ns/pF) C _L
	10			40	80	ns	29 ns + (0,23 ns/pF) C _L
	15			30	60	ns	22 ns + (0,16 ns/pF) C _L
Output transition times							
HIGH to LOW	5	t _{THL}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10			30	60	ns	9 ns + (0,42 ns/pF) C _L
	15			20	40	ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10			30	60	ns	9 ns + (0,42 ns/pF) C _L
	15			20	40	ns	6 ns + (0,28 ns/pF) C _L
3-state propagation delays							
Output enable times							
EO → O _n HIGH	5	t _{PZH}		45	90	ns	
	10			20	40	ns	
	15			18	36	ns	
LOW	5	t _{PZL}		45	90	ns	
	10			20	40	ns	
	15			18	36	ns	
Output disable times							
EO → O _n HIGH	5	t _{PHZ}		35	70	ns	
	10			20	40	ns	
	15			18	36	ns	
LOW	5	t _{PLZ}		45	90	ns	
	10			20	40	ns	
	15			18	36	ns	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Minimum ST pulse width; HIGH	5	t_{WSTH}	50	25	ns	see also waveforms Fig. 4
	10		30	15	ns	
	15		20	10	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	40	20	ns	
	10		24	12	ns	
	15		20	10	ns	
Recovery time for MR	5	t_{RMR}	20	0	ns	
	10		20	0	ns	
	15		15	0	ns	
Set-up times $D_n \rightarrow ST$	5	t_{su}	35	10	ns	
	10		25	5	ns	
	15		20	0	ns	
Hold times $D_n \rightarrow ST$	5	t_{hold}	20	0	ns	
	10		20	0	ns	
	15		15	0	ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$9\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$25\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

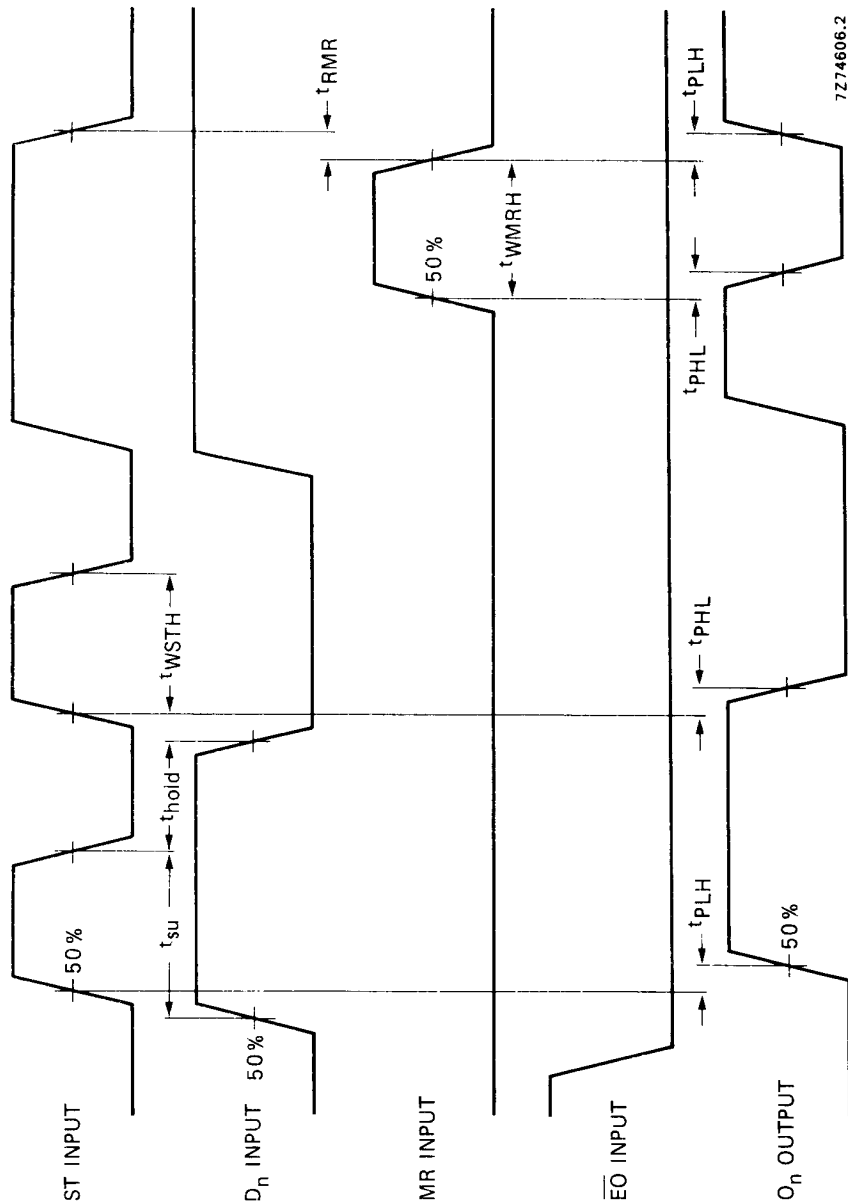


Fig. 4 Waveforms showing minimum ST and MR pulse widths, set-up and hold times for D_n to ST, recovery time for MR and propagation delays from ST to O_n, D_n to O_n and MR to O_n.

APPLICATION INFORMATION

Some examples of application for the HEF4508B are:

- Buffer storage
- Holding registers
- Data storage and multiplexing

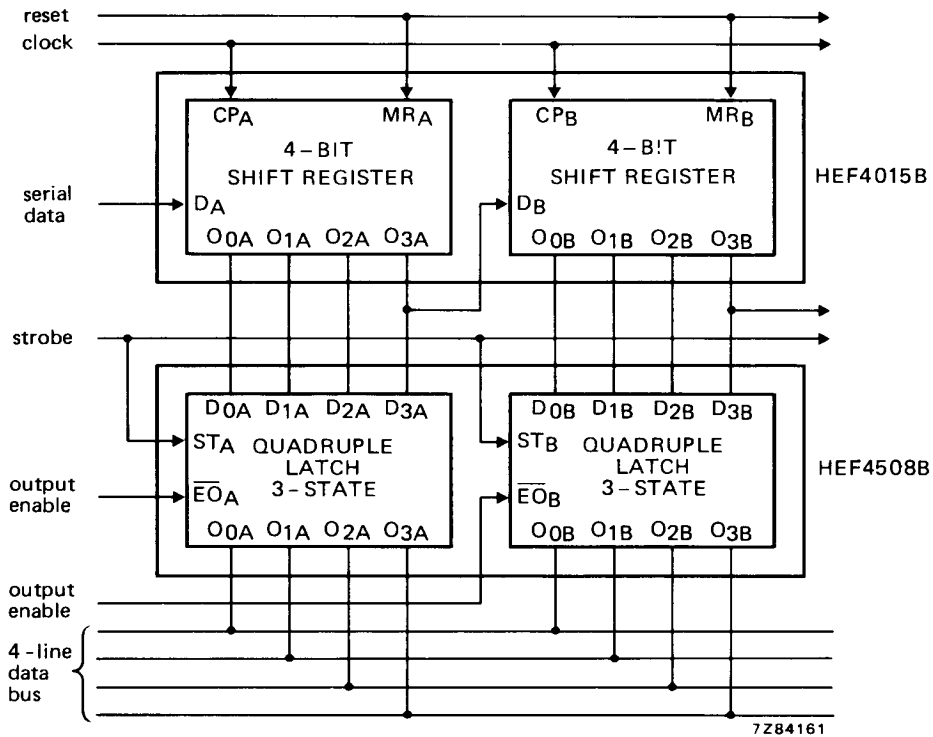


Fig. 5 Example of a bus register using HEF4508B and HEF4015B.

APPLICATION INFORMATION (continued)

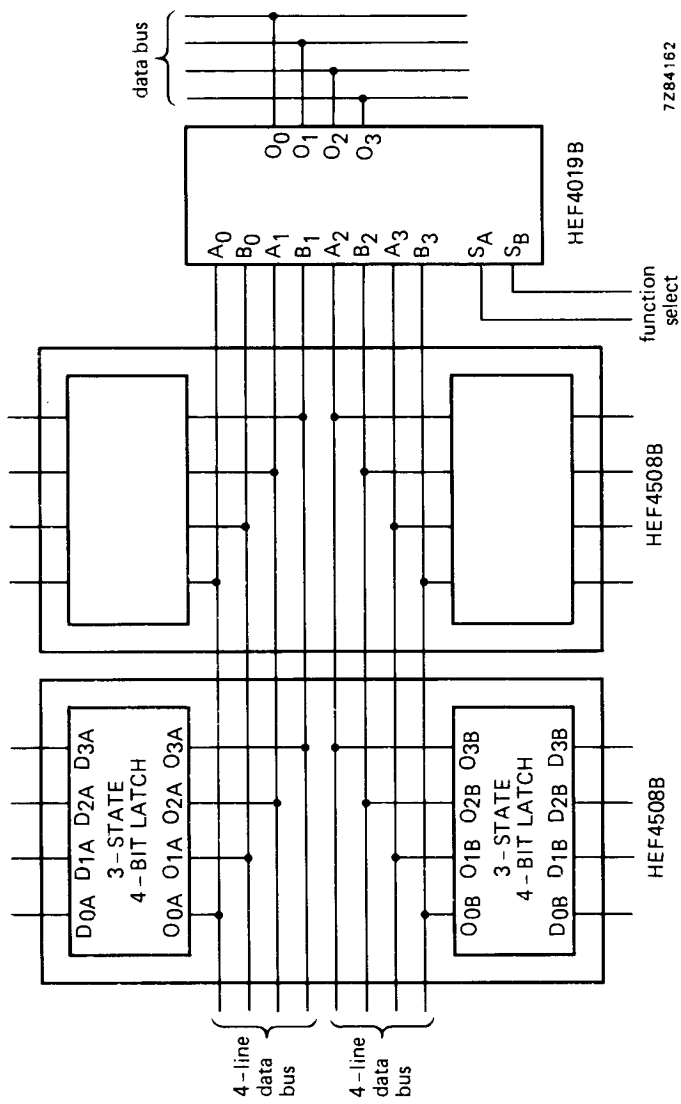


Fig. 6 Example of a dual multiplexed bus register with function select using two HEF4508B and one HEF4019B.

FUNCTION SELECT

SA	SB	function
L	L	inhibit (all L)
H	L	select A bus
L	H	select B bus
H	H	$A_1 + B_1$