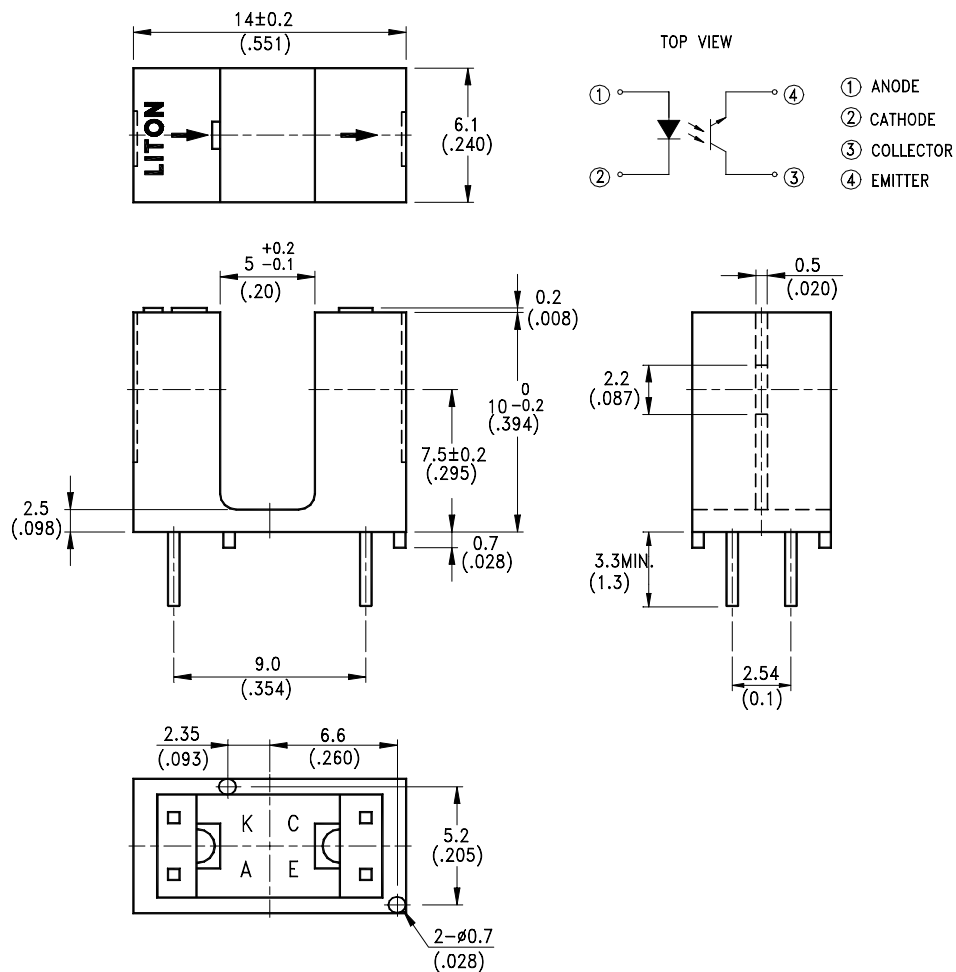


FEATURES

- * NON-CONTACT SWITCHING.
- * FOR DIRECT PC BOARD OR DUAL-IN-LINE SOCKET MOUNTING.
- * FAST SWITCHING SPEED.

PACKAGE DIMENSIONS



NOTES:

1. All dimensions are in millimeters (inches).
2. Tolerance is ±0.25mm(.010") unless otherwise noted.
3. Lead spacing is measured where the leads emerge from the package.

ABSOLUTE MAXIMUM RATINGS AT T_A=25°C

PARAMETER	MAXIMUM RATING	UNIT
INPUT LED		
Power Dissipation	75	mA
Peak Forward Current (300pps, 10 μ S pulse)	1	A
Continuous Forward Current	60	mA
Reverse Voltage	5	V
OUTPUT PHOTOTRANSISTOR		
Power Dissipation	100	mW
Collector-Emitter Voltage	30	V
Emitter-Collector Voltage	5	V
Collector Current	20	mA
Operating Temperature Range	-25°C to + 85°C	
Storage Temperature Range	-40°C to + 100°C	
Lead Soldering Temperature [1.6mm(.063") From Body]	260°C for 5 Seconds	

ELECTRICAL OPTICAL CHARACTERISTICS AT TA=25°C

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
INPUT LED							
Forward Voltage		V_F		1.2	1.6	V	$I_F = 20\text{mA}$
Reverse Current		I_R			100	μA	$V_R = 5\text{V}$
OUTPUT PHOTOTRANSISTOR							
Collector-Emitter Dark Current		I_{CEO}			100	nA	$V_{CE} = 10\text{V}$
COUPLER							
Collector-Emitter Saturation Voltage		$V_{CE(SAT)}$			0.4	V	$I_C = 0.25\text{mA}$ $I_F = 20\text{mA}$
On State Collector Current		$I_{C(ON)}$	0.6			mA	$V_{CE} = 5\text{V}$ $I_F = 20\text{mA}$
Response Time	Rise Time	T_r		3	15	μS	$V_{CE} = 5\text{V}, I_C = 2\text{mA}$ $R_L = 100\Omega$
	Fall Time	T_f		4	20		

TYPICAL ELECTRICAL / OPTICAL CHARACTERISTICS CURVES

(25°C Ambient Temperature Unless Otherwise Noted)

Fig.1 Power Dissipation vs.
Ambient Temperature

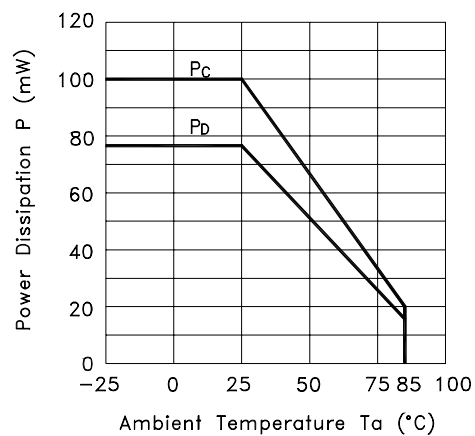


Fig.2 Forward Current vs.
Forward Voltage

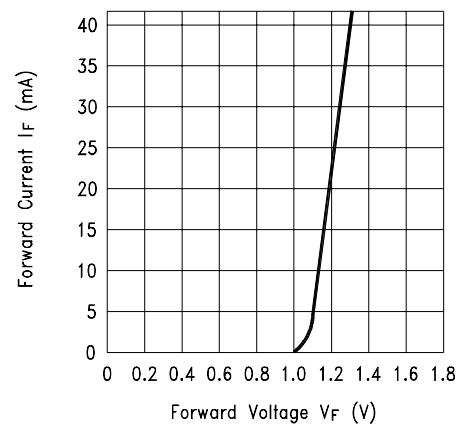
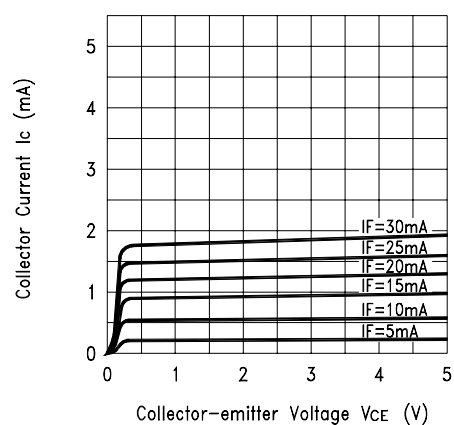


Fig.3 Collector Current vs.
Collector-emitter Voltage



TYPICAL ELECTRICAL / OPTICAL CHARACTERISTICS CURVES

(25°C Ambient Temperature Unless Otherwise Noted)

Fig.4 Collector Current vs. Ambient Temperature

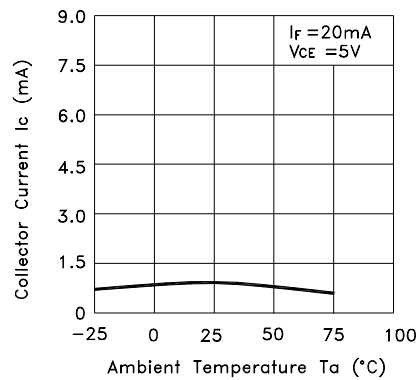


Fig.5 Collector-emitter Saturation Voltage vs. Ambient Temperature

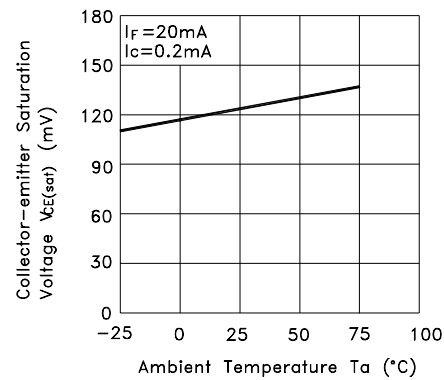
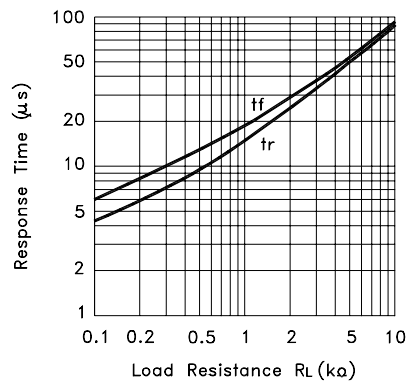


Fig.6 Response Time vs. Load Resistance



Test Circuit for Response Time

