TOSHIBA

THM72V2010AG/ATG-60/70

PRELIMINARY

2,097,152 WORDS X 72 BIT DYNAMIC RAM MODULE

Description

The THM72V2010AG/ATG is a 2,097,152 words by 72 bits dynamic RAM module which assembled 9 pcs of TC51V17800ANJ/ANT on the printed circuit board. This module is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

Features

- 2,097,152 words by 72 bits organization
- Fast access time and cycle time
- Single power supply of 3.3V±5%
- Low Power
  - 4,095mW MAX. Operating
  - (THMxxxxxx-60)
  - 3,470mW MAX. Operating
  - (THMxxxxxx-70)
  - 50.4mW MAX. Standby
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 2,048 refresh cycles/32ms
- Package: 168pin Gold Contact
  THM72V2010AG-x SOJ type
  THM72V2010ATG-x TSOP type

Key Parameters

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

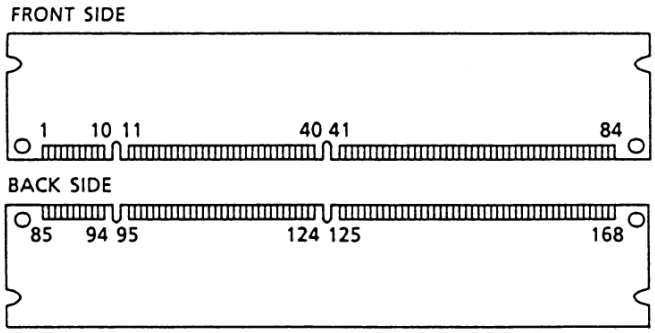
	-60	-70
PD0	"H"	"H"
PD1	"L"	"L"
PD2	"L"	"L"
PD3	"H"	"H"
PD4	"L"	"L"
PD5	"H"	"L"
PD6	"H"	"H"
PD7	"L"	"L"
ID0	V_{SS}	V_{SS}
ID1	V_{SS}	V_{SS}

Note "H": High Level (buffered)
"L": Low Level (buffered)

Pin Name

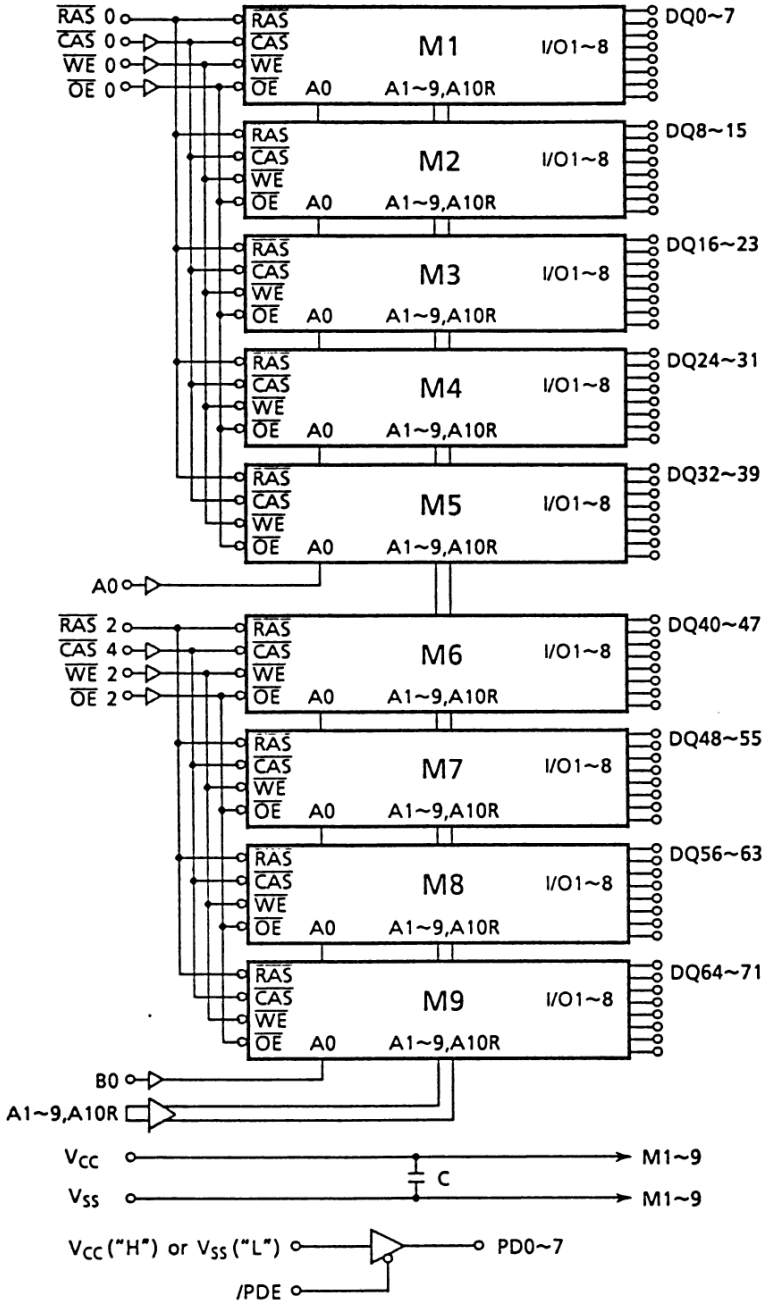
B0, A0 ~ 9, A10R	Address Inputs
DQ0 ~ 71	Data Input/Outputs
$\overline{RAS}$0, 2	Row Address Strobe
$\overline{CAS}$0, 4	Column Address Strobe
$\overline{WE}$0, 2	Write Enable
$\overline{OE}$0, 2	Output Enable
V_{CC}	Power (+3.3V)
V_{SS}	Ground
PD0 ~ 7	Presence Detect Pin
ID0, 1	ID bit
NC	No Connection

Pin Connection (Top View)



1	V_{SS}	85	V_{SS}	18	V_{CC}	102	V_{CC}	35	A4	119	A5	52	DQ18	136	DQ54	69	DQ28	153	DQ64
2	DQ0	86	DQ36	19	DQ14	103	DQ50	36	A6	120	A7	53	DQ19	137	DQ55	70	DQ29	154	DQ65
3	DQ1	87	DQ37	20	DQ15	104	DQ51	37	A8	121	A9	54	V_{SS}	138	V_{SS}	71	DQ30	155	DQ66
4	DQ2	88	DQ38	21	DQ16	105	DQ52	38	A10R	122	NC	55	DQ20	139	DQ56	72	DQ31	156	DQ67
5	DQ3	89	DQ39	22	DQ17	106	DQ53	39	NC	123	NC	56	DQ21	140	DQ57	73	V_{CC}	157	V_{CC}
6	V_{CC}	90	V_{CC}	23	V_{SS}	107	V_{SS}	40	V_{CC}	124	V_{CC}	57	DQ22	141	DQ58	74	DQ32	158	DQ68
7	DQ4	91	DQ40	24	NC	108	NC	41	NC	125	NC	58	DQ23	142	DQ59	75	DQ33	159	DQ69
8	DQ5	92	DQ41	25	NC	109	NC	42	NC	126	B0	59	V_{CC}	143	V_{CC}	76	DQ34	160	DQ70
9	DQ6	93	DQ42	26	V_{CC}	110	V_{CC}	43	V_{SS}	127	V_{SS}	60	DQ24	144	DQ60	77	DQ35	161	DQ71
10	DQ7	94	DQ43	27	$\overline{WE}$0	111	NC	44	$\overline{OE}$2	128	NC	61	NC	145	NC	78	V_{SS}	162	V_{SS}
11	DQ8	95	DQ44	28	$\overline{CAS}$0	112	NC	45	$\overline{RAS}$2	129	NC	62	NC	146	NC	79	PD0	163	PD1
12	V_{SS}	96	V_{SS}	29	NC	113	NC	46	$\overline{CAS}$4	130	NC	63	NC	147	NC	80	PD2	164	PD3
13	DQ9	97	DQ45	30	$\overline{RAS}$0	114	NC	47	NC	131	NC	64	NC	148	NC	81	PD4	165	PD5
14	DQ10	98	DQ46	31	$\overline{OE}$0	115	NC	48	$\overline{WE}$2	132	$\overline{PDE}$	65	DQ25	149	DQ61	82	PD6	166	PD7
15	DQ11	99	DQ47	32	V_{SS}	116	V_{SS}	49	V_{CC}	133	V_{CC}	66	DQ26	150	DQ62	83	ID0	167	ID1
16	DQ12	100	DQ48	33	A0	117	A1	50	NC	134	NC	67	DQ27	151	DQ63	84	V_{CC}	168	V_{CC}
17	DQ13	101	DQ49	34	A2	118	A3	51	NC	135	NC	68	V_{SS}	152	V_{SS}				

Block Diagram



Absolute Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}	Input Voltage	-0.3 ~ V_{CC} + 0.3	V	1
V_{OUT}	Output Voltage	-0.3 ~ V_{CC} + 0.3	V	1
V_{CC}	Power Supply Voltage	-0.5 ~ 4.6	V	1
T_{OPR}	Operating Temperature	0 ~ 70	°C	1
T_{STG}	Storage Temperature	-55 ~ 125	°C	1
P_D	Power Dissipation	3.9	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

Recommended DC Operating Conditions (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	3.13	3.3	3.47	V	2
V_{IH}	Input High Voltage	2.2	-	V_{CC} + 0.3*	V	2
V_{IL}	Input Low Voltage	-0.3**	-	0.8	V	2

*V_{CC} + 1.2V at pulse width ≤ 20ns (pulse width is measured at V_{CC}).
**-1.2V at pulse width ≤ 20ns (pulse width is measured at V_{SS}).

DC Electrical Characteristics (V_{CC} = 3.3V±5%, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1180	mA	3, 4 5
		THMxxxxxx-70	-	1000		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	19	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1180	mA	3, 5
		THMxxxxxx-70	-	1000		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	685	mA	3, 4 5
		THMxxxxxx-70	-	595		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	14.5	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1180	mA	3, 5
		THMxxxxxx-70	-	1000		
$I_{I\ (L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤V_{CC}, All Other Pins Not Under Test=0V)		-10	10	µA	
$I_{O\ (L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, (0V≤V_{OUT}≤V_{CC})		-10	10	µA	
V_{OH}	OUTPUT LEVEL Output “H” Level Voltage (I_{OUT}= -2mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output “L” Level Voltage (I_{OUT}=2mA)		-	0.4	V	

Capacitance (V_{CC} = 3.3V±5%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (B0, A0 ~ A9, A10R)	-	13	$_{P}$F
C_{I2}	Input Capacitance ($\overline{WE}$0, 2)	-	10	
C_{I3}	Input Capacitance ($\overline{RAS}$0, 2)	-	33	
C_{I4}	Input Capacitance ($\overline{CAS}$0, 4)	-	10	
C_{I5}	Input Capacitance ($\overline{OE}$0, 2)	-	10	
C_{I6}	Input Capacitance ($\overline{PDE}$)	-	13	
C_{DQ}	I/O Capacitance (DQ0 ~ 71)	-	30	

Electrical Characteristics and Recommended AC Operating Conditions (V_{CC} = 3.3V±5%, Ta = 0 ~ 70°C) (Notes 6,7,8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		UNIT	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	-	190	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	95	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	9, 14
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	45	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	25	15	30	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	10	-	10	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	ns	

Electrical Characteristics and Recommended AC Operating Conditions (Cont)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		UNIT	NOTES
		MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	20	-	ns	12
t_{REF}	Refresh Period	-	32	-	32	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	-	55	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	90	-	100	-	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	-	70	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	70	-	75	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	20	-	30	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	15	-	15	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	15	-	15	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	15	-	15	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	ns	
t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{PD}	$\overline{PDE}$ to Presence Detect Data in Low-Z	-	10	-	10	ns	
t_{PDOFF}	Presence Detect Data turn off Delay Time from $\overline{PDE}$	1	-	1	-	ns	

Electrical Characteristics and Recommended AC Operating Conditions (V_{CC} = 3.3V±5%, Ta = 0 ~ 70°C) (Notes 6,7,8)

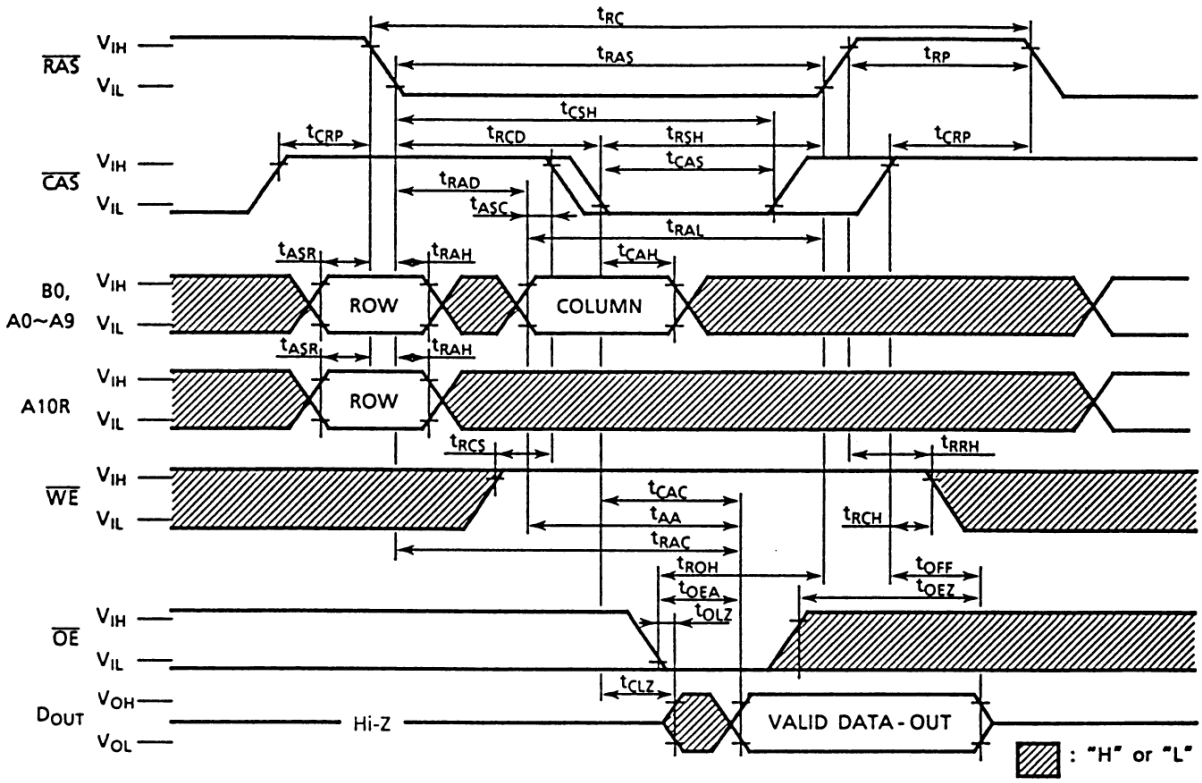
SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		UNIT	NOTES
		MIN	MAX	MIN	MAX	ns	
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	30	ns	9, 14
t_{AA}	Access Time from Column Address	-	40	-	45	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	50	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold	45	-	50	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead	40	-	45	-	ns	

Notes:

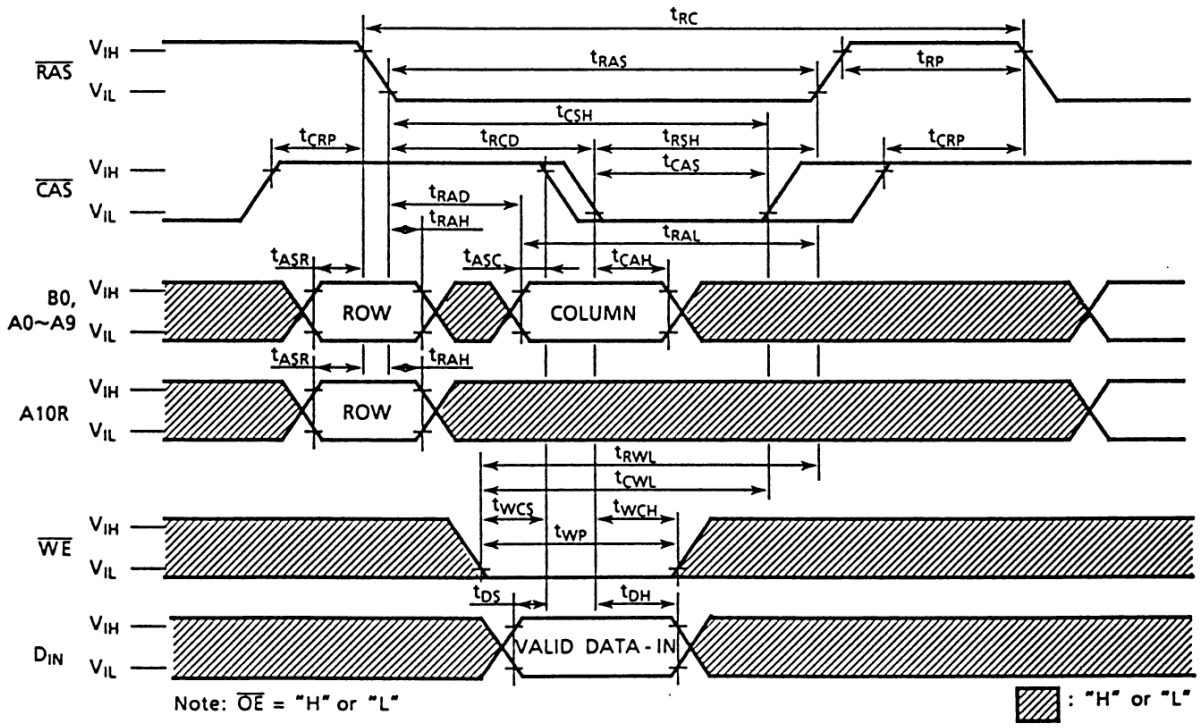
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).
6. An initial pause of 500μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. When the internal refresh counter is used, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume t_T=5ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. This parameter is measured with a load equivalent to 100pF and at V_{OH}=2.0V (I_{OUT}= -2mA), V_{OL}=2.0V (I_{OUT}=2mA).
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWD} \geq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.27

Timing Waveforms

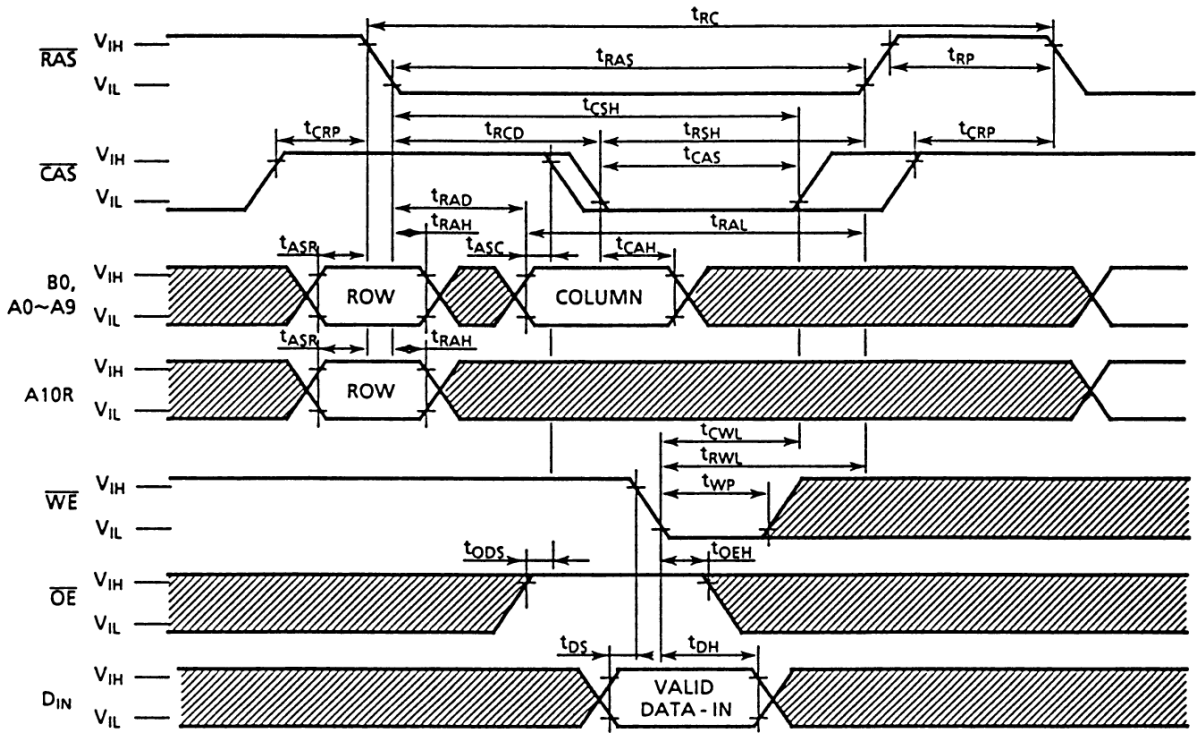
Read Cycle



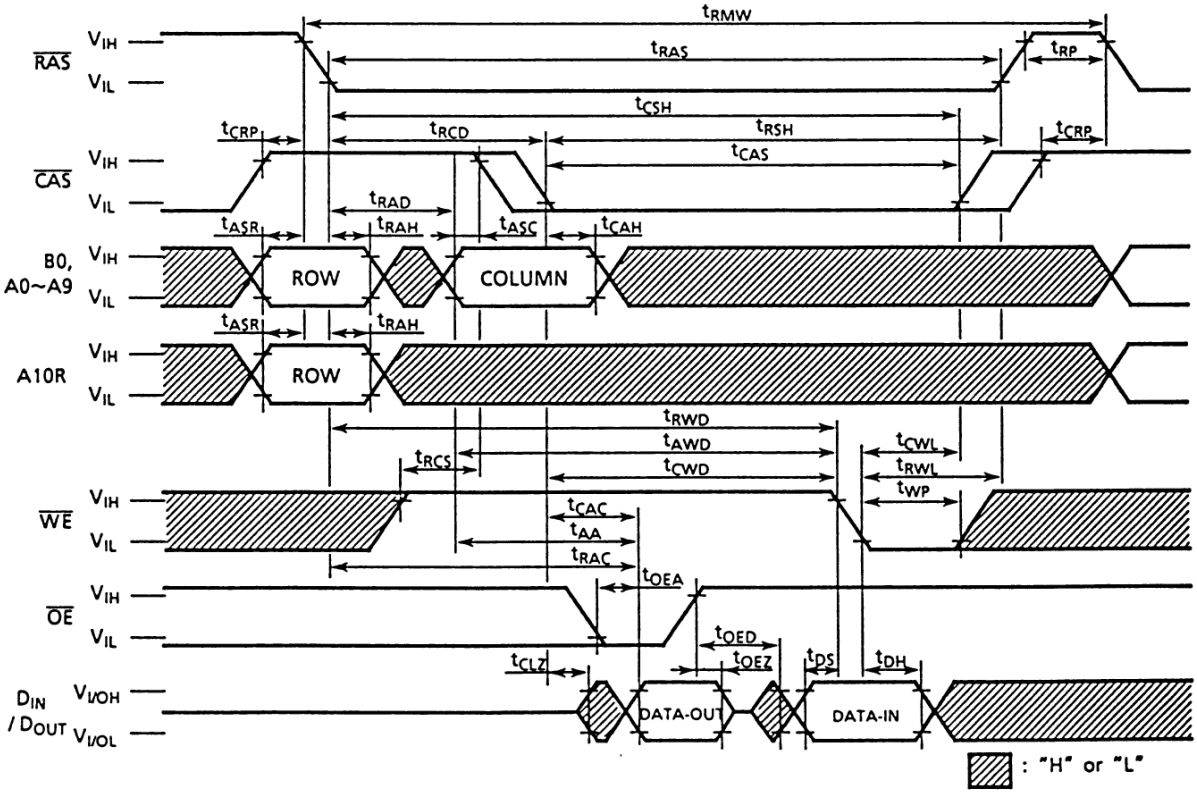
Write Cycle (Early Write)



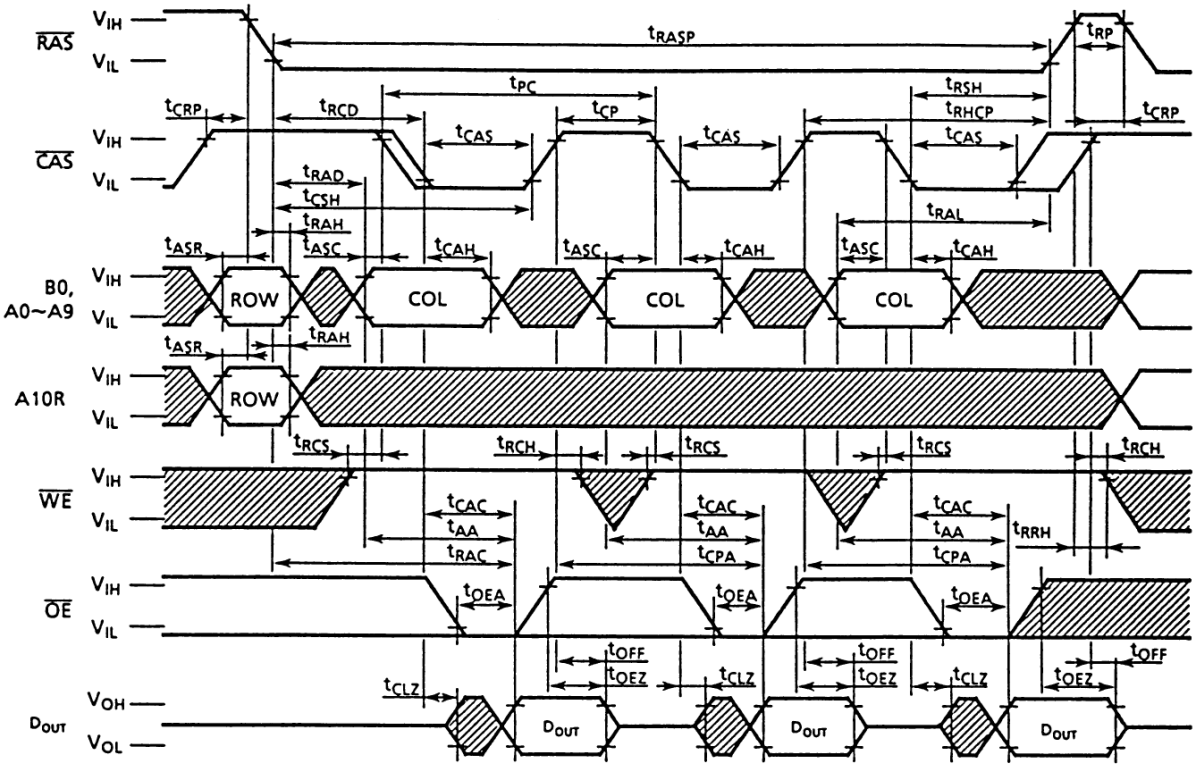
Write Cycle ($\overline{OE}$ Controlled Write)



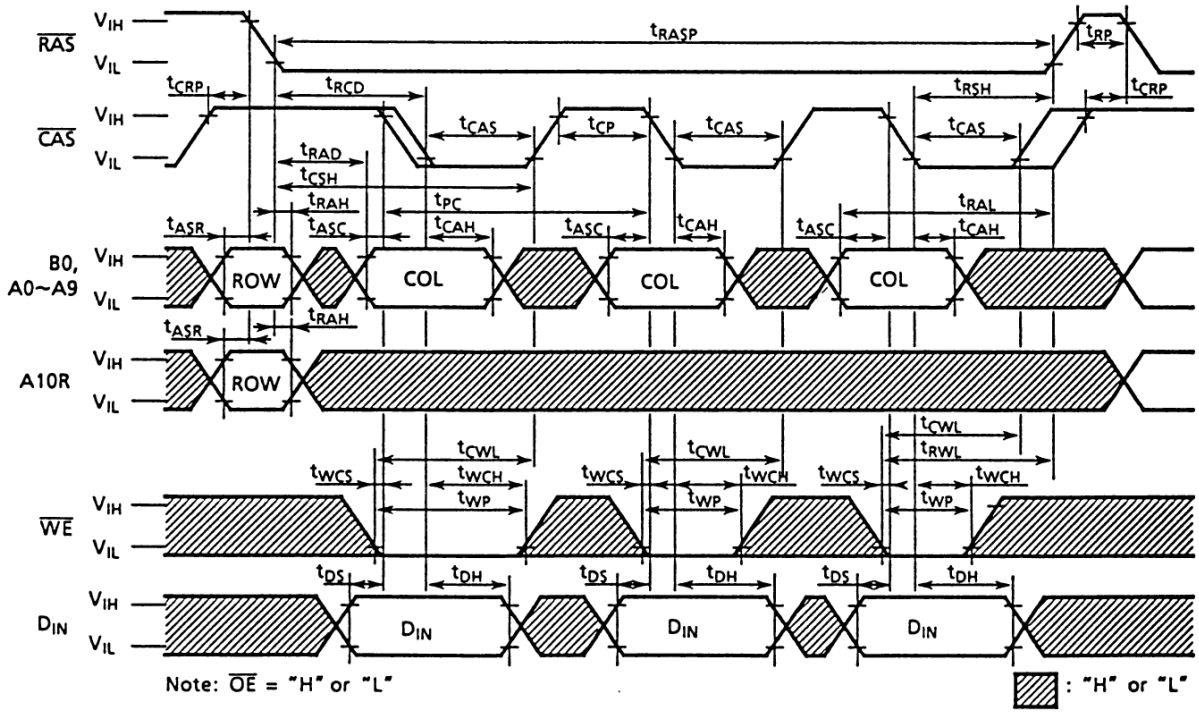
Read-Modify-Write Cycle



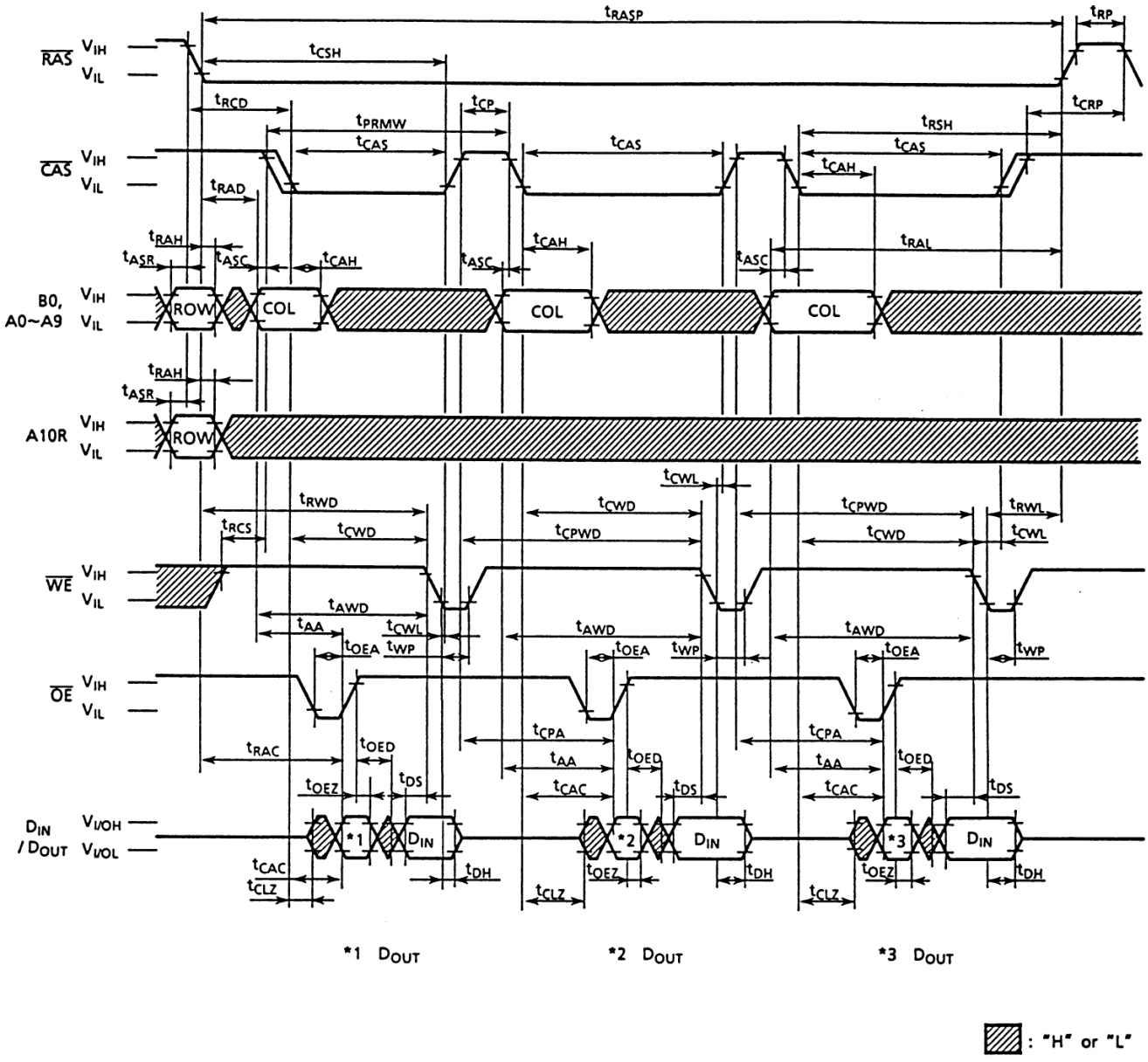
Fast Page Mode Read Cycle



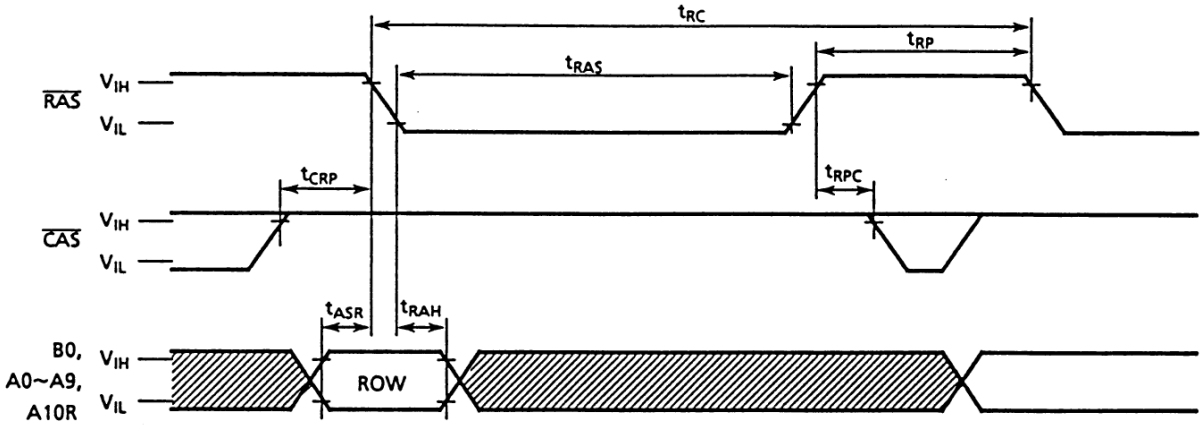
Fast Page Mode Write Cycle (Early Write)



Fast Page Mode Read-Modify-Write Cycle



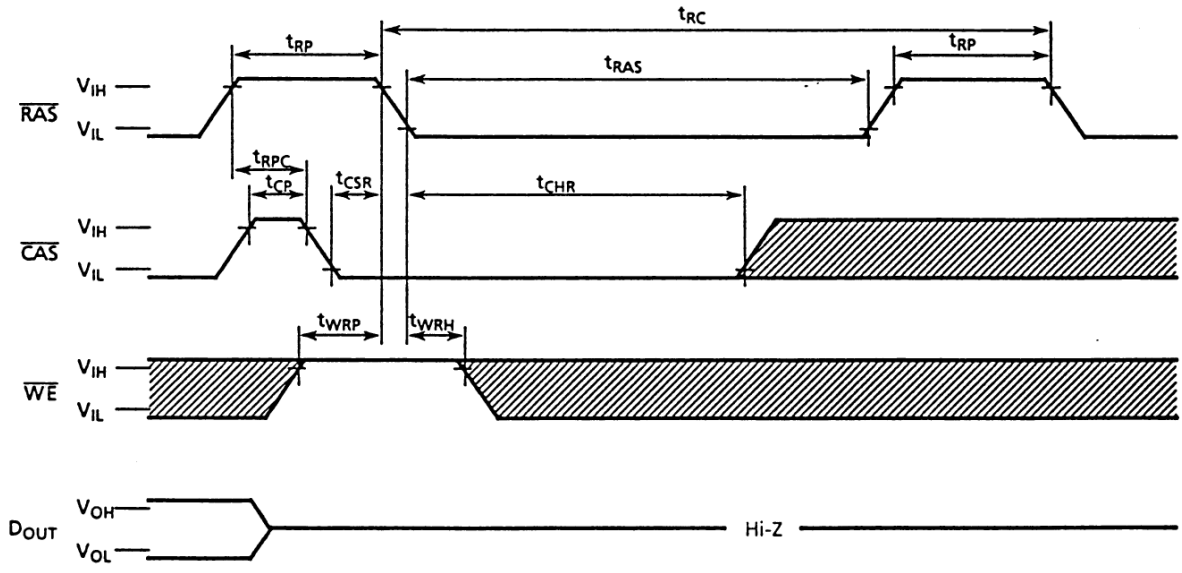
$\overline{RAS}$ Only Refresh Cycle



Note: D_{IN}, $\overline{WE}$, $\overline{OE}$ = "H" or "L"

: "H" or "L"

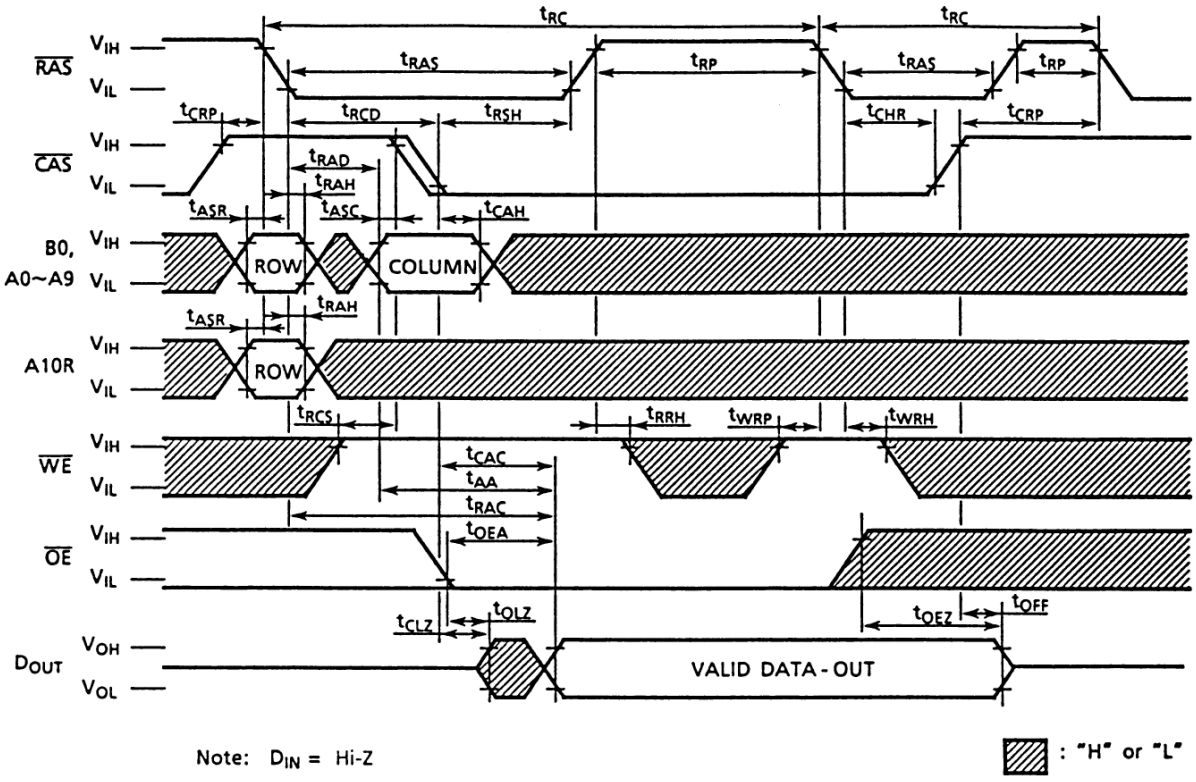
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



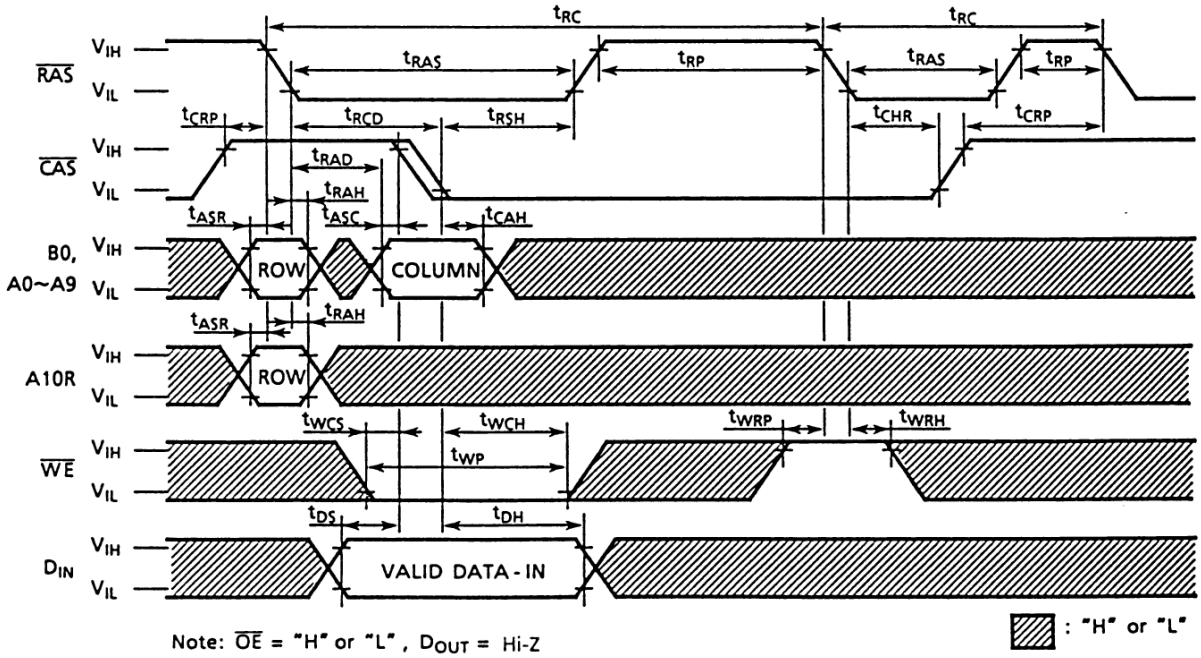
Note: D_{IN}, $\overline{OE}$, B0, A0~A9, A10R = "H" or "L"

: "H" or "L"

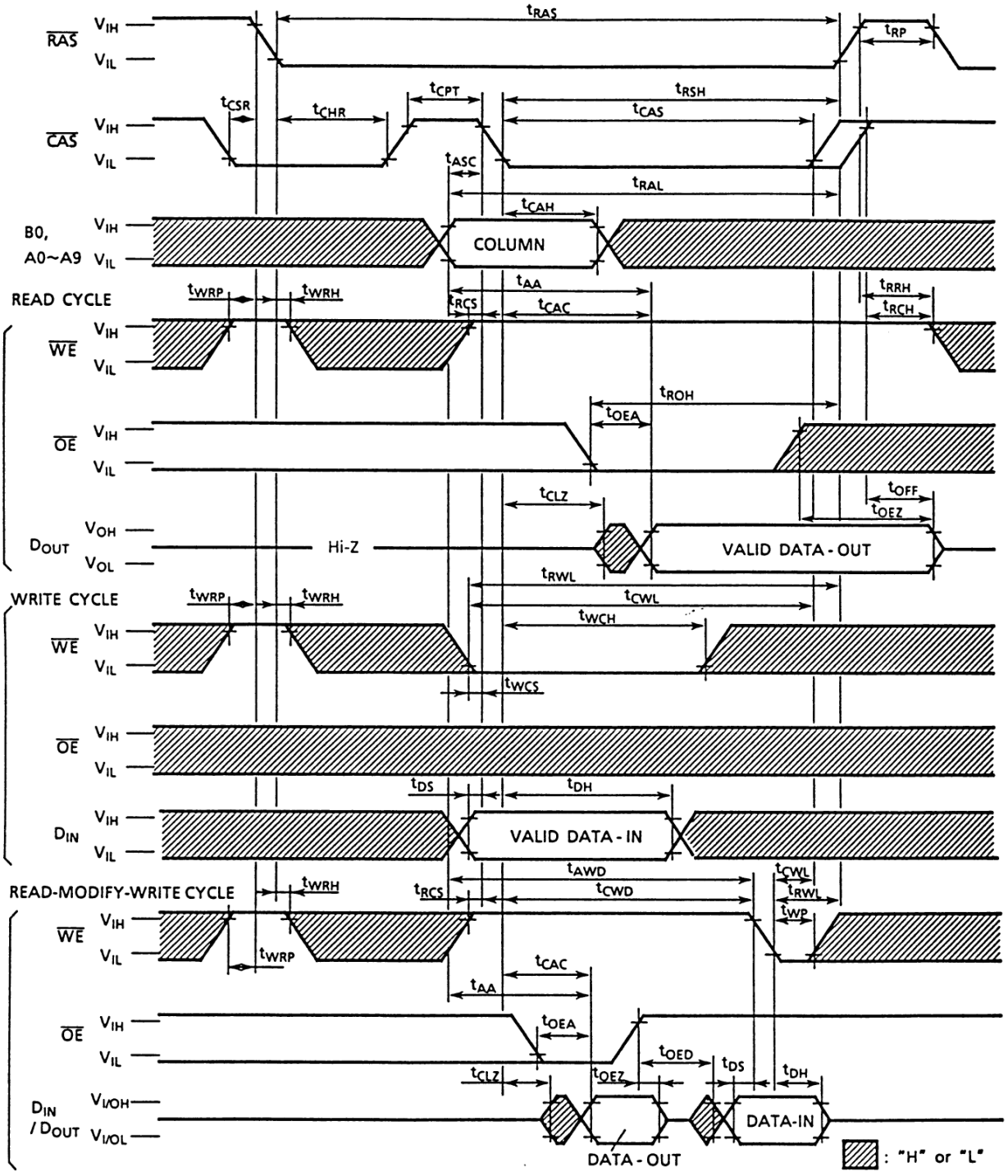
Hidden Refresh Cycle (Read)



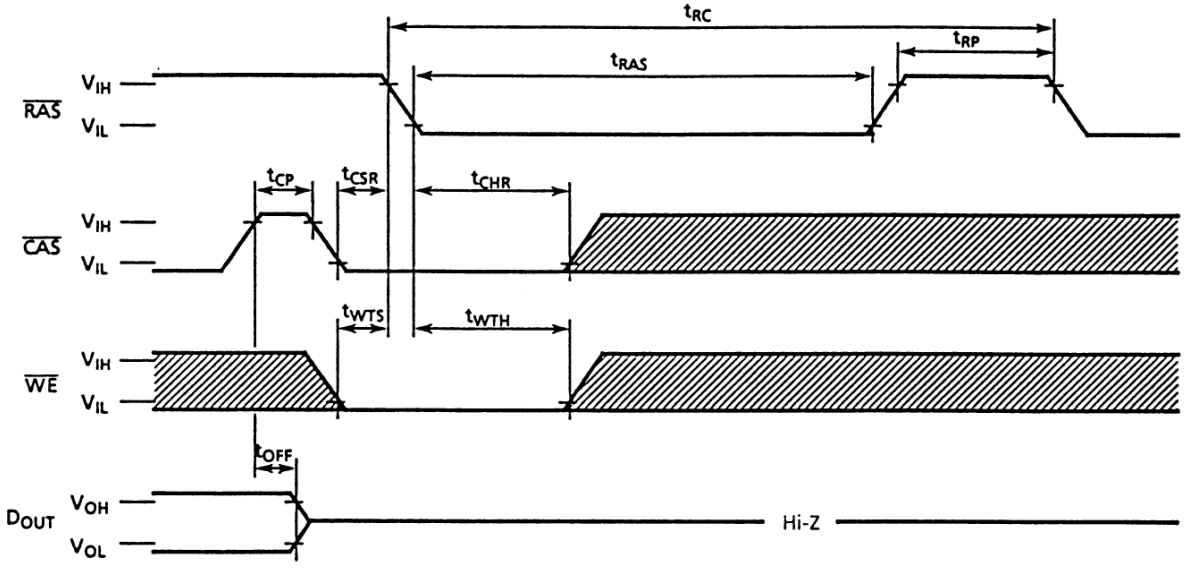
Hidden Refresh Cycle (Write)



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle



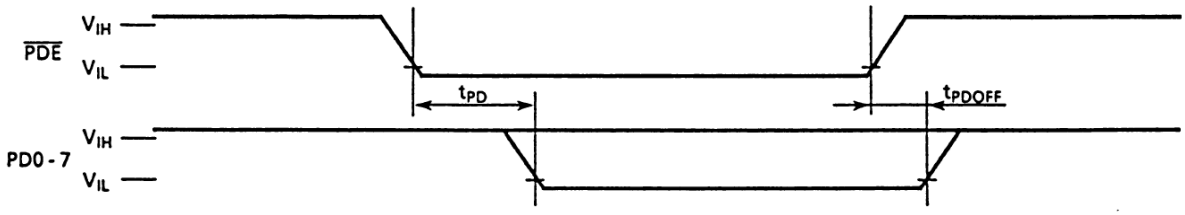
$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: D_{IN}, $\overline{OE}$, B0, A0~A9, A10R = "H" or "L"

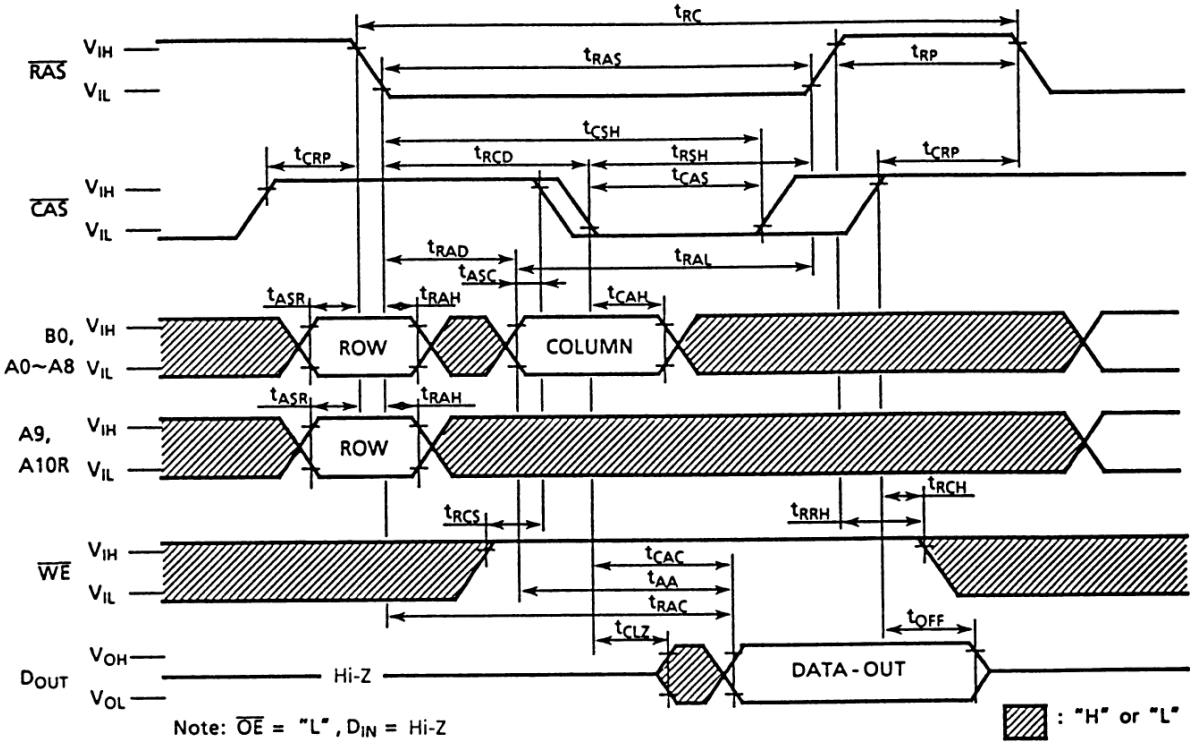
▨ : "H" or "L"

Presence Detect Data Read Cycle

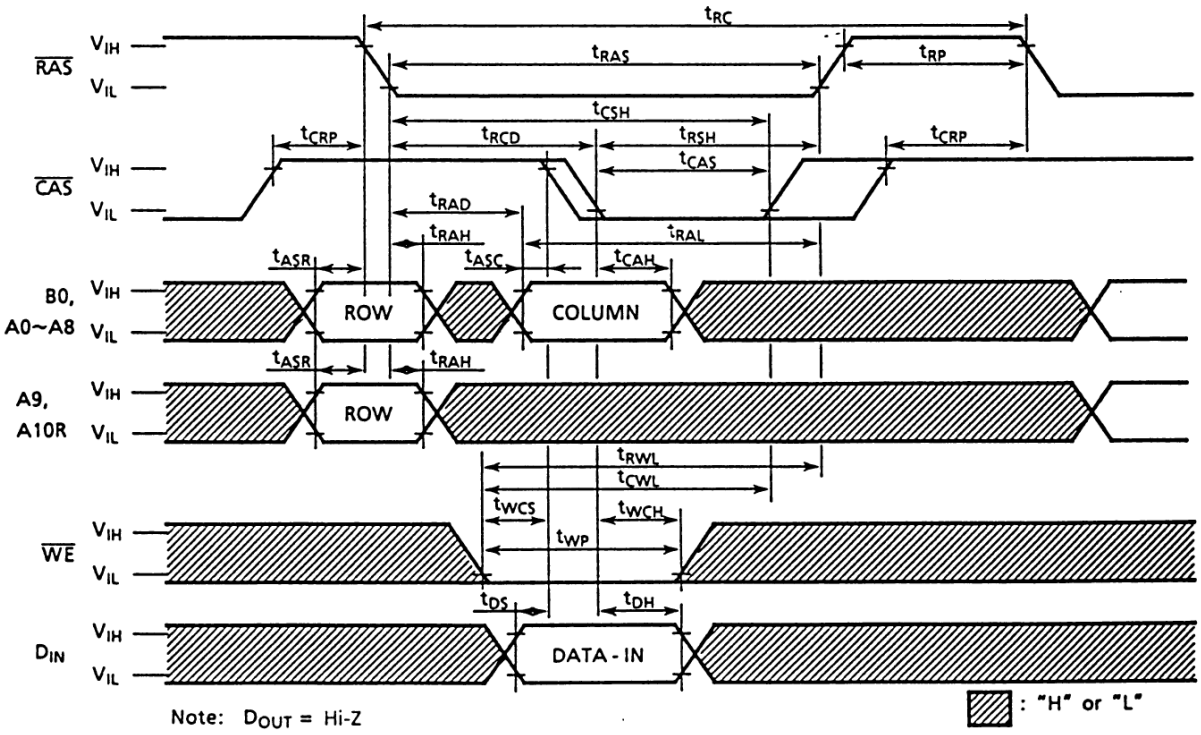


Note: t_{PDOFF} is measured with PD pin pulled V_{CC} .

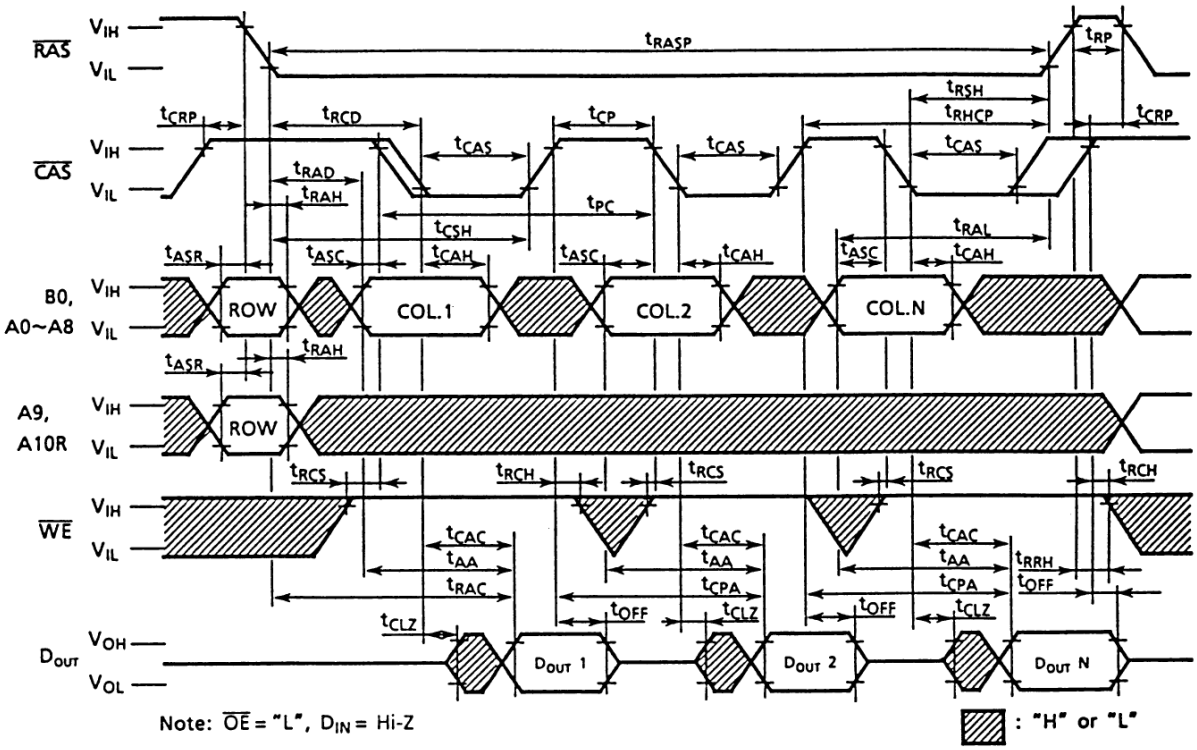
Read Cycle in the Test Mode



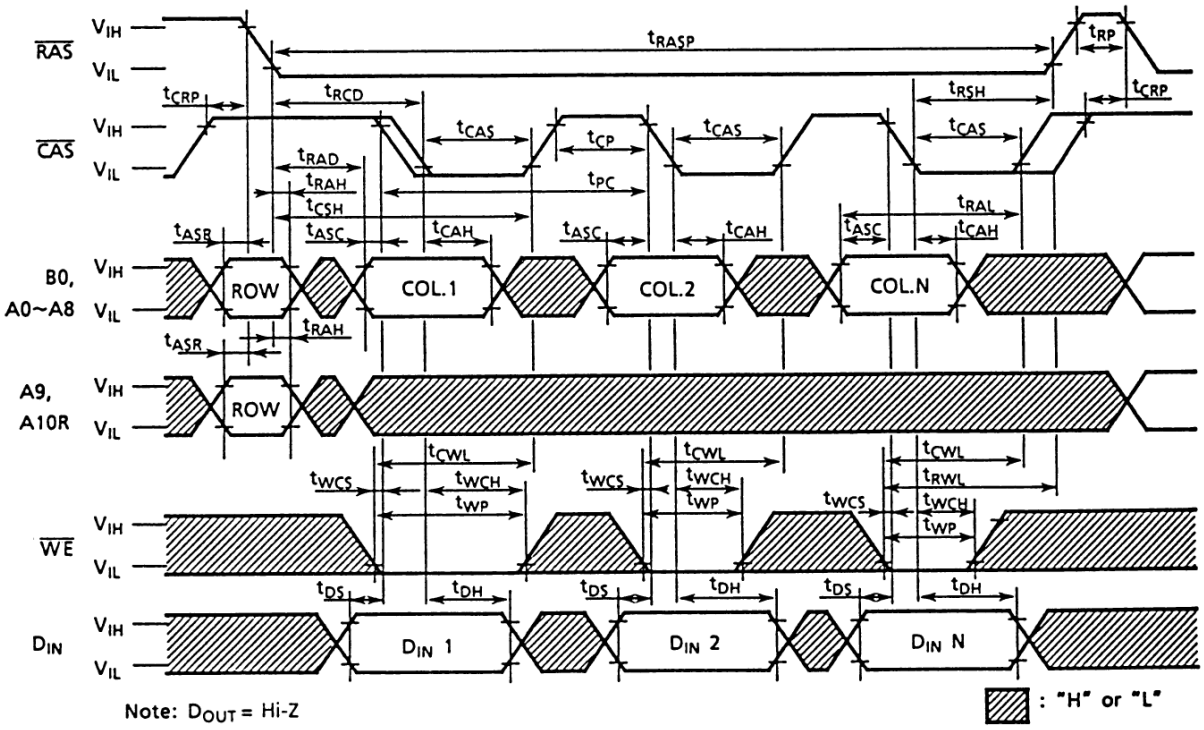
Write Cycle (Early Write) in the Test Mode



Fast Page Mode Read Cycle in the Test Mode



Fast Page Mode Write Cycle in the Test Mode

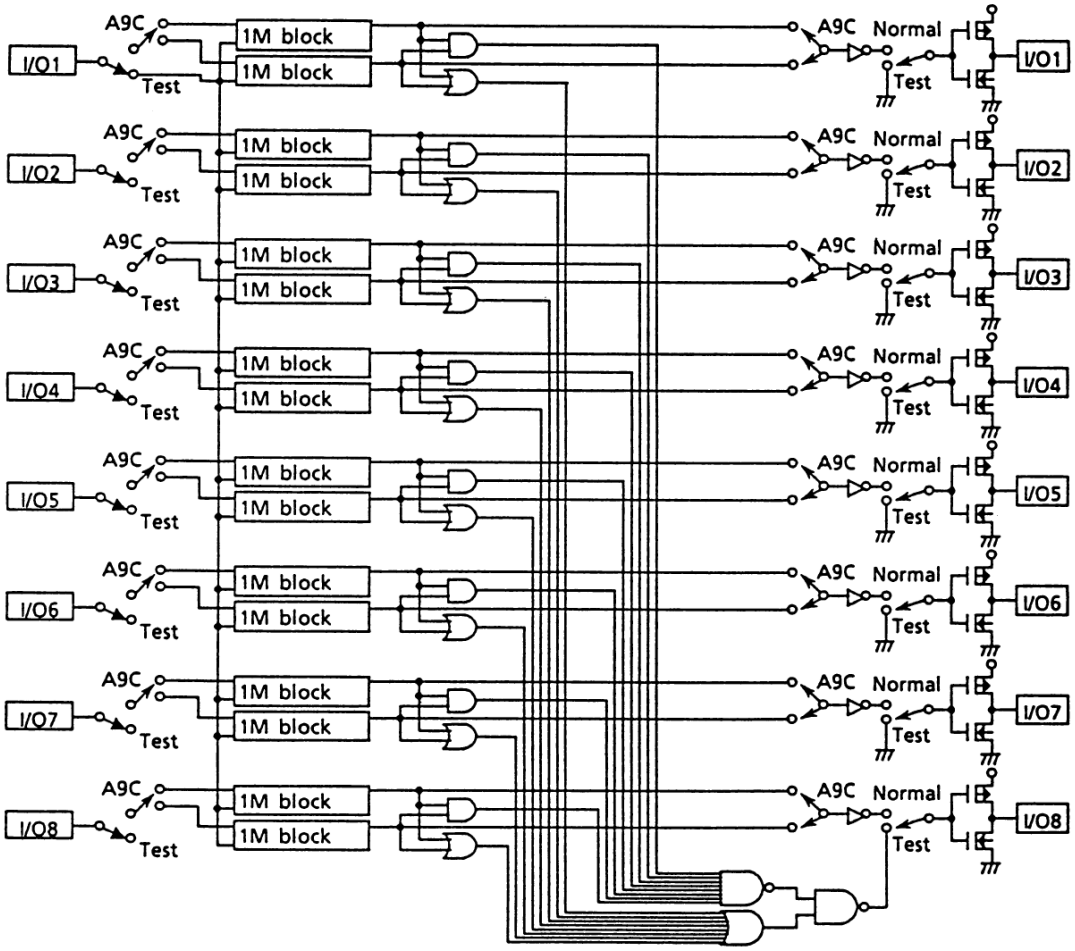


Test Mode

The TC51V17800ANJ/ANT is the RAM organized as 2,097,152 words by 8 bits, it is internally organized as 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel by using only I/O1. A9C is not used. If, upon reading, 16 bits are equal (all "1"'s or "0"'s), the I/O8 pin indicates a "1". If they were not equal, the I/O8 pin would indicate a "0". Other I/O pins (I/O1 ~ 7) always indicate a "1" a during test mode read cycle. Figure 1 shows the block diagram of TC51V17800ANJ/ANT. In "Test Mode", the 2Mx8 DRAM can be tested as if it were a 1Mx16 DRAM.

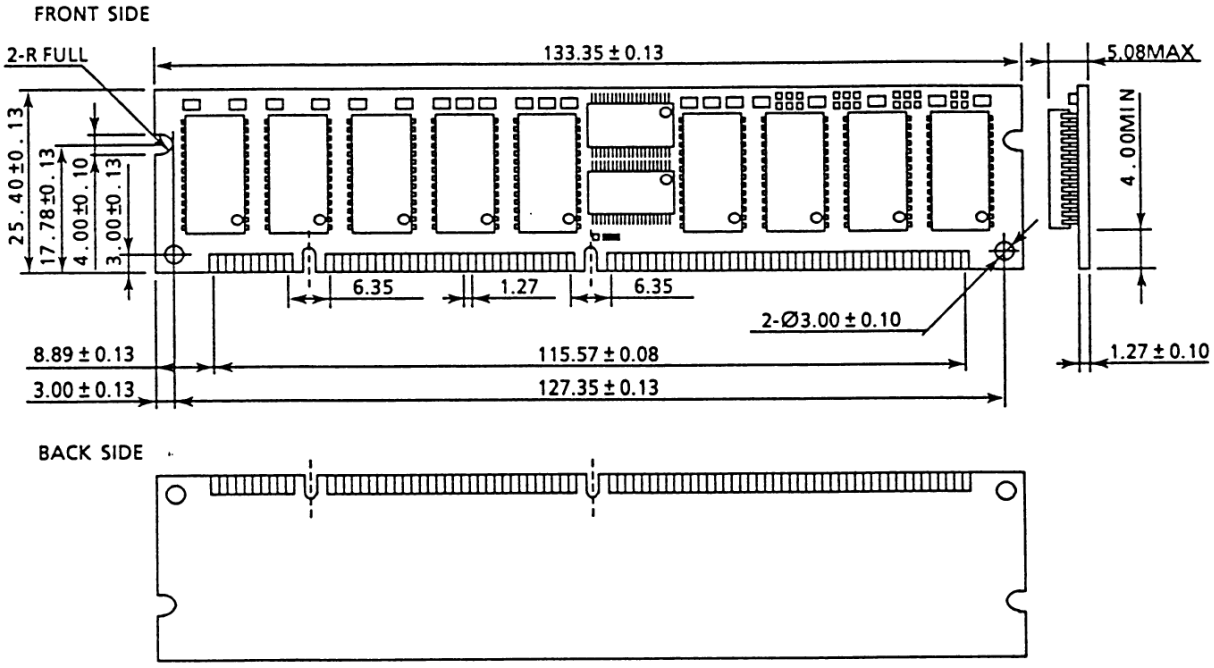
"$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" puts the device into "Test Mode", and "$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

Block Diagram in the Test Mode

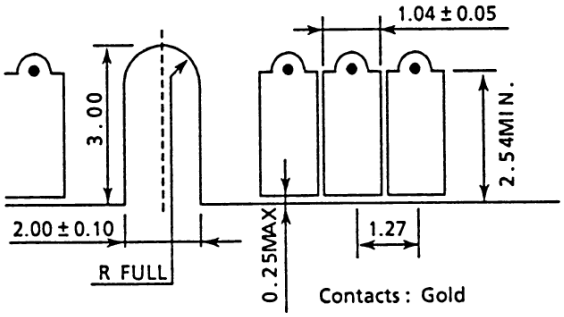


Outline Drawing

THM72V2010AG **Unit in mm**

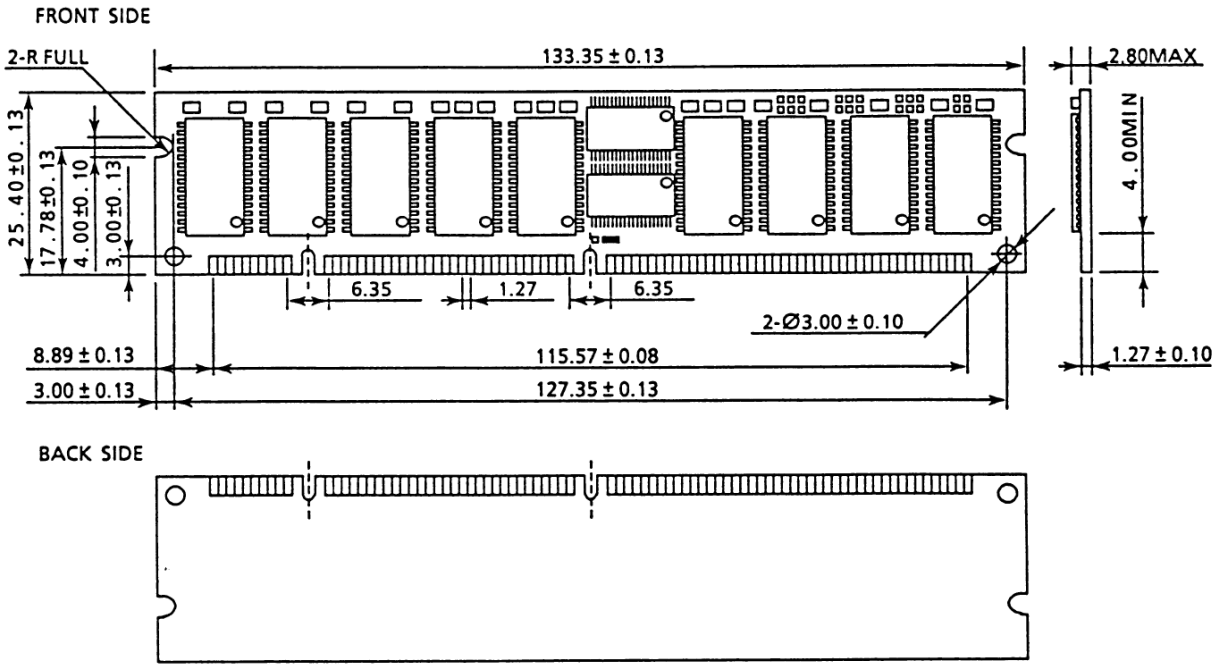


DETAIL OF CONTACTS

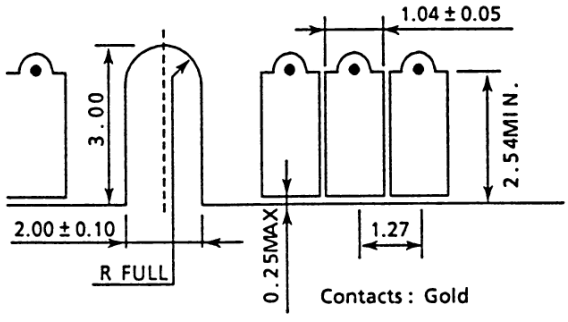


Outline Drawing

THM72V2010ATG **Unit in mm**



DETAIL OF CONTACTS



Weight : 14.6g (Typ.)