NEC

NEC Electronics Inc.

μPD7533/75CG33E
4-Bit, Single-Chip
CMOS Microcomputers
With A/D Converter

Description

The μPD7533 is a 4-bit, single-chip CMOS micro-computer with a 4-channel, 8-bit A/D converter, 8-bit timer/event counter, and an 8-bit serial interface. The μPD7533 has 30 I/O lines, 8 of which can be used to directly drive LEDs. The μPD7533 executes 67 instructions of the μPD7500 series "A" instruction set.

The A/D converter has various temperature monitoring applications that can be used with household electrical appliances, such as air conditioners and electric ovens. Other applications include health monitoring equipment and cameras.

The μPD75CG33E consists of a 28-pin socket "piggy-backed" on the lower 42-pin ceramic DIP. This socket is configured to hold either a 2732A or 2764 EPROM. For engineering purposes, programs can be tried and debugged before ROM code submission.
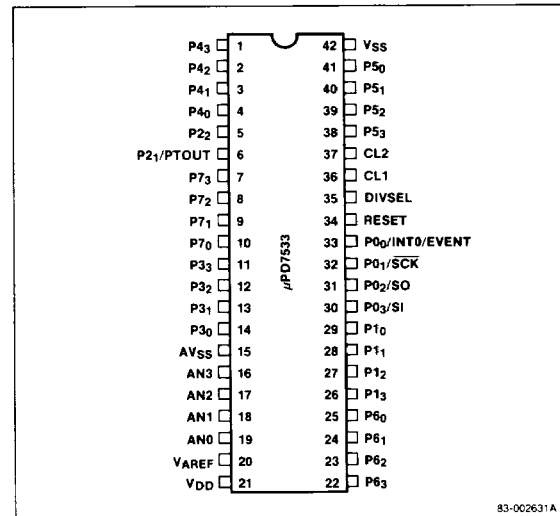
Features

□ 4-bit single chip microcomputer
□ 67 instructions (subset of μPD7500 series set A)
□ Instruction cycle
  — 5 μs at 5 V, 400-kHz clock at ceramic oscillation, DIVSEL = high
  — 10 μs at 5 V, 400-kHz clock at ceramic oscillation, DIVSEL = low
□ Program memory (ROM): 4096 words x 8 bits
  — External in the μPD75CG33E
□ Data memory (RAM): 160 words x 4 bits
□ 8 high current output lines for LED direct drive
□ Input/output ports
  — Two 4-bit input ports
  — One 2-bit output port
  — One 4-bit output port
  — Three 4-bit input/output ports (two of these can function in 8-bit units)
  — One 4-bit input/output port usable at bit level
□ Interrupts: two internal and one external
□ 8-bit serial interface
□ Standby operation
  — STOP mode
  — HALT mode
□ On-chip system clock oscillator
  — Ceramic resonator
  — Full or 1/2 oscillation frequency
□ CMOS technology
□ Low power consumption
□ Single power supply

Ordering Information

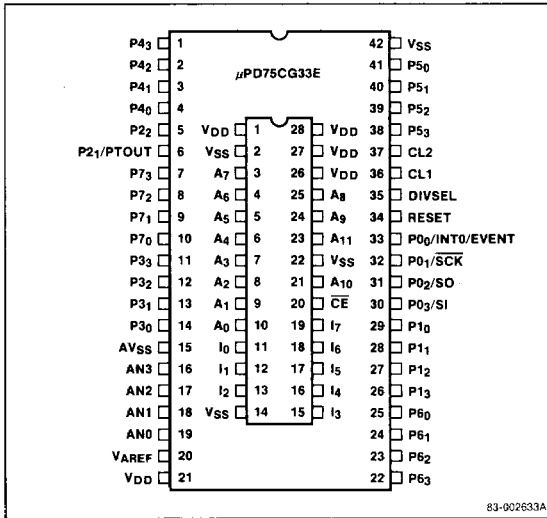| Part Number	Package Type	Maximum Frequency of Operation
μPD7533C	42-pin plastic DIP	510 kHz
μPD7533CU	42-pin plastic shrink DIP	510 kHz
μPD7533G-22	44-pin plastic QFP	510 kHz
μPD75CG33E	42-pin ceramic piggyback DIP	510 kHz

Pin Configurations

42-Pin Plastic DIP or Plastic Shrink DIP

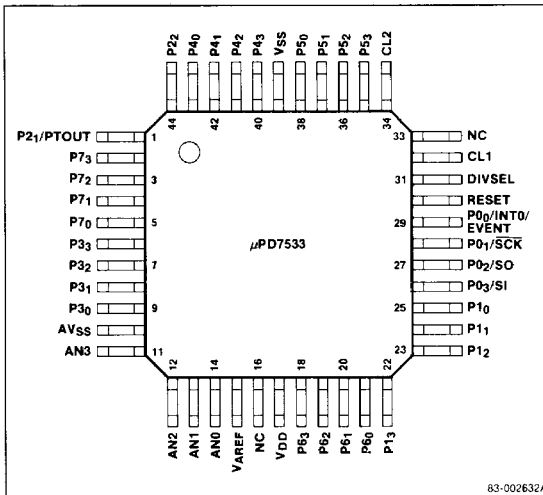| Pin		Pin
P4₃	1	42 Vss
P4₂	2	41 P5₀
P4₁	3	40 P5₁
P4₀	4	39 P5₂
P2₂	5	38 P5₃
P2₁/PTOUT	6	37 CL2
P7₃	7	36 CL1
P7₂	8	35 DIVSEL
P7₁	9	34 RESET
P7₀	10	33 P0₀/INT0/EVENT
P3₃	11	32 P0₁/SCK
P3₂	12	31 P0₂/SO
P3₁	13	30 P0₃/SI
P3₀	14	29 P1₀
AVss	15	28 P1₁
AN3	16	27 P1₂
AN2	17	26 P1₃
AN1	18	25 P6₀
AN0	19	24 P6₁
VAREF	20	23 P6₂
VDD	21	22 P6₃

83-002631A

Pin Configurations (cont)

42-Pin Ceramic Piggyback DIP

83-002633A

44-Pin Plastic QFP

83-002632A

Pin Identification

42-Pin DIP, Shrink DIP, and Piggyback DIP

No.	Symbol	Function
1-4	$P4_3$-$P4_0$	I/O port 4
5, 6	$P2_2$, $P2_1$/PTOUT	Port 2 output
7-10	$P7_3$-$P7_0$	I/O port 7
11-14	$P3_3$-$P3_0$	Port 3 output
15	A_{VSS}	A/D converter ground
16-19	AN3-AN0	Analog input
20	V_{AREF}	A/D reference voltage input
21	V_{DD}	Positive power supply
22-25	$P6_3$-$P6_0$	I/O port 6
26-29	$P1_3$-$P1_0$	Port 1 input
30	$P0_3$/SI	Port 0 input/Serial input
31	$P0_2$/SO	Port 0 input/Serial output
32	$P0_1$/$\overline{SCK}$	Port 0 input/(I/O) Serial clock
33	$P0_0$/INT0/EVENT	Port 0 input/Interrupt 0/Event input
34	RESET	RESET input
35	DIVSEL	System clock selection input
36, 37	CL1, CL2	External clock input/System clock terminal
38-41	$P5_3$-$P5_0$	I/O port 5
42	V_{SS}	Ground

Pin Identification (cont)

44-Pin QFP

No.	Symbol	Function
1, 44	P2$_1$/PTOUT, P2$_2$	Port 2 output
2-5	P7$_3$-P7$_0$	I/O port 7
6-9	P3$_3$-P3$_0$	Port 3 output
10	A$_{VSS}$	A/D converter ground
11-14	AN3-AN0	Analog input
15	V$_{AREF}$	A/D reference voltage input
17	V$_{DD}$	Positive power supply
18-21	P6$_3$-P6$_0$	I/O port 6
22-25	P1$_3$-P1$_0$	Port 1 input
26	P0$_3$/SI	Port 0 input/Serial input
27	P0$_2$/SO	Port 0 input/Serial output
28	P0$_1$/$\overline{SCK}$	Port 0 input/(I/O) Serial clock
29	P0$_0$/INT0/EVENT	Port 0 input/Interrupt 0/Event input
30	RESET	RESET input
31	DIVSEL	System clock selection input
32, 34	CL1, CL2	External clock input/System clock
35-38	P5$_3$-P5$_0$	I/O port 5
39	V$_{SS}$	Ground
40-43	P4$_3$-P4$_0$	I/O port 4
16, 33	NC	No connect

28-Pin EPROM Socket on 42-pin Piggyback DIP

No.	Symbol	Function
1, 26-28	V$_{DD}$	Positive power supply
2, 14, 22	V$_{SS}$	Ground
20	$\overline{CE}$	Chip enable output
3-10, 21, 23-25	A$_0$-A$_{11}$	Address bus
11-13, 15-19	I$_0$-I$_7$	Data bus

Pin Functions

P0$_0$-P0$_3$ [Port 0]

P0$_0$-P0$_3$ function as port 0. P0$_0$ also functions as a count pulse input pin for the timer/event counter (EVENT) or as interrupt 0 (INT0). P0$_1$ also functions as a serial clock input/output pin ($\overline{SCK}$) for the serial interface. P0$_2$ functions as a serial data output pin (SO) and pins P0$_3$ as a serial data input pin (SI). The P0$_1$/$\overline{SCK}$ and P0$_2$/SO pins are three-state input/output.

The shift mode register (SM$_0$-SM$_3$) determines the operation mode of the port 0 input/output pins; however, the data on P0$_0$-P0$_3$ can be loaded into the accumulator at any time by executing a port input instruction (IP/IPL). This is possible even when P0$_1$-P0$_3$ are functioning as the serial interface.

After a RESET, P0$_0$-P0$_3$ become input ports (high impedance).

P1$_0$-P1$_3$ [Port 1]

P1$_0$-P1$_3$ function as port 1. Execution of an IP or IPL instruction reads data present on P1$_0$-P1$_3$ into the accumulator. Tie any unused lines of P1$_0$-P1$_3$ to V$_{DD}$ or V$_{SS}$.

P2$_1$-P2$_2$ [Port 2]

P2$_1$-P2$_2$ function as port 2 with an output latch. When an output instruction (OP/OPL) to port 2 is executed, the middle 2 bits (A$_1$ and A$_2$) of the accumulator are latched by the output latch and, at the same time, output to P2$_1$-P2$_2$.

After being written once, the output latch contents remain until they are rewritten by an output instruction or a reset. The status of the corresponding output signal also remains. After a reset, the output latch contents become undefined, all output signals are disabled, and the output drivers are turned off.

P2$_1$ is also used as an output pin (PTOUT) for the timer-out F/F signal (PTOUT). Bit 3 (CM$_3$) of the clock mode register controls the PTOUT output. When CM$_3$ is 1, TOUT is ORed with the P2$_1$ output latch contents and sent to the output driver. Therefore, to output the P2$_1$ output latch contents, reset CM$_3$ to 0 to inhibit the TOUT signal.

Note that soon after the RESET signal is asserted, CM$_3$ is reset and TOUT is inhibited. However, since the output latch contents are undefined after a reset, to output the TOUT signal, first write 0 in the P2$_1$ output latch and then set CM$_3$ to 1 to output TOUT.

P3₀-P3₃ [Port 3]

P3₀-P3₃ function as port 3 with an output latch. When an output instruction to port 3 is executed, the accumulator contents are latched and output.

Once data is written in the output latch, the data is held until the next output instruction to port 3 is executed or RESET is asserted. After a reset, the output latch contents become undefined and the output driver is turned off.

P4₀-P4₃ [Port 4]
P5₀-P5₃ [Port 5]

P4₀-P4₃ function as port 4 and P5₀-P5₃ function as port 5. When an input instruction is executed, the data on these pins is read into the accumulator. When an output instruction is executed, the accumulator contents are latched and output. After the data is written into the latch, it is held until the next output instruction to ports 4 or 5 is executed, or RESET is asserted.

Ports 4 and 5 can work as a pair enabling data (input with the IP54 instruction and output with the OP54 instruction) in 8-bit units. The high four bits of data are from the accumulator and the low four bits are from memory (addressed by HL).

Ports 4 and 5 automatically set in the input mode (high impedance output) after a reset or when the input instructions to these ports are executed. After a reset, the output latch contents become undefined. Both ports 4 and 5 can drive LEDs directly.

Note that after the port changes from output mode to input mode, the data on the line is unstable when the input instruction that changes the mode is first executed. It is strongly recommended that you re-execute the input instruction considering the input/output mode switching time. This will insure reading stable data.

The bit manipulation instruction affects the specified bit only. So when the output latch contents are undefined, (immediately after a reset), initialize the output latch contents with an output instruction before the bit manipulation instruction is executed.

P6₀-P6₃ [Port 6]

P6₀-P6₃ function as the 4-bit input latched, three-state output port. The individual lines can be programmed as either inputs or outputs.
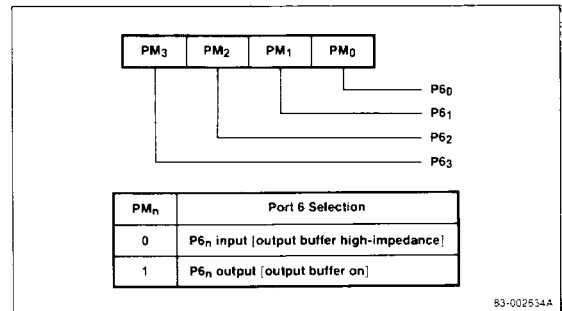
In input mode, data present at this port is read into the accumulator by the execution of an IP or IPL instruction. Accumulator data written to this port by the execution of an OP, OPL, ANP, or ORP instruction is statically latched, and remains unchanged until re-written. This data, however, is not output since the output buffer is disabled and placed in the high impedance state.

In output mode, accumulator data written to the specified port line by the execution of the OP, OPL, ANP, or ORP instruction is statically latched and output to the P6ₙ pin. Data present at P6ₙ is read into the accumulator by the execution of the IP or IPL instruction, making it possible to read the contents of the P6ₙ output latch.

All lines of port 6 are initialized to the high impedance state at Reset. Leave any unused lines open (if outputs) or tied to V_{DD} or V_{SS} (if inputs).

The port 6 mode select register (MSR) controls the function of the individual port 6 lines. The execution of the OP or OPL instruction loads the port 6 MSR with the accumulator contents. The 4-bit immediate data operand or the contents of the L register must be set to 0EH. Figure 1 shows the format of the port 6 MSR.

Figure 1.   Port 6 MSR Format

PM₃	PM₂	PM₁	PM₀

P6₀
P6₁
P6₂
P6₃

PMₙ	Port 6 Selection
0	P6ₙ input (output buffer high-impedance)
1	P6ₙ output (output buffer on)

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P7$_0$-P7$_3$ [Port 7]

Port 7 is a 4-bit input or latched three-state output port. The execution of an IP or IPL instruction execution reads data present at this port into the accumulator. Accumulator data written to this port by the execution of an OP, OPL, ANP, or ORP instruction is statically latched and remains unchanged until rewritten.

Upon reset, all lines are initialized to the high-impedance state. Leave any unused lines open (if outputs) or tied to V$_{DD}$ or V$_{SS}$ (if inputs).

AN0-AN3 [A/D Input Terminal]

AN0-AN3 are the 4-channel A/D converter input terminals. The A/D converter uses a successive approximation method.

V$_{AREF}$ [A/D Converter Positive Reference]

The voltage on V$_{AREF}$ determines the full scale analog voltage.

A$_{VSS}$ [A/D Converter Ground]

A$_{VSS}$ is the ground for the A/D circuit.

CL1, CL2 [Clock]

CL1 and CL2 connect external oscillator elements to the system clock. Connect a ceramic resonator to these pins. If an external clock is used, place a buffer between the clock source and the CL1 and CL2 pins.

When connecting the oscillation parts to the CL1 and CL2 pins, use the shortest wiring possible. Ground the capacitor as close to the V$_{SS}$ pin as possible.

DIVSEL [System Clock Divider Selection Input]

DIVSEL selects whether the system clock runs at ceramic oscillation frequency, or at one-half the ceramic oscillation frequency. If a logic 0 (V$_{SS}$) is connected to DIVSEL, the system clock is one-fourth the ceramic oscillation. If DIVSEL is high, then the system clock will be one-half of the ceramic oscillation.

RESET [Reset]

A high on RESET activates this input.

V$_{DD}$ [Power Supply]

V$_{DD}$ is the positive power supply pin.

V$_{SS}$ [Ground]

V$_{SS}$ is the ground pin.

Pin Functions, *µ*PD75CG33 EPROM

A$_0$-A$_{11}$ [EPROM Address]

A$_0$-A$_{11}$ output the contents of the EPROM program address counter. A reset leaves A$_0$-A$_{11}$ undefined.

I$_0$-I$_7$ [Data Bus]

I$_0$-I$_7$ input the contents of the EPROM data bus.
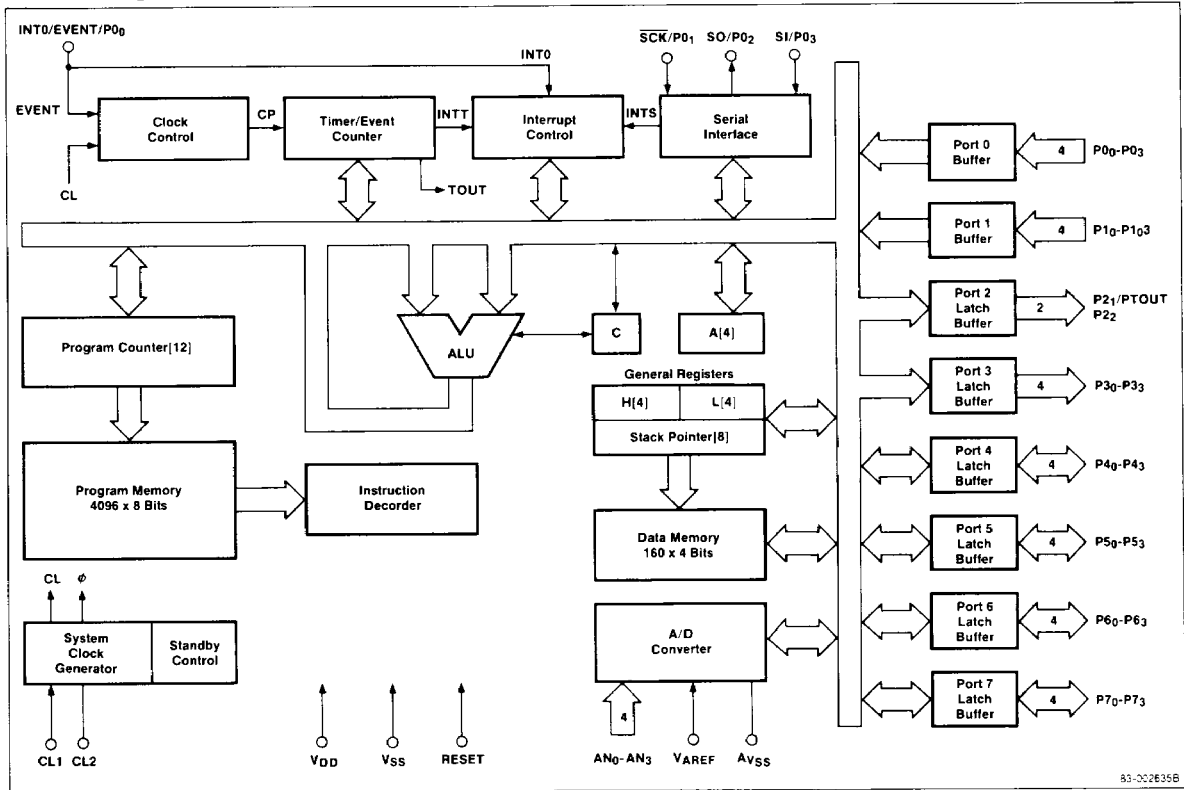
$\overline{CE}$ [Chip Enable]

$\overline{CE}$ outputs the EPROM chip enable signal. (Active low.)

V$_{DD}$ [Power Supply], V$_{SS}$ [Ground]

V$_{DD}$ is the positive power supply pin with the same voltage as the lower portion pin 21. V$_{SS}$ is the ground pin with the same voltage as the lower portion pin 42. The following voltages are supplied to the 2764 or 2732A pins from V$_{DD}$ or V$_{SS}$.

Pin Number		Symbol	Voltage
2764	2732A		
1	20	V$_{PP}$	V$_{DD}$ pin 21 = +5 V
28	24	V$_{CC}$	V$_{DD}$ pin 21 = +5 V
22	20	$\overline{OE}$	V$_{SS}$ pin 42 = 0 V
2	—	A$_{12}$	V$_{DD}$ pin 21 = +5 V
14	12	V$_{SS}$	V$_{SS}$ pin 42 = 0 V

Block Diagram

INT0/EVENT/P0₀

$\overline{SCK}$/P0₁ SO/P0₂ SI/P0₃

INT0

EVENT

Clock Control — CP — Timer/Event Counter — INTT — Interrupt Control — INTS — Serial Interface

CL — TOUT

Port 0 Buffer — 4 — P0₀-P0₃

Port 1 Buffer — 4 — P1₀-P1₀₃

Program Counter[12]

ALU — C — A[4]

Port 2 Latch Buffer — 2 — P2₁/PTOUT P2₂

General Registers
H[4] L[4]
Stack Pointer[8]

Port 3 Latch Buffer — 4 — P3₀-P3₃

Program Memory 4096 x 8 Bits — Instruction Decorder

Port 4 Latch Buffer — 4 — P4₀-P4₃

Data Memory 160 x 4 Bits

Port 5 Latch Buffer — 4 — P5₀-P5₃

CL φ

System Clock Generator — Standby Control

A/D Converter

Port 6 Latch Buffer — 4 — P6₀-P6₃

Port 7 Latch Buffer — 4 — P7₀-P7₃

CL1 CL2

V_DD V_SS RESET

AN₀-AN₃ V_AREF A_VSS

83-002635B

Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{DD} + 0.3 V
Output voltage, V_O	−0.3 V to V_{DD} + 0.3 V
High level output current, I_{OH}	−17 mA (1 pin)
	−20 mA (all output ports)
Low level output current, I_{OL}	17 mA (1 pin)
	80 mA ports 2,3,4,7 (total pins)
	80 mA ports 0,5,6
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C
A/D V_{SS}, A_{VSS}	−0.3 to +0.3 V
A/D reference, V_{AREF}	−0.3 V to V_{DD}

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V

Parameter	Symbol	Limits		Unit	Test Conditions
		Min	Max		
Input capacitance	C_{IN}		15	pF	f =1 MHz Unmeasured pins are 0 V.
Output capacitance	C_{OUT}		15	pF	
I/O capacitance	C_{IO}		15	pF	

DC Characteristics

$T_A = -10$ to $+70°C$, $V_{DD} = 2.7$ to 6.0 V, DIVSEL = 1

Parameter	Symbol	Min	Max	Unit	Test Conditions
High level input voltage (other than CL1, CL2)	V_{IH1}	$0.7\ V_{DD}$	V_{DD}	V	Conditions specified by oscillation characteristics
High level input voltage (CL1, CL2)	V_{IH2}	$V_{DD} - 0.5$	V_{DD}	V	
Low level input voltage (other than CL1, CL2)	V_{IL1}	0	$0.3\ V_{DD}$	V	
Low level input voltage (CL1, CL2)	V_{IL2}	0	0.5	V	
High level output voltage	V_{OH}	$V_{DD} - 1.0$		V	$V_{DD} = 4.5-6.0$ V $I_{OH} = -1$ mA except P63
		$V_{DD} - 0.5$		V	$I_{OH} = -100\ \mu A$
		$V_{DD} - 0.5$	$V_{DD} - 0.2$	V	$V_{DD} = 4.5-6.0$ V $I_{OH} = -2$ mA (P63 only)
Low level output voltage	V_{OL}	0.6 (typ)	2.0	V	$V_{DD} = 4.5-6.0$ V $I_{OL} = 15$ mA
		0.7 (typ)	2.5	V	(75CG33: $V_{DD} = 4.5 - 6.0$ V)
			0.4	V	$I_{OL} = 1.6$ mA
			0.5	V	$I_{OL} = 400\ \mu A$
High level input leakage current (other than CL1, CL2)	I_{LIH1}		3	μA	$V_{IN} = V_{DD}$
High level input leakage current (CL1, CL2)	I_{LIH2}		20	μA	$V_{IN} = V_{DD}$
Low level input leakage current (other than CL1, CL2)	I_{LIL1}		-3	μA	$V_{IN} = 0$ V
Low level input leakage current (CL1, CL2)	I_{LIL2}		-20	μA	$V_{IN} = 0$ V
High level output leakage current	I_{LOH}		3	μA	$V_{OUT} = V_{DD}$
Low level output leakage current	I_{LOL}		-3	μA	$V_{OUT} = 0$ V

DC Characteristics

$T_A = -10$ to $+70°C$, $V_{DD} = 2.7$ to 6.0 V, DIVSEL = 1

Parameter	Symbol	Min	Max	Unit	Test Conditions
Supply current	I_{DD1}	1.0 (typ)	3.0	mA	Operating mode: $f_{CC} = 500$ kHz
	I_{DD2}	250 (typ)	750	μA	HALT mode: $f_{CC} = 500$ kHz
		300 (typ)	900	μA	(75CG33: $V_{DD} = 4.5 - 6.0$ V; $f_{CC} = 500$ kHz)
	I_{DD3}	0.1 (typ)	10	μA	STOP mode
		25 (typ)	200	μA	(75CG33: $V_{DD} = 4.5 - 6.0$ V)

AC Characteristics

$T_A = -10$ to $+70°C$, $V_{DD} = 2.7$ to 6.0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Cycle time	t_{CY}	3.92	200	μs	$V_{DD} = 4.5-6.0$ V
		9.52	200	μs	
EVENT input frequency	f_E	0	510	kHz	$V_{DD} = 4.5-6.0$ V
		0	210	kHz	
EVENT input high duration	t_{EH}	0.8		μs	$V_{DD} = 4.5-6.0$ V
EVENT input low duration	t_{EL}	2.2		μs	
SCK cycle time	t_{KCY}	4.0		μs	Input $V_{DD} = 4.5-6.0$ V
		3.92		μs	Output $V_{DD} = 4.5-6.0$ V
		10.0		μs	Input
		9.52		μs	Output
SCK high, low level duration	t_{KH}, t_{KL}	1.8		μs	Input $V_{DD} = 4.5-6.0$ V
		1.76		μs	Output $V_{DD} = 4.5-6.0$ V
		4.8		μs	Input
		4.6		μs	Output
SI setup time (SCK high)	t_{SIK}	300		ns	
SI hold time (SCK high)	t_{KSI}	450		ns	
SCK low to SO output delay time	t_{KSO}		850	ns	$V_{DD} = 4.5-6.0$ V
			1200		
INT0 high, low level duration	t_{I0H}, t_{I0L}	10		μs	
RESET high, low level duration	t_{RSH}, t_{RSL}	10		μs	

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Data Memory, STOP Mode Data Retention Characteristics

$T_A = -10$ to $+70°C$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Data retention supply voltage	V_{DDDR}	2.0		6.0	V	
Data retention supply current	I_{DDDR}		0.1	10	μA	$V_{DDDR} = 2.0$ V
RESET setup time	t_{SRS}	0			μs	
Oscillation stabilizing time	t_{OS}	20			ms	Ceramic resonator: when V_{DD} greater than 4.5 V

A/D Converter Characteristics

$T_A = -10$ to $+70°C$, $V_{DD} = +5.0$ V $\pm 5\%$,
$V_{SS} = A_{VSS} = 0$ V, $V_{AREF} = V_{DD} - 0.5$ V to V_{DD}

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Resolution			8		Bits	
Absolute accuracy				± 1.5	LSB	
Conversion time	t_{CONV}	9			t_{CYC}*	$V_{DD} - 0.5$ $\leq V_{AREF} \leq V_{DD}$
Sampling time	t_{SAMP}		1		t_{CYC}*	
Analog input voltage	V_{IAN}	A_{VSS}		V_{AREF}	V	
Analog input impedance	R_{AN}		1000		$M\Omega$	
V_{AREF} current	I_{AREF}	0.4	1	2	mA	

$$* \; t_{CYC} = \frac{2}{f_{CC}} \; (DIVSEL = 1)$$

Data Retention Timing
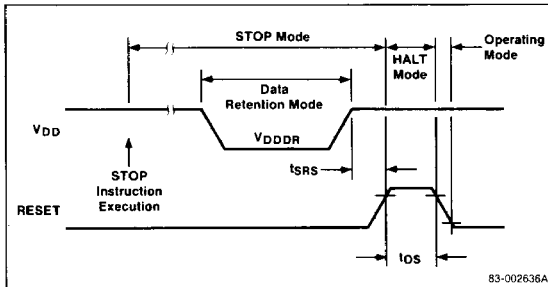
Oscillator Characteristics

$T_A = -10$ to $+70°C$, $V_{DD} = 2.7$ to 6.0 V, DIVSEL = 1

Oscillation	Configuration	Parameter	Limits			Unit	Test Conditions
			Min	Typ	Max		
Ceramic	See figure 3	Oscillation frequency (f_{CC})	390	500	510	kHz	$V_{DD} = 4.5$ to 6.0 V
			390	500	510	kHz	$V_{DD} = 4.0$ to 6.0 V
			390	500	510	kHz	$V_{DD} = 3.0$ to 6.0 V DIVSEL = 0
			390	400	410	kHz	$V_{DD} = 2.7$ to 6.0 V DIVSEL = 0
		Stabilization time	20			ms	V_{DD} greater than 4.5 V
External clock	See figure 3	CL1 input frequency	10		510	kHz	$V_{DD} = 4.5$ to 6.0 V
			10		210	kHz	
		CL1 input high, low level duration (t_{CH}, t_{CL})	1.0		50	μs	$V_{DD} = 4.5$ to 6.0 V
			1.0		50	μs	

Timing Waveforms

AC Timing Measuring Points (Except CL1)

83-002637A

Clock Timing

83-002638A

EVENT Timing

83-002639A
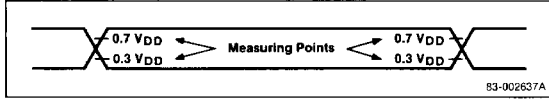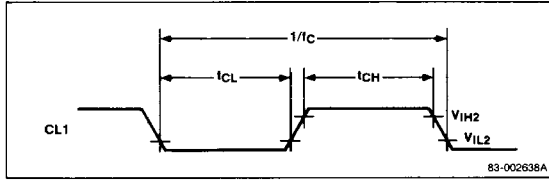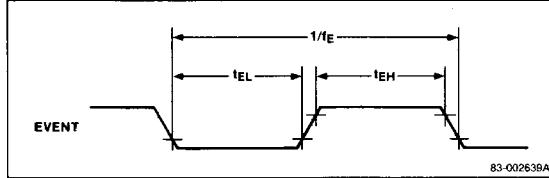
Serial Transfer Timing

83-002640A
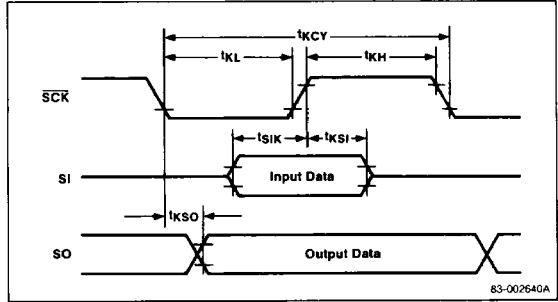
Interrupt Input Timing

83-002641A
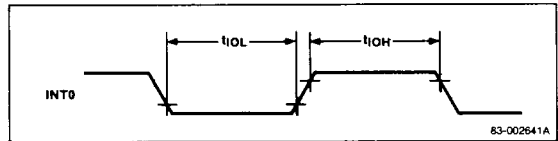
RESET Input Timing

83-002642A
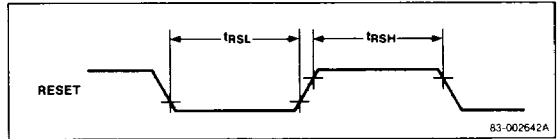
Functional Description

System Clock Generator

The ceramic oscillator circuit generates the system clock for the *µ*PD7533. Figure 2 shows that the oscillator circuit for the *µ*PD7533 includes a ceramic oscillator, two divide-by-two circuits, the DIVSEL input, and control circuitry for the standby modes, HALT and STOP.

Figure 3 shows that the ceramic oscillator requires that a ceramic resonator be connected to the CL1 and CL2 pins. An external clock can also be input at CL1. In this case, the oscillator operates as an inverted buffer.

Figure 2 shows that the output frequency from the ceramic oscillator connects either directly to the clock selector or via a divide-by-two circuit. The selector is controlled by the DIVSEL line. If DIVSEL is low, the divide-by-two frequency is selected. This option is used during a low power operating mode. If DIVSEL is high, then the direct frequency is chosen. The output of the selector is used as system clock (CL), and is also divided by two to supply the CPU clock (ϕ).

Table 1 shows how DIVSEL selects the system and CPU clocks, and machine cycle timing.

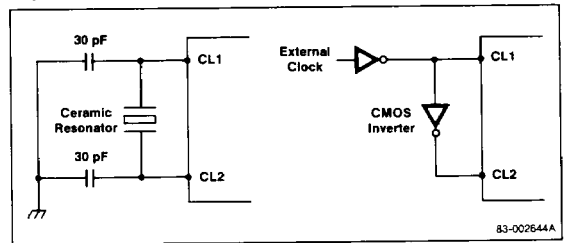### Standby Control

The HALT F/F and the STOP F/F comprise the control circuitry for standby mode (figure 2). The STOP F/F is set by the STOP instruction. When the STOP F/F is set, the ceramic oscillator stops. The rising edge of the RESET input resets the STOP F/F.
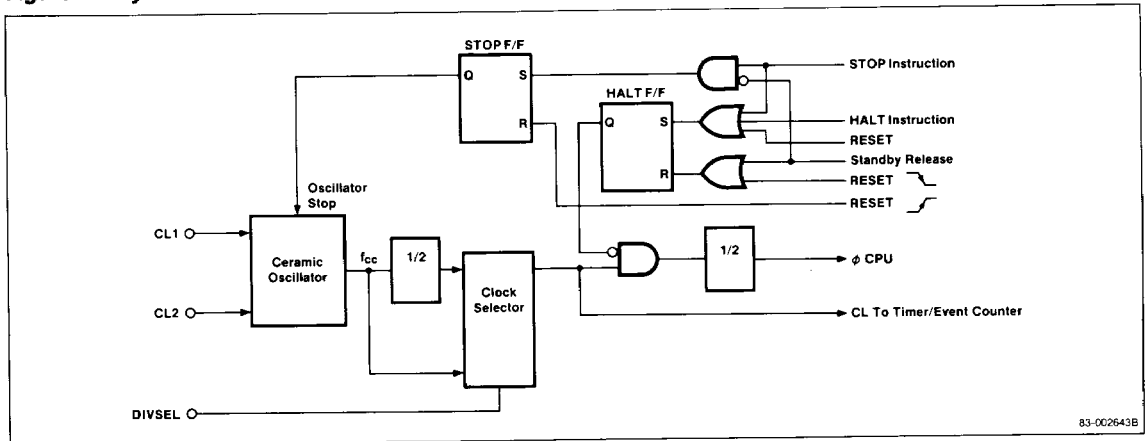
The HALT instruction sets the HALT F/F and inhibits the input of the half-frequency divider which generates the CPU clock. As a result, only the CPU clock is stopped in HALT mode. The RELEASE signal resets the HALT F/F. RELEASE becomes active when any interrupt request flag is set, or at the falling edge of the RESET input.

While RESET is active, the HALT F/F is set, and the chip goes into the HALT mode. At a power-on Reset, the ceramic oscillation is driven when the RESET input signal becomes high.

Figure 3. Clock Driver Configuration

Table 1. Clock Selection

DIVSEL	System Clock (CL)	CPU Clock (ϕ)	Machine Cycle
Low	200 kHz	100 kHz	10 μs
High	400 kHz	200 kHz	5 μs

Figure 2. System Clock Generator

It takes a short period of time for the oscillator output to become stable. To prevent errors due to an unstable clock, the HALT F/F is set to inhibit the CPU clock while the RESET input is high. Therefore, the high-level pulse width for the RESET input should be wide enough to cover the required time for the ceramic resonator oscillation to stabilize.
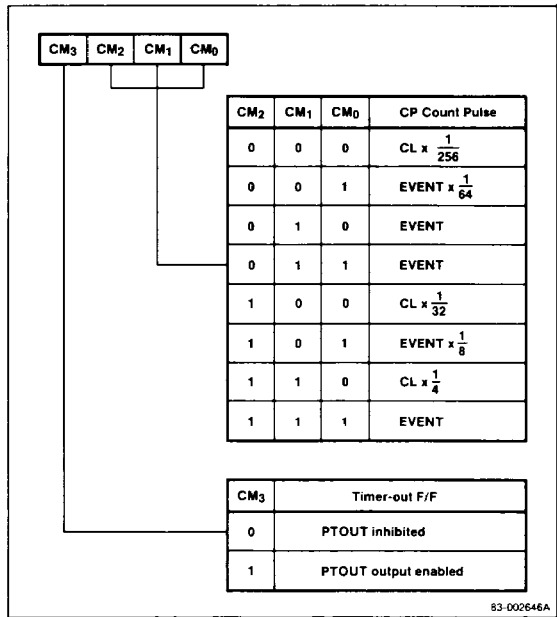
Clock Control

Figure 4 shows that the clock controller contains a 4-bit clock mode register (CM0-CM3), prescalers 1-3, and multiplexers. The clock controller selects the clock sources and prescalers, and supplies the count pulses (CP) to the timer/event counter. The clock sources are the system clock generator output (CL) or the EVENT pulse.

The OP 12 or OPL (L = 12) instruction sets codes in the clock mode register. CM3 designates the output of the timer-out signals. If CM3 = 1, the output of the timer-out F/F (TOUT) is available at the PTOUT (P21) pin.
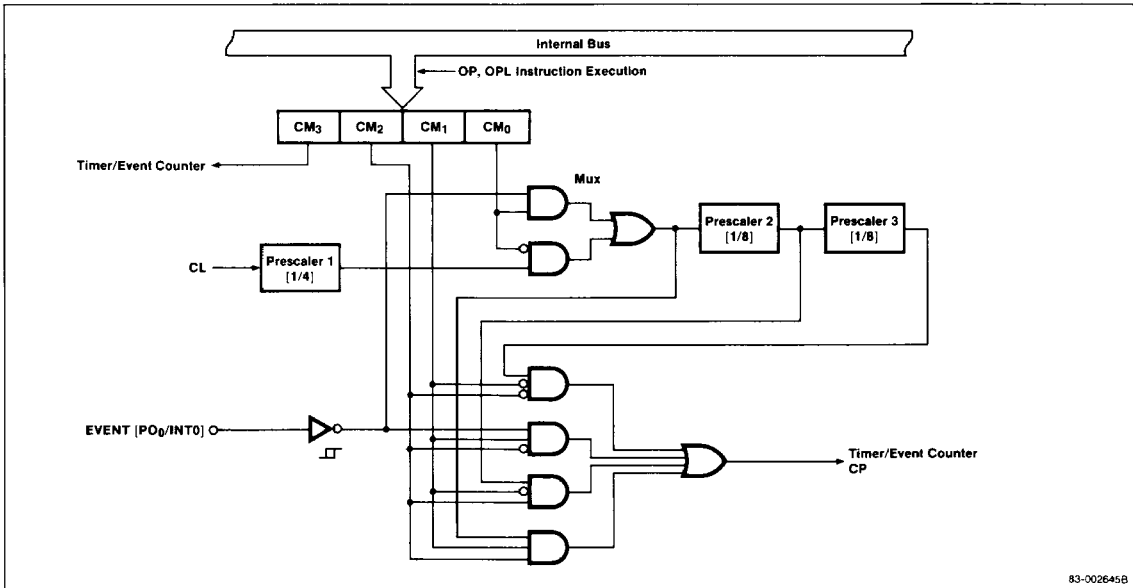
Figure 5 shows the format of the clock mode register.

Figure 5. Format of Clock Mode Register

CM2	CM1	CM0	CP Count Pulse
0	0	0	$CL \times \frac{1}{256}$
0	0	1	$EVENT \times \frac{1}{64}$
0	1	0	EVENT
0	1	1	EVENT
1	0	0	$CL \times \frac{1}{32}$
1	0	1	$EVENT \times \frac{1}{8}$
1	1	0	$CL \times \frac{1}{4}$
1	1	1	EVENT

CM3	Timer-out F/F
0	PTOUT inhibited
1	PTOUT output enabled

83-002646A

Figure 4. Clock Controller Block Diagram

83-002645B

Timer/Event Counter

Figure 6 shows the timer/event counter has an 8-bit count register, 8-bit modulo register, an 8-bit comparator, and a timer-out flip flop.

Timer Operation

After the TAMMOD instruction sets a count value in the modulo register and the TIMER instruction clears the contents of the count register, the timer starts counting count pulses (CP). If an external clock is used, the count pulses are synchronized with the rising edge of CL1 or the $P0_0$ input.

When the value of the modulo register equals the value of the count register, the comparator generates a coincidence signal (INTT) to set an interrupt request flag. Then it clears the count register to repeat the counting. In this manner, the timer functions as an interval timer whose interval is set by the modulo register.

Regardless of any instructions, the count pulses are always input into the count register, updating the count value. If the contents of the count register are equal to those of the modulo register, the INTT request flag is then set. For this reason, inhibit INTT interrupts when not using the timer.

Event Counter Operation

To use the timer/event counter as an event counter, input the external event pulse into the $P0_0$ pin, and select $P0_0'$ as the count pulse (CP) for the clock controller. The count register counts the external event pulses input at the $P0_0$ pin, either as they are, or frequency divided.

As a result, the timer/event counter operates as an event counter that generates interrupts after observing the number of counts (events) specified by the modulo register. The TCNTAM instruction can read the current count at any time.

Set the modulo register with the number of count pulses minus one. If set to 0, no counting will occur because the counter register is held at 0 (both the detection of coincidence and zero-clearing are simultaneously made).

Figure 6. Block Diagram of Timer/Event Counter
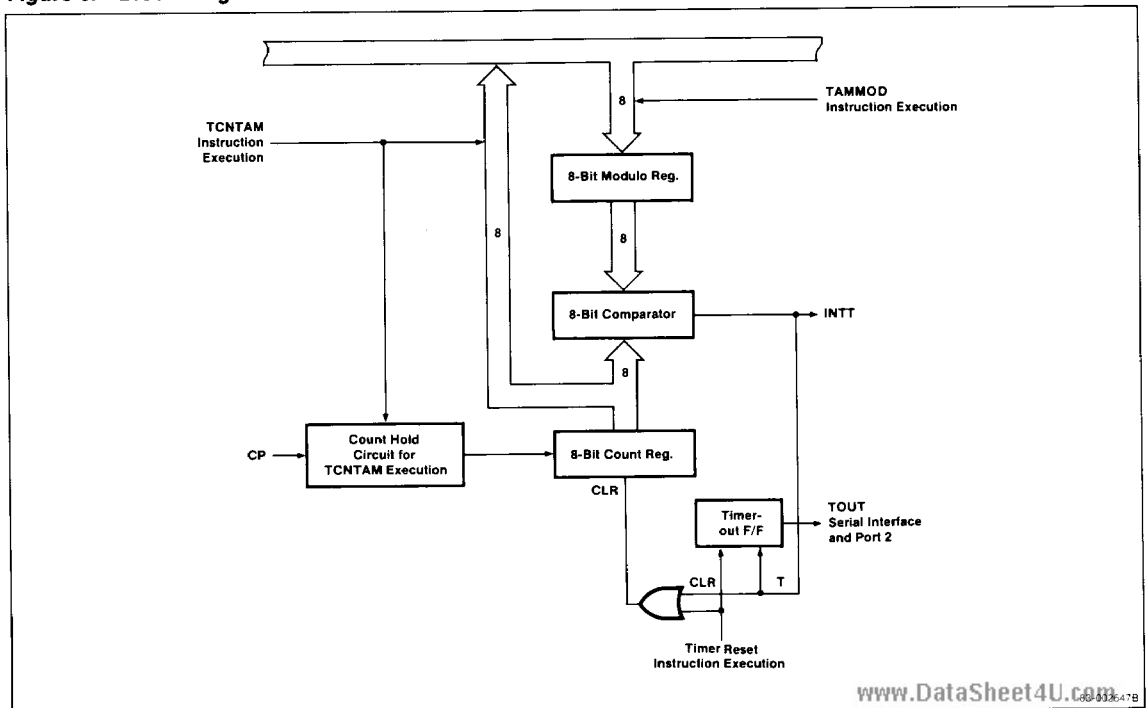
Serial Interface

As figure 7 shows, the serial interface includes an 8-bit shift register, a 4-bit shift mode register, and a 3-bit counter.

The serial clock controls serial data I/O. At the falling edge of the serial clock ($\overline{SCK}$), the SO line outputs the most significant bit (7) of the shift register. The contents of the shift register are shifted by one bit at the rising edge of the next serial clock ($n \leftarrow 0\ n+1$). At the same time, the data on the SI line is loaded into the least significant bit (0) of the shift register.

The 3-bit counter (octal counter) counts up the serial clocks and generates an internal interrupt signal INTS at every count of 8 clocks (at the end of a 1-byte serial data transfer). It then sets the interrupt request flag (INTO/S RQF). The TAMSIO instruction sets data in the shift register during the transmission of serial data, then starts transmission. At the end of the transmission of each byte (8 bits) an internal interrupt (INTS) is generated.

The SIO instruction also starts the reception of serial data. The received data is taken from the shift register by executing the TSIOAM instruction after an interrupt (INTS) is generated by the reception of one byte of data.

The end of a 1-byte transfer can be confirmed by testing the INTS RQF with the SKI instruction instead of interrupt processing.

The following three types of serial clock sources are available: system clock ϕ, external clock ($\overline{SCK}$ input), and timer-out F/F output signal (TOUT). Bits SM_2-SM_0 of the shift mode register select the clock source.

If the system clock ϕ is chosen, execute the SIO instruction to supply the clock to the serial interface, controlling the input/output of serial data while ϕ is output from the $\overline{SCK}$ pin.

After eight ϕ pulses, the clock is automatically discontinued by holding the $\overline{SCK}$ output at a high level. Therefore, the input/output of serial data automatically stops after each byte has been transferred. Consequently, the software does not need to control the serial clock and the transfer rate is determined by the system clock frequency.

In this mode, after six machine cycles from the execution of the SIO, the TSIOAM instruction can read out the received data from the shift register or can write in the next transmit data.

Figure 8 shows the shift mode register format.

Figure 7. Serial Interface Block Diagram
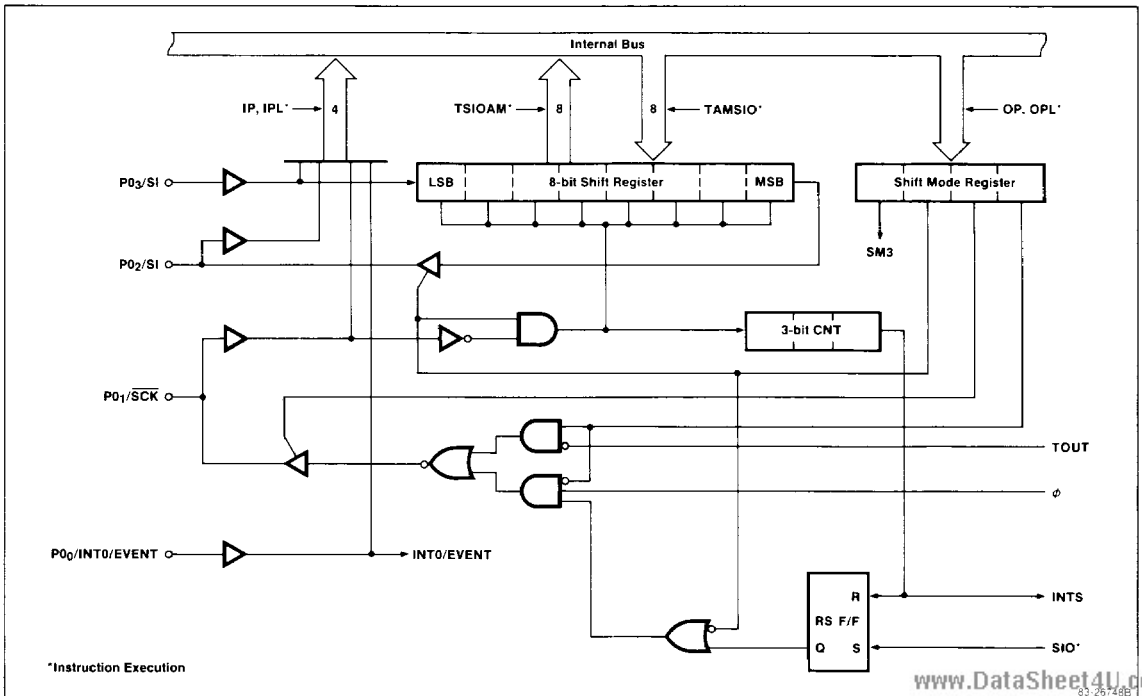
Figure 8.   Format of Shift Mode Register

SM$_2$	SM$_1$	SM$_0$	PO$_3$/SI	PO$_2$/SO	PO$_1$/$\overline{\text{SCK}}$	Serial Operation
0	0	0	Port input	Port input	Port input	Stops
0	1	0			Outputs ϕ continuously	
0	1	1			Outputs TOUT continuously	
1	0	0	SI input	SO output	$\overline{\text{SCK}}$ input	Operates with external clock
1	1	0			$\overline{\text{SCK}}$ output (ϕ x 8)	Operates with ϕ
1	1	1			$\overline{\text{SCK}}$ output (TOUT)	Operates with TOUT

Bit SM$_3$ selects the interrupt source in the following manner:

SM$_3$	Interrupt Source
0	INTS
1	INT0

If the external clock ($\overline{\text{SCK}}$ input) is selected, the serial clocks are input from $\overline{\text{SCK}}$. When the eighth external serial clock is input, an internal interrupt (INTS) is generated, signalling the end of a 1-byte data transfer.

Since the serial clocks are not internally inhibited, the external clock must hold the signal high after eight clocks. The external serial clock determines the transfer rate. The serial interface can be operated from DC to the maximum rate in the electrical specifications.

If TOUT is selected, the half-frequency divided co-incidence signal of the timer/event counter is the serial clock. This serial clock controls the input/output of the serial data and is output from the $\overline{\text{SCK}}$ pin.

The count pulse supplied to the timer/event counter and the value set in the modulo register determine the transfer rate. The end of a 1-byte data transfer is signalled by INTS. TOUT is not inhibited automatically, therefore the program should stop TOUT at intervals of 16.

To use the external clock or the TOUT signal, execute the SIO, TAMSIO or TSIOAM instructions while the serial clock ($\overline{\text{SCK}}$) is held high. Operation cannot be guaranteed if these intructions are executed over the rising or falling edge of $\overline{\text{SCK}}$, or at the low level.

In a system that does not require serial data transfer, the 8-bit shift register can be ued as a register with the serial operation stopped. The TSIOAM or TAMSIO instruction can read or write data.
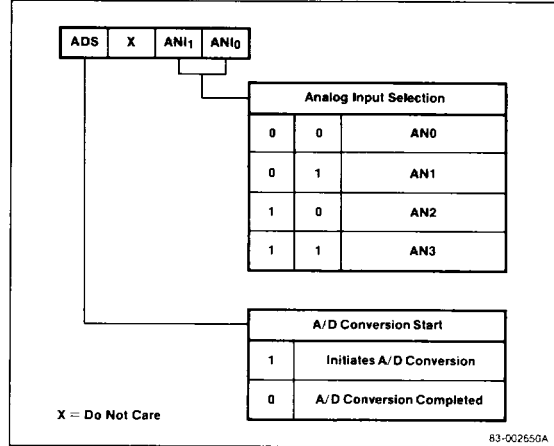
Analog to Digital Converter

The μPD7533 integrates a 4-channel 8-bit A/D converter with separate positive reference and ground from the device power supply. Figure 9 shows that the A/D converter includes an A/D converter mode register, successive approximation (SA) register, and end of conversion (EOC) control circuitry.

A/D Converter Mode Register

The A/D converter mode register is a 4-bit internal port that controls the A/D circuitry. The lower two bits, ANI0 and ANI1, select which analog signal (AN0-AN3) is input to the A/D converter. The most significant bit, ADS, initiates the A/D conversion. If ADS is set to a logic 1, the analog signal selected by ANI1 and ANI0 is converted to 8-bit digital data. Upon completion of the data conversion, ADS is cleared to 0.
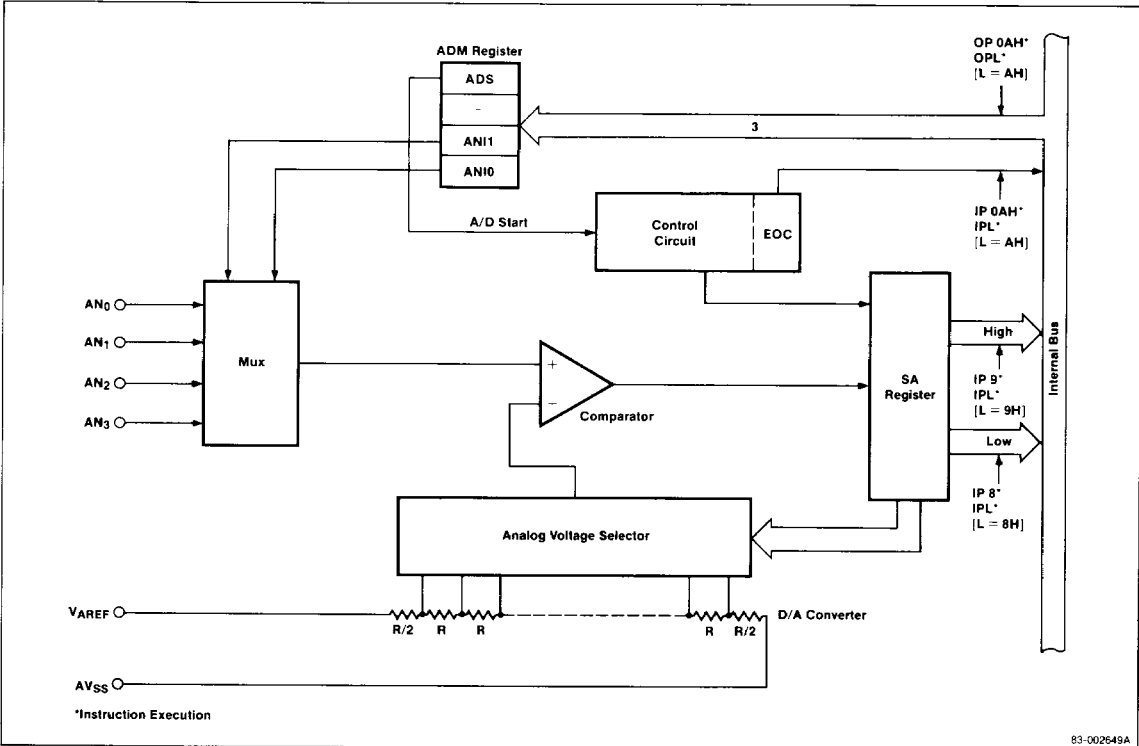
Figure 10 shows the format for the A/D conversion mode register.

Figure 10. A/D Conversion Mode Register Format

| ADS | X | ANI1 | ANI0 |

		Analog Input Selection
0	0	AN0
0	1	AN1
1	0	AN2
1	1	AN3

	A/D Conversion Start
1	Initiates A/D Conversion
0	A/D Conversion Completed

X = Do Not Care

Figure 9. A/D Converter Block Diagram

*Instruction Execution

Successive Approximation [SA]

The 8-bit data converted from the analog signal using the successive approximation method is stored in the SA register. When ADS is set to a logic 1, the contents of the SA register are undetermined. The SA register is set to 7FH after a reset.

End of Conversion [EOC] Flag

The EOC flag specifies the completion of an A/D conversion. When ADS is set to 1, the EOC flag is set to a logic 0 and an A/D conversion starts. When the 8-bit A/D conversion is complete, the EOC flag is set to a logic 1. The EOC flag resides in bit 2 of internal Port A. The IP 0AH or IPL instruction can read the contents of Port A when the L register is set to 0AH. The contents of Port A (other than bit 2) will be read as a logic 0. The EOC flag is set to 1 after a reset.

A/D Converter Operation

An OP 0AH or OPL instruction selects one of four analog signals and starts a conversion when the L register is set to 0AH. The lower two bits of the accumulator specify which analog signal will be converted. Bit 3 of the accumulator sets to 1 to initiate the A/D conversion. The A/D conversion requires 9 machine cycles for completion. When the conversion is complete, the EOC flag is set.

In order to assure an accurate data conversion, do not execute an output instruction when EOC is a logic 0.

Figure 11 shows how the analog input voltage corresponds to the converted digital data.

Figure 11. A/D Conversion Graph
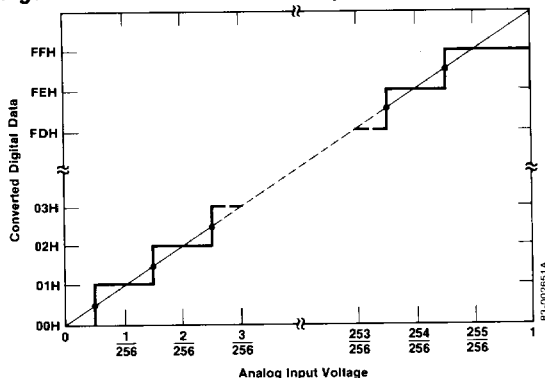
Reading Converted Data

Internal port 9 specifies the upper four bits of the SA register. Therefore, execute an IP 9 or IPL (L = 9) instruction to read the data in the accumulator.
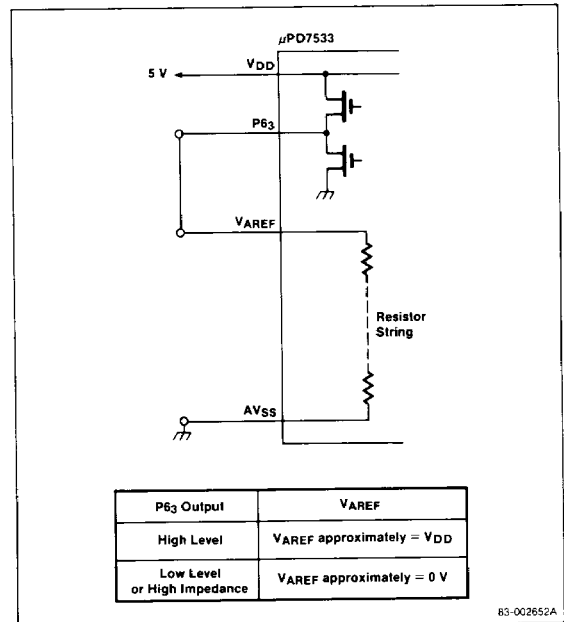
Internal port 8 specifies the lower four bits of the SA register. Therefore, execute an IP 8 or IPL (L = 8) instruction to read the data in the accumulator. Do not read the SA register until EOC is set to 1.

Figure 12 shows the configuration for the A/D converter reference voltage during standby mode.
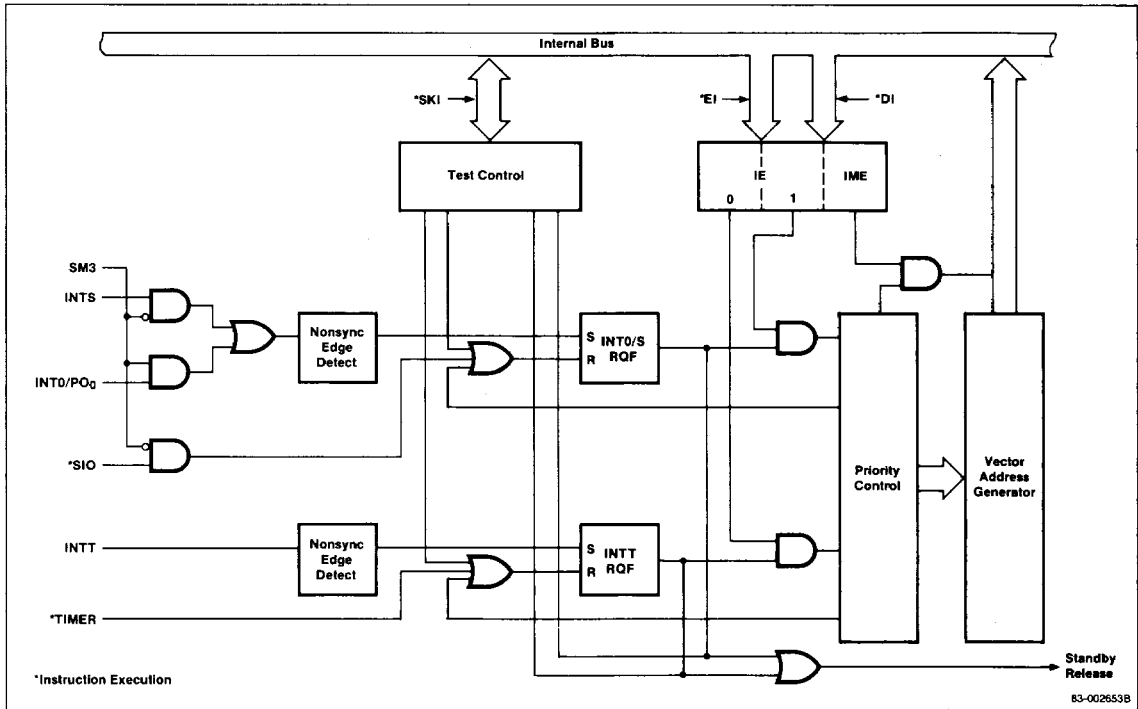
Interrupt Function

The μPD7533 provides one external interrupt and two types of internal interrupts. The $P0_0$ pin is used as the input pin for external interrupt INT0. INT0 shares priority and vectored addresses with internal interrupt INTS. Figure 13 shows the interrupt controller block diagram.

Figure 12. Configuration of V_{AREF} for Standby Mode Operation

$P6_3$ Output	V_{AREF}
High Level	V_{AREF} approximately = V_{DD}
Low Level or High Impedance	V_{AREF} approximately = 0 V

Figure 13. Interrupt Controller Block Diagram

Standby Function

The µPD7533 has two types of standby modes (STOP and HALT) to minimize power consumption during a program standby state. STOP mode is set by the STOP instruction and HALT mode by the HALT instruction.

When standby mode is set, program execution is stopped, and the contents of all internal registers and data memory are held. However, it is possible to operate the shift register and the timer/event counter. An interrupt or reset releases standby mode. Since an interrupt releases standby mode, neither STOP nor HALT modes can be set if an interrupt request flag is set. Therefore, when setting standby mode when there is a possibility of a request flag being set, first reset the interrupt request flag by processing the interrupt in advance or by executing the SKI instruction.

The major difference in the two modes is that crystal oscillation (CL) stops in STOP mode but does not stop in HALT mode.

In STOP mode, it is possible to go into data retention mode by lowering the power supply voltage. During data retention mode, all operation stops and only the data RAM stays intact.

Table 2 shows the differences between STOP and HALT modes.

Table 2. Differences Between STOP and HALT Modes

	Mode	
Operation	STOP Mode	HALT Mode
Ceramic Oscillation	X (1)	O (2)
1/2 Ceramic Oscillation	X (1)	X (1)
CPU	X (1)	X (1)
Serial I/O	(3)	(2)
Timer/Event Counter	X (1)	O (2)
A/D Converter	X (1)	O (2)
Release of Standby Mode	RESET	INT0/S RQF NTT RQF RESET Input

Note:

(1) Not possible
(2) Possible
(3) Possible depending on clock source selected

STOP Mode

In STOP mode, ceramic oscillation and the half-frequency divider stop. The CPU stops and the operations requiring the system clock (CL, 0) stop.

Release from STOP mode is with the RESET input only. All other functions cease to operate.

In order to minimize power consumption, the current flowing through the resistor ladder of the A/D converter must be minimized. To minimize power consumption, turn off the power to the V_{AREF} pin.

Note that ceramic oscillation stops and disables the system clock during STOP mode by bringing CL2 to ground. Therefore, if the external clock is connected to CL1 and a STOP instruction is executed, the CPU will enter HALT mode instead.

HALT Mode

In HALT mode, only the half-frequency divider circuit stops in the clock generator circuit (CL operates, ϕ stops). Therefore, the CPU and the operation of the serial interface (when using ϕ as a serial clock) stop.

However, since the clock control circuit is still in operation, it can select the CL signal from the clock generator or the EVENT input and supply the count pulse (CP) to the timer/event counter.

Consequently, the timer/event counter can be operated in HALT mode. The serial interface operates if a serial clock other than ϕ (such as the external clock, TOUT signal) is selected. The HALT mode is released by the RESET input or an interrupt, even if the interrupt is disabled.

Release from Standby Mode by Interrupt

The standby mode is released when the interrupt request flag is set by an interrupt source, whether interrupts are disabled or enabled. However, the operations after release differ in each case.

If the interrupt master enable F/F is enabled, and if the interrupt is enabled, the corresponding interrupt routine is initiated after execution of one instruction after the STOP/HALT instruction. Then, the result flag is reset. If the corresponding bit of the interrupt enable register has been reset, execution of instructions starts after the STOP/HALT instruction, and the interrupt routine is not initiated. In this case, the request flag for release remains set. If necessary, reset the request flag with the SKI instruction.

If the interrupt master enable F/F is disabled, the instruction following the STOP/HALT instruction is executed regardless of the state of the interrupt enable register (interrupt routine is not initiated). In this case, the interrupt request flag is left set. If necessary, it can be reset by the SKI instruction.

After any release, operation resumes with the same register contents as before standby mode.

## Release From Standby Mode with RESET

Both STOP and HALT modes are released unconditionally by the RESET input. Figure 14 shows the release timing.

If the device is reset during STOP mode, the low to high transition of the RESET pin will take the processor from STOP mode to HALT mode. When RESET goes high to low, the HALT mode is abandoned, and after a normal reset operation, the PC is initialized to 0. Only the data memory will stay intact during the HALT mode, but all registers become undefined.

If the device is reset during HALT mode, the high to low transition of RESET will release the device from standby mode. After a normal reset operation, the PC is initialized to 0. Only the data memory will stay intact during the HALT mode, but all registers become undefined.

Figure 15 shows the release from HALT mode by RESET.

Figure 14.   Release from STOP mode by RESET
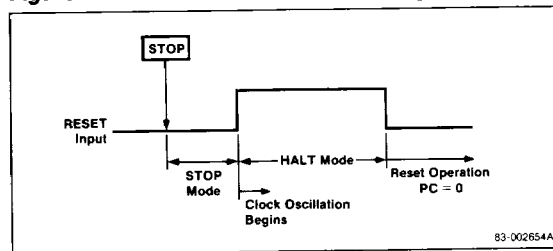
Figure 15.   Release from HALT Mode by RESET
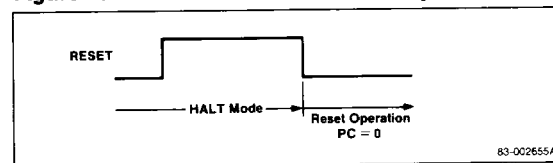
Reset Function

The µPD7533 is reset and initialized by the input of the RESET signal (active high).

A RESET causes the CPU to initialize in the following manner:

- Program counter (PC) is cleared to 0
- Skip flags (SK1, SK0) and program status word (PSW) are reset to 0
- Timer/event counter:
  — Count register = 00H
  — Modulo register = FFH
  — Timer-out F/F = 0
- Clock control circuitry:
  — Clock mode register (CM_3-CM_0) = 0
  — $CP = \dfrac{CL}{256}$
  — Timer-out FF signal not output to PTOUT
  — Prescalers 1-3 = 0
- Shift Mode Register (SM_3-SM_0) is cleared to 0.
  — Shift operation stops
  — Port 0 is in input mode (high impedance)
  — INTS is selected interrupt source of INT0/S
- A/D converter circuit:
  — ADM register is set to 0
  — AN0 is selected
  — SA register is set to 7FH
  — EOC flag is set to logic 1
- Interrupt control circuit:
  — Interrupt request flags = 0
  — Interrupt master enable F/F = 0
  — Interrupt enable register = 0
  — All pending interrupts are cancelled
  — All interrupts are disabled
- All Port 2-7 output buffers are turned off
- Contents of data memory and the following registers are undefined:
  — Stack pointer (SP)
  — Accumulator (A)
  — Carry flag (C)
  — General purpose registers (H,L)
  — All port output latches
  — Shift register

Power-on Reset Circuit

Figure 16 shows an example of the simplest power-on reset circuit using a resistor and a capacitor.

Figure 16.   Power-on Reset Circuit