

Silicon NPN Darlington Power Transistors

2SD2557

DESCRIPTION

- With TO-3PN package
- DARLINGTON

APPLICATIONS

- Series regulator and general purpose

PINNING

PIN	DESCRIPTION
1	Base
2	Collector;connected to mounting base
3	Emitter

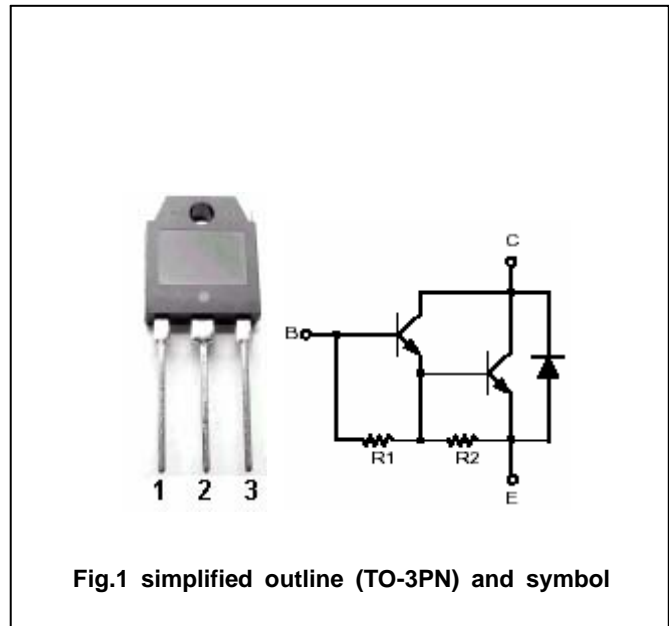


Fig.1 simplified outline (TO-3PN) and symbol

Absolute maximum ratings(Ta=)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	200	V
V_{CEO}	Collector-emitter voltage	Open base	200	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		5	A
I_B	Base current		2	A
P_C	Collector power dissipation	$T_C=25$	70	W
T_j	Junction temperature		150	
T_{stg}	Storage temperature		-55~150	

Silicon NPN Darlington Power Transistors

2SD2557

CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =10mA ; I _B =0	200			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =1A ; I _B =5mA			1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =200V; I _E =0			100	μA
I _{EBO}	Emitter cut-off current	V _{EB} =6V; I _C =0			5	mA
h _{FE}	DC current gain	I _C =1A ; V _{CE} =5V	1500		6500	
C _{ob}	Output capacitance	I _E =0 ; V _{CB} =10V; f=1MHz		110		pF
f _T	Transition frequency	I _E =0.5A ; V _{CE} =10V		15		MHz

Silicon NPN Darlington Power Transistors

2SD2557

PACKAGE OUTLINE

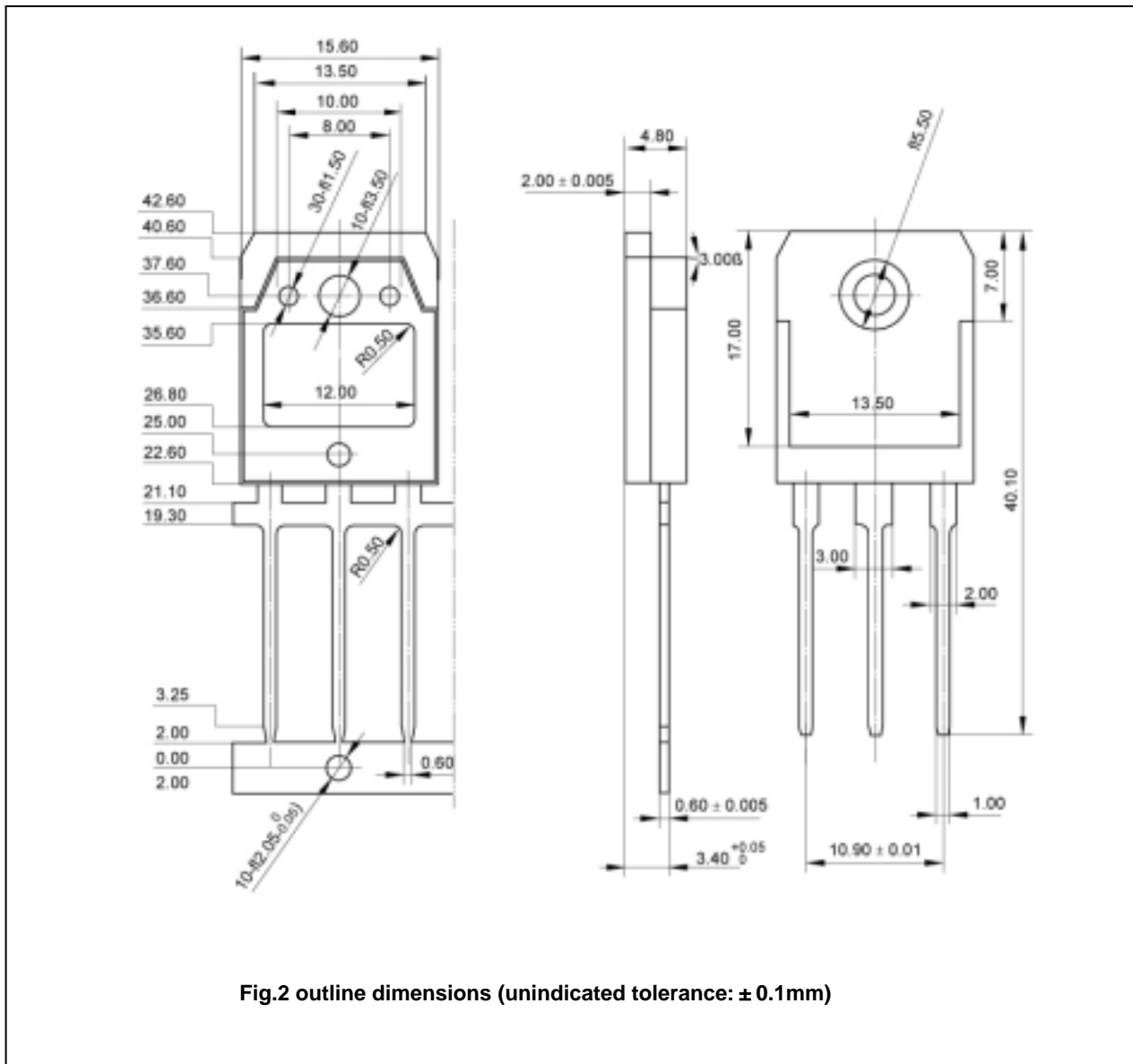


Fig.2 outline dimensions (unindicated tolerance: ± 0.1 mm)