

## TrenchMOS™ transistor Standard level FET

BUK7608-55

### GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using 'trench' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

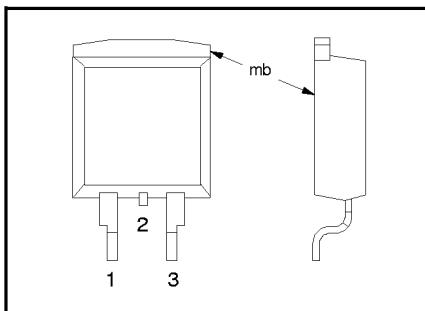
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	Drain-source voltage	55	V
$I_D$	Drain current (DC)	75	A
$P_{tot}$	Total power dissipation	187	W
$T_j$	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 10$ V	8	mΩ

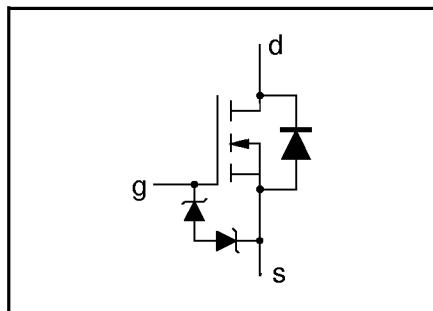
### PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

### PIN CONFIGURATION



### SYMBOL



### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	-	-	55	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20$ kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
$I_D$	Drain current (DC)	$T_{mb} = 25$ °C	-	75	A
$I_D$	Drain current (DC)	$T_{mb} = 100$ °C	-	65	A
$I_{DM}$	Drain current (pulse peak value)	$T_{mb} = 25$ °C	-	240	A
$P_{tot}$	Total power dissipation	$T_{mb} = 25$ °C	-	187	W
$T_{stg}, T_j$	Storage & operating temperature	-	-55	175	°C

### ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_C$	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th j-mb}$	Thermal resistance junction to mounting base	-	-	0.8	K/W
$R_{th j-a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

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**STATIC CHARACTERISTICS** $T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.25 \text{ mA}$	55	-	-	V
$V_{GS(\text{TO})}$	Gate threshold voltage	$T_j = -55^\circ\text{C}$ $V_{DS} = V_{GS}; I_D = 1 \text{ mA}$	50	-	-	V
$I_{DSS}$	Zero gate voltage drain current	$T_j = 175^\circ\text{C}$ $V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}$	2	3.0	4.0	V
$I_{GSS}$	Gate source leakage current	$T_j = -55^\circ\text{C}$ $V_{GS} = \pm 10 \text{ V}; V_{DS} = 0 \text{ V}$	1	-	-	V
$\pm V_{(\text{BR})\text{GSS}}$	Gate-source breakdown voltage	$T_j = 175^\circ\text{C}$ $I_G = \pm 1 \text{ mA}$	-	0.05	10	$\mu\text{A}$
$R_{DS(\text{ON})}$	Drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}$ $T_j = 175^\circ\text{C}$	16	-	500	$\mu\text{A}$
			-	0.02	1	$\mu\text{A}$
			-	-	20	$\mu\text{A}$
			-	-	-	V
			-	6.5	8	$\text{m}\Omega$
			-	-	17	$\text{m}\Omega$

**DYNAMIC CHARACTERISTICS** $T_{mb} = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$g_{fs}$	Forward transconductance	$V_{DS} = 25 \text{ V}; I_D = 25 \text{ A}$	10	45	-	S
$C_{iss}$	Input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}$	-	3600	4500	pF
$C_{oss}$	Output capacitance		-	830	1000	pF
$C_{rss}$	Feedback capacitance		-	320	440	pF
$t_{d\text{ on}}$	Turn-on delay time	$V_{DD} = 30 \text{ V}; I_D = 25 \text{ A}$	-	27	40	ns
$t_r$	Turn-on rise time	$V_{GS} = 10 \text{ V}; R_G = 10 \Omega$	-	70	105	ns
$t_{d\text{ off}}$	Turn-off delay time	Resistive load	-	100	140	ns
$t_f$	Turn-off fall time		-	50	70	ns
$L_d$	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
$L_s$	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

**REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS** $T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DR}$	Continuous reverse drain current		-	-	75	A
$I_{DRM}$	Pulsed reverse drain current		-	-	240	A
$V_{SD}$	Diode forward voltage	$I_F = 25 \text{ A}; V_{GS} = 0 \text{ V}$	-	0.85	1.2	V
		$I_F = 75 \text{ A}; V_{GS} = 0 \text{ V}$	-	1.0	-	V
$t_{rr}$	Reverse recovery time	$I_F = 75 \text{ A}; -dI_F/dt = 100 \text{ A}/\mu\text{s}$	-	65	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{GS} = -10 \text{ V}; V_R = 30 \text{ V}$	-	0.18	-	$\mu\text{C}$

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### AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$W_{DSS}$	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 75 \text{ A}$ ; $V_{DD} \leq 25 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; $R_{GS} = 50 \Omega$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	-	500	mJ

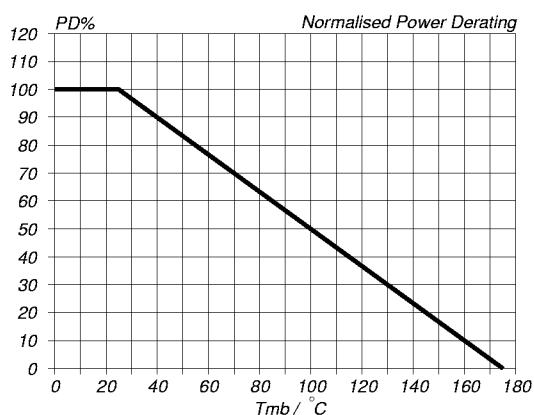


Fig.1. Normalised power dissipation.  
 $PD\% = 100 \cdot P_D / P_{D, 25 \text{ }^\circ\text{C}} = f(T_{mb})$

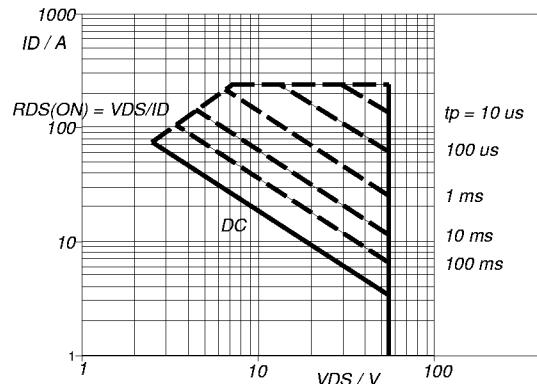


Fig.3. Safe operating area.  $T_{mb} = 25 \text{ }^\circ\text{C}$   
 $I_D$  &  $I_{DM} = f(V_{DS})$ ;  $I_{DM}$  single pulse; parameter  $t_p$

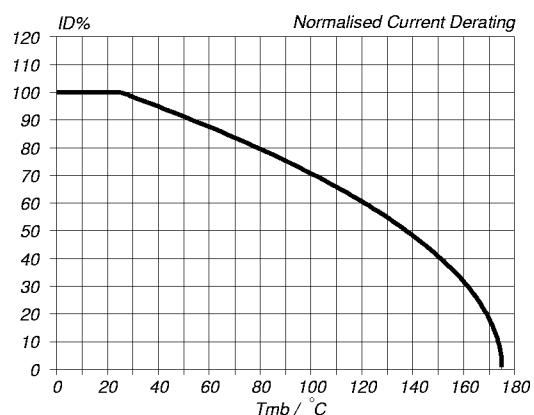


Fig.2. Normalised continuous drain current.  
 $ID\% = 100 \cdot I_D / I_{D, 25 \text{ }^\circ\text{C}} = f(T_{mb})$ ; conditions:  $V_{GS} \geq 5 \text{ V}$

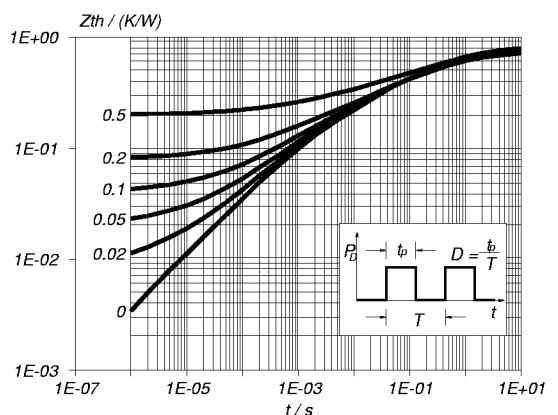


Fig.4. Transient thermal impedance.  
 $Z_{th,j-mb} = f(t)$ ; parameter  $D = t_p/T$

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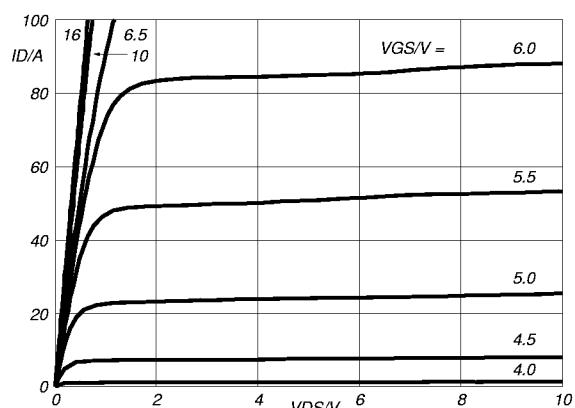


Fig.5. Typical output characteristics,  $T_j = 25^\circ\text{C}$ .  
 $I_D = f(V_{DS})$ ; parameter  $V_{GS}$

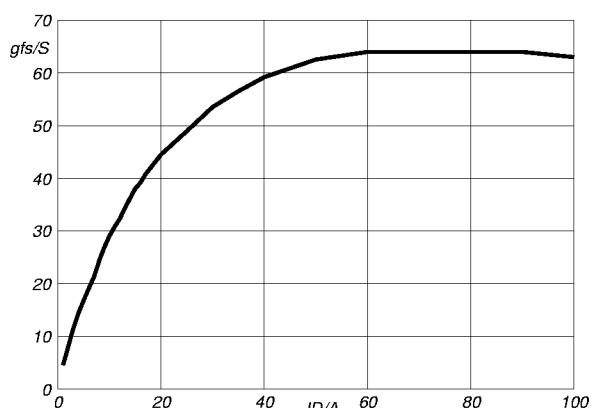


Fig.8. Typical transconductance,  $T_j = 25^\circ\text{C}$ .  
 $g_{fs} = f(I_D)$ ; conditions:  $V_{DS} = 25$  V

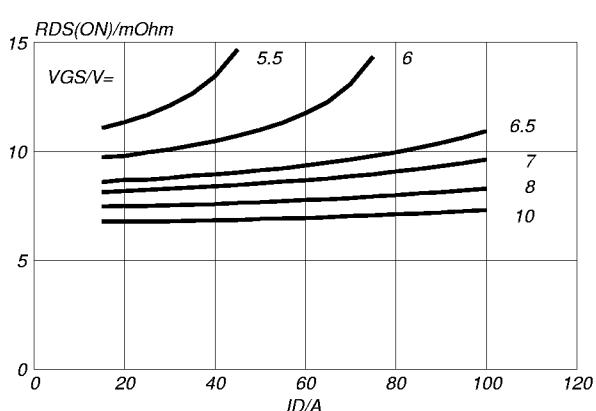


Fig.6. Typical on-state resistance,  $T_j = 25^\circ\text{C}$ .  
 $R_{DS(ON)} = f(I_D)$ ; parameter  $V_{GS}$

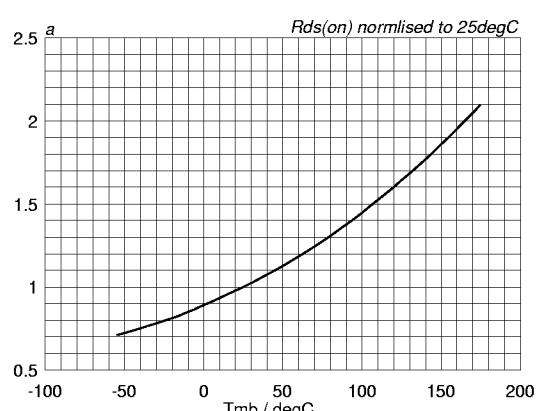


Fig.9. Normalised drain-source on-state resistance.  
 $a = R_{DS(ON)}/R_{DS(ON)25^\circ\text{C}} = f(T_j)$ ;  $I_D = 25$  A;  $V_{GS} = 5$  V

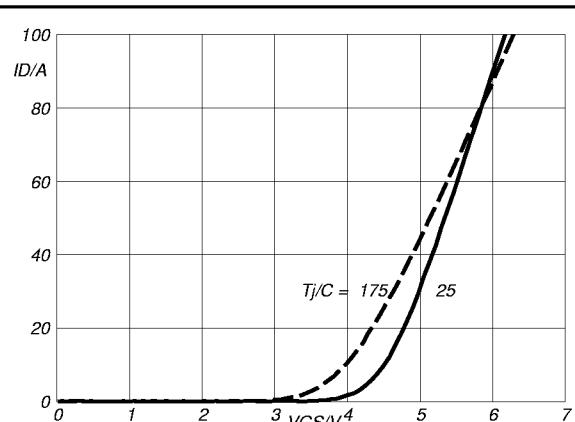


Fig.7. Typical transfer characteristics.  
 $I_D = f(V_{GS})$ ; conditions:  $V_{DS} = 25$  V; parameter  $T_j$

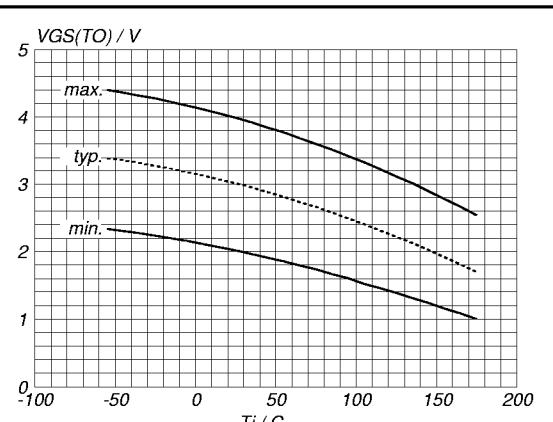


Fig.10. Gate threshold voltage.  
 $V_{GS(TO)} = f(T_j)$ ; conditions:  $I_D = 1$  mA;  $V_{DS} = V_{GS}$

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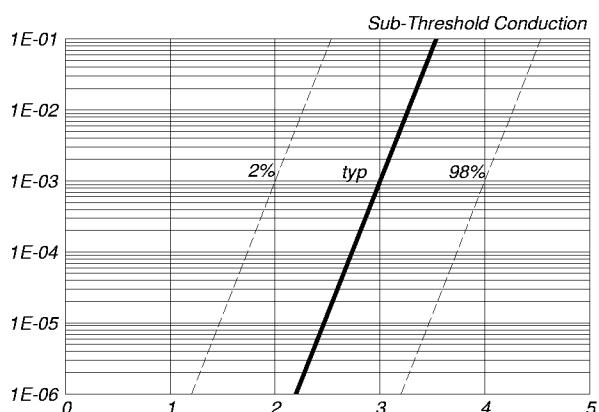


Fig.11. Sub-threshold drain current.  
 $I_D = f(V_{GS})$ ; conditions:  $T_j = 25^\circ C$ ;  $V_{DS} = V_{GS}$

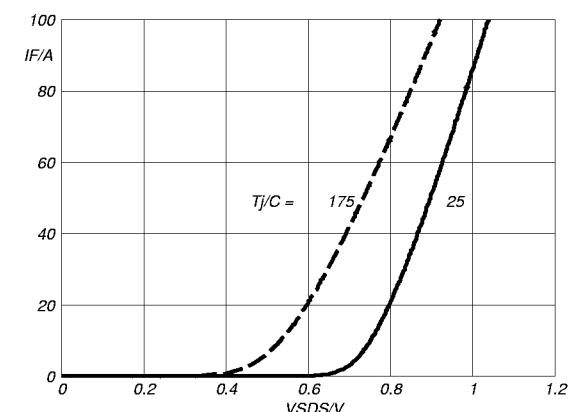


Fig.14. Typical reverse diode current.  
 $I_F = f(V_{SDS})$ ; conditions:  $V_{GS} = 0 V$ ; parameter  $T_j$

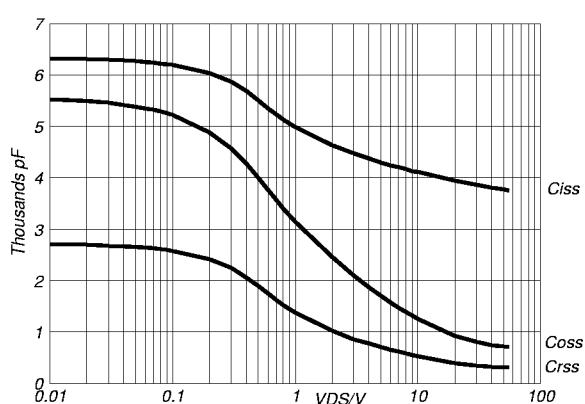


Fig.12. Typical capacitances,  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$ .  
 $C = f(V_{DS})$ ; conditions:  $V_{GS} = 0 V$ ;  $f = 1 MHz$

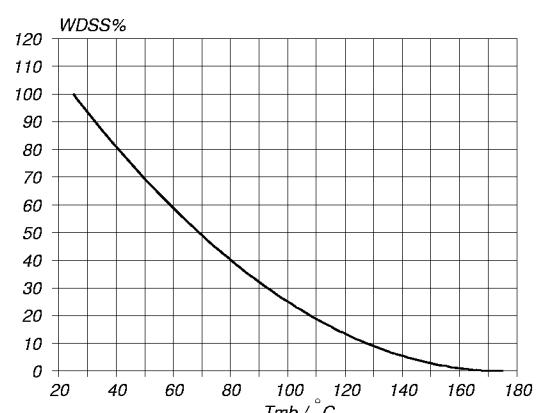


Fig.15. Normalised avalanche energy rating.  
 $W_{DSS}\% = f(T_{mb})$ ; conditions:  $I_D = 75 A$

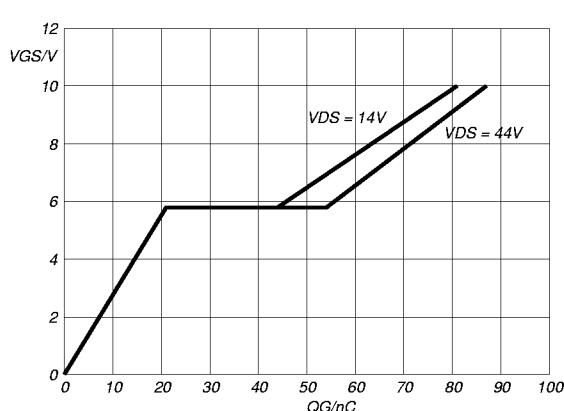


Fig.13. Typical turn-on gate-charge characteristics.  
 $V_{GS} = f(Q_G)$ ; conditions:  $I_D = 50 A$ ; parameter  $V_{DS}$

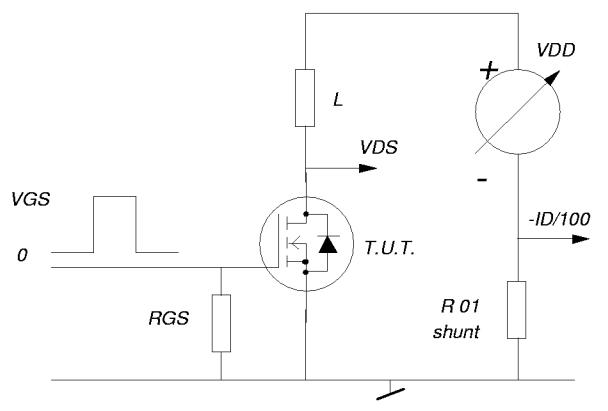
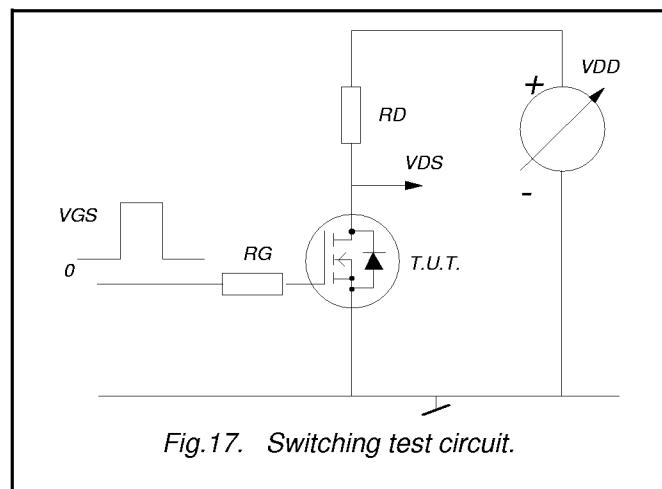


Fig.16. Avalanche energy test circuit.  
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

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### MECHANICAL DATA

*Dimensions in mm*

Net Mass: 1.4 g

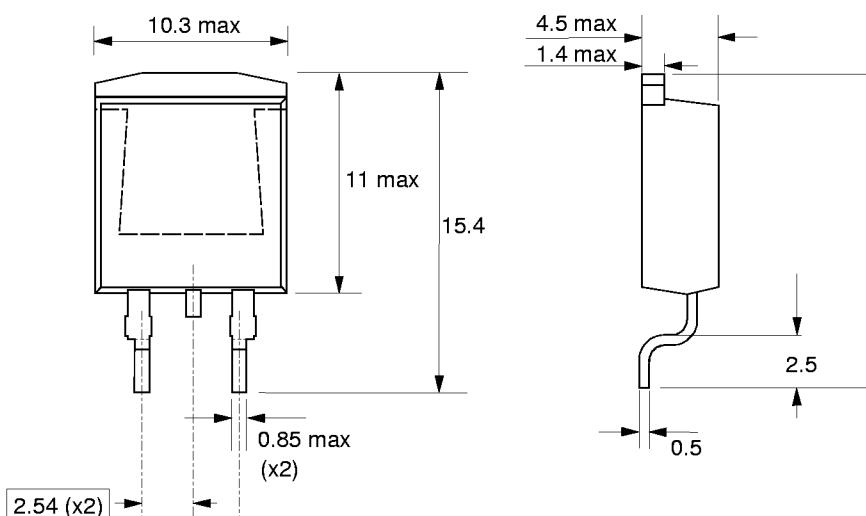


Fig.18. SOT404 : centre pin connected to mounting base.

### MOUNTING INSTRUCTIONS

*Dimensions in mm*

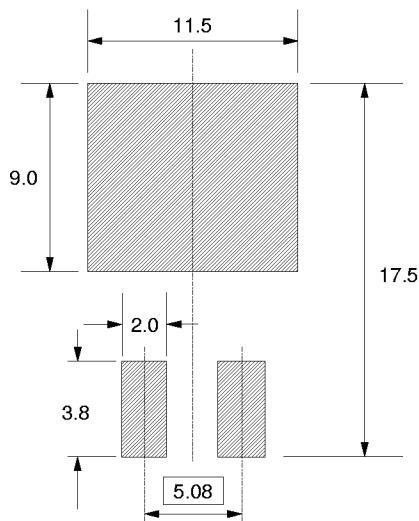


Fig.19. SOT404 : soldering pattern for surface mounting.

#### Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".