

TrenchMOS™ transistor

Standard level FET

BUK78150-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using 'trench' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection. It is intended for use in automotive and general purpose switching applications.

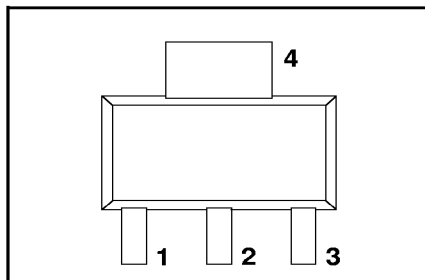
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current	5.5	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 10$ V	150	mΩ

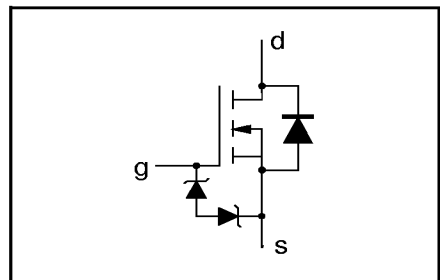
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20$ kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	$T_{sp} = 25$ °C	-	5.5	A
I_D	Drain current (DC)	On PCB in Fig.19	-	2.6	A
I_D	Drain current (DC)	$T_{amb} = 25$ °C	-	1.6	A
I_{DM}	Drain current (pulse peak value)	$T_{amb} = 100$ °C	-	30	A
P_{tot}	Total power dissipation	$T_{sp} = 25$ °C	-	8.3	W
P_{tot}	Total power dissipation	On PCB in Fig.19	-	1.8	W
T_{stg}, T_j	Storage & operating temperature	$T_{amb} = 25$ °C	- 55	150	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

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THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j-amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	70	K/W

STATIC CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$ $T_j = -55^\circ\text{C}$	55 50	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$ $T_j = 150^\circ\text{C}$ $T_j = -55^\circ\text{C}$	2.0 1.2 -	3.0 - -	4.0 - 4.4	V V V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 55\text{ V}; V_{GS} = 0\text{ V};$ $T_j = 150^\circ\text{C}$	-	0.05	10	μA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 10\text{ V}$ $T_j = 150^\circ\text{C}$	-	0.04	1	μA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	$I_G = \pm 1\text{ mA}$ $T_j = 150^\circ\text{C}$	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}$ $T_j = 150^\circ\text{C}$	-	120	150	$\text{m}\Omega$
			-	-	277	$\text{m}\Omega$

DYNAMIC CHARACTERISTICS

 $T_{mb} = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 5\text{ A}; T_j = 25^\circ\text{C}$	0.5	2.5	-	S
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	190	240	pF
C_{oss}	Output capacitance		-	65	80	pF
C_{rss}	Feedback capacitance		-	32	45	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 5\text{ A};$ $V_{GS} = 10\text{ V}; R_G = 10\ \Omega;$	-	9	14	ns
t_r	Turn-on rise time		-	28	42	ns
$t_{d\ off}$	Turn-off delay time		-	15	23	ns
t_f	Turn-off fall time	$T_j = 25^\circ\text{C}$	-	8	12	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

 $T_j = -55$ to 175°C unless otherwise specified

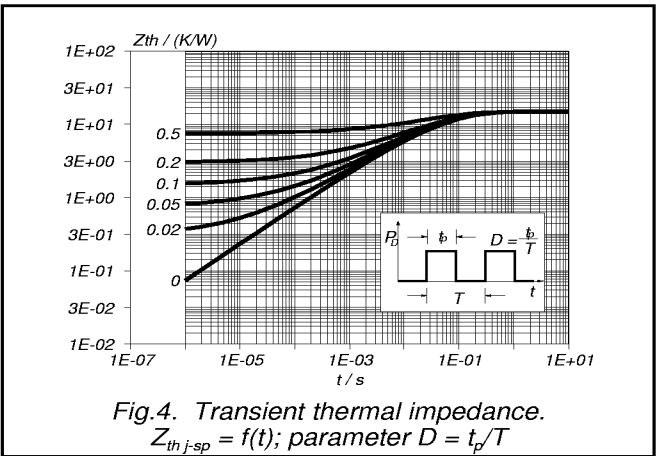
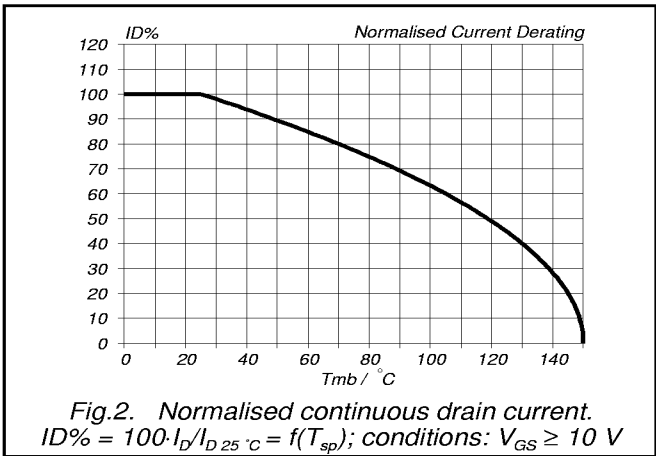
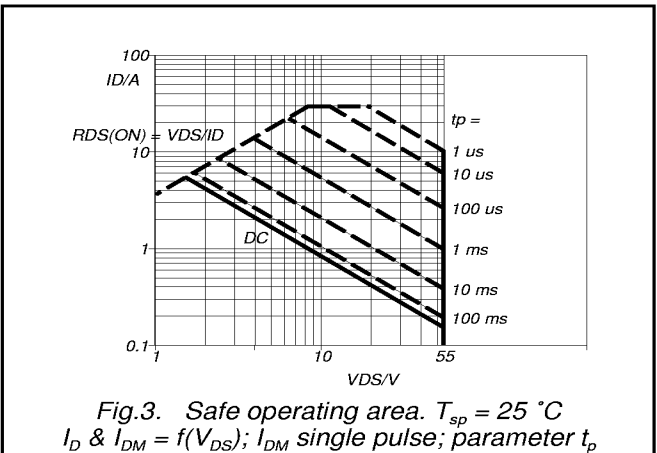
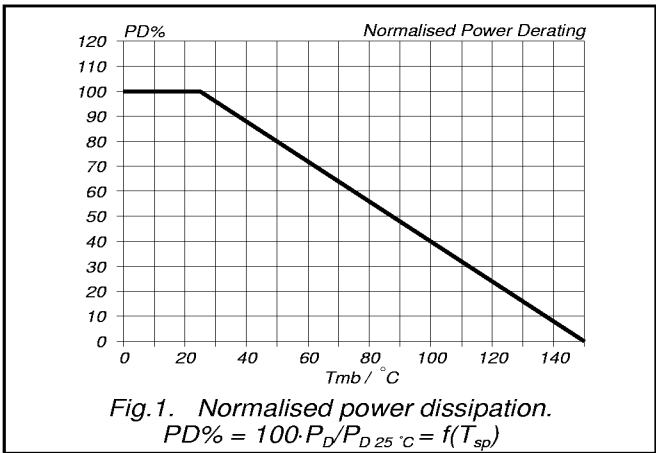
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	$T_{sp} = 25^\circ\text{C}$	-	-	5.5	A
I_{DRM}	Pulsed reverse drain current	$T_{sp} = 25^\circ\text{C}$	-	-	30	A
V_{SD}	Diode forward voltage	$I_F = 2\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	1.1	V
t_{rr}	Reverse recovery time	$I_F = 2\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$ $V_{GS} = -10\text{ V}; V_R = 30\text{ V}$	-	43	-	ns
Q_{rr}	Reverse recovery charge		-	0.16	-	μC

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AVALANCHE LIMITING VALUE

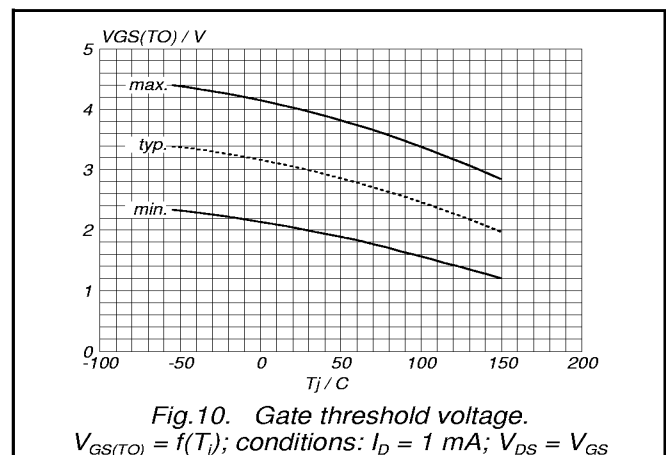
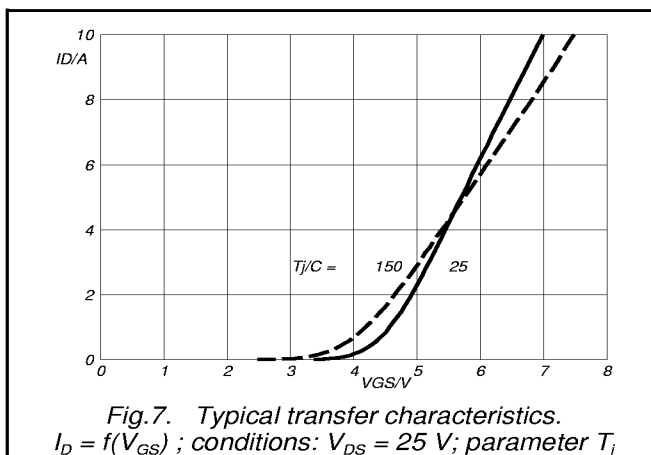
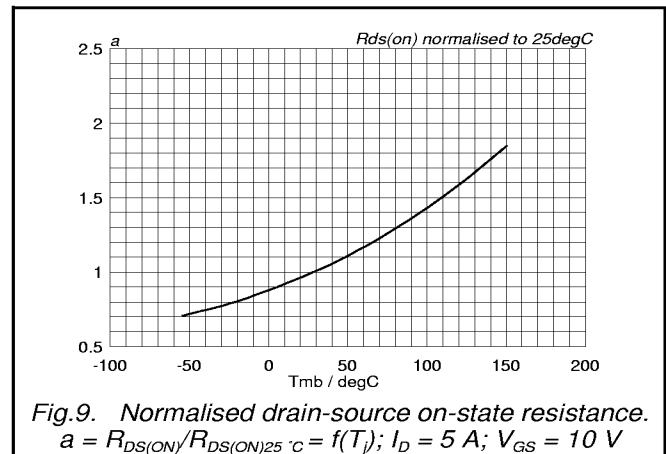
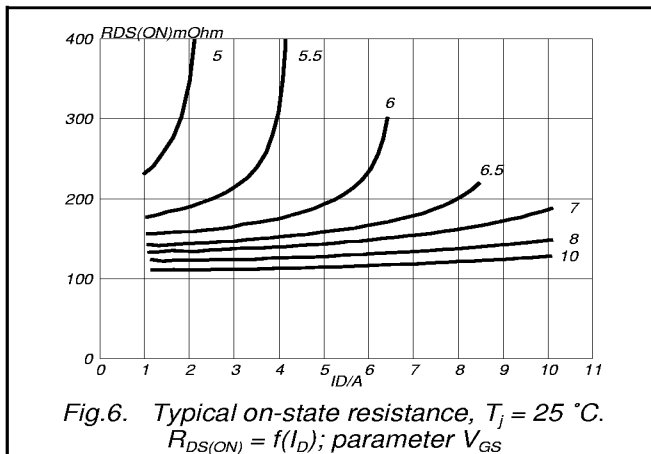
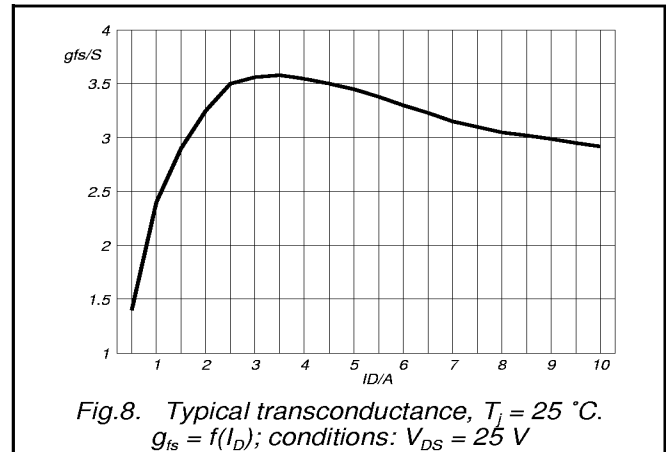
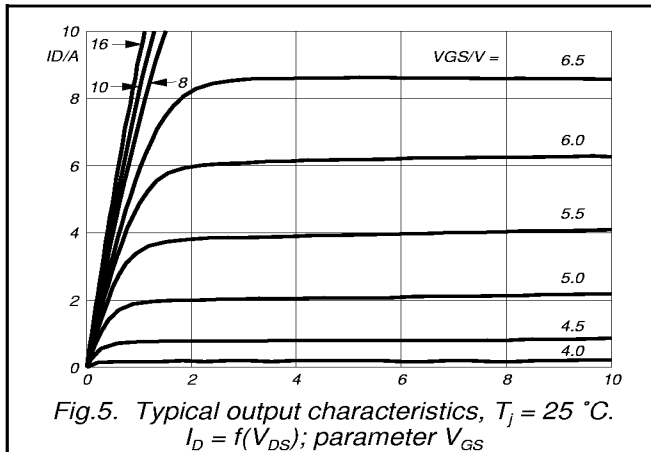
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 1.9\text{ A}$; $V_{DD} \leq 25\text{ V}$; $V_{GS} = 10\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $T_{sp} = 25\text{ }^\circ\text{C}$	-	-	15	mJ



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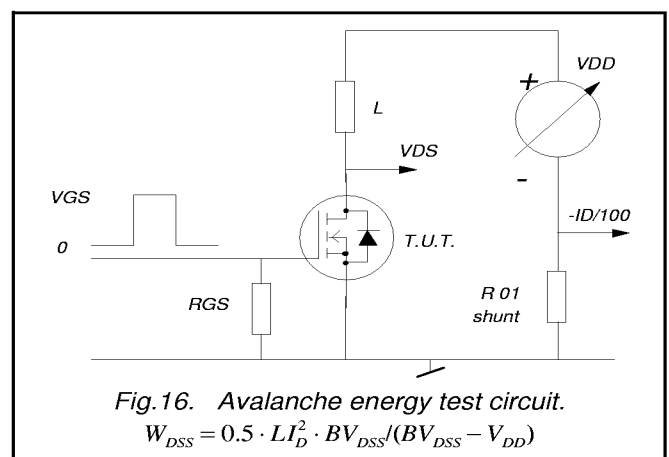
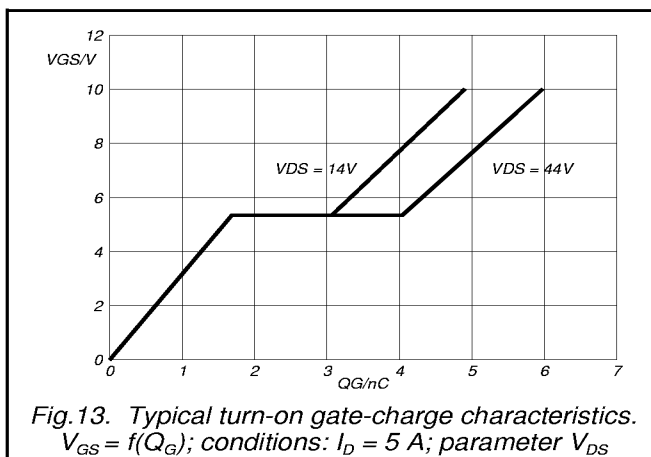
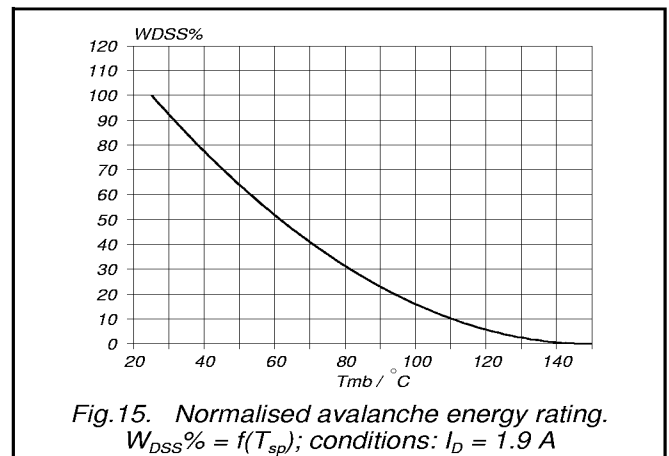
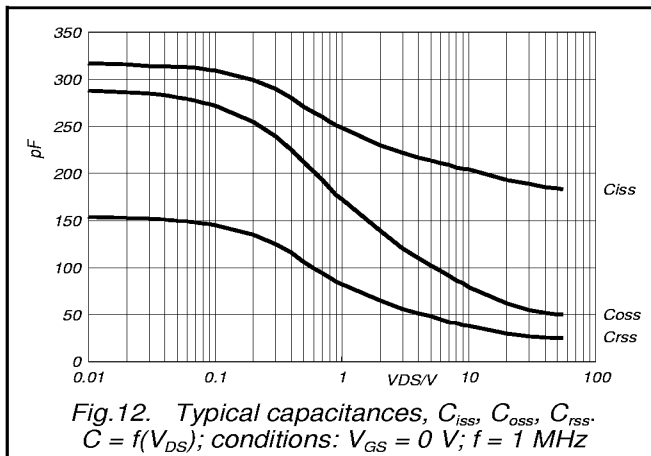
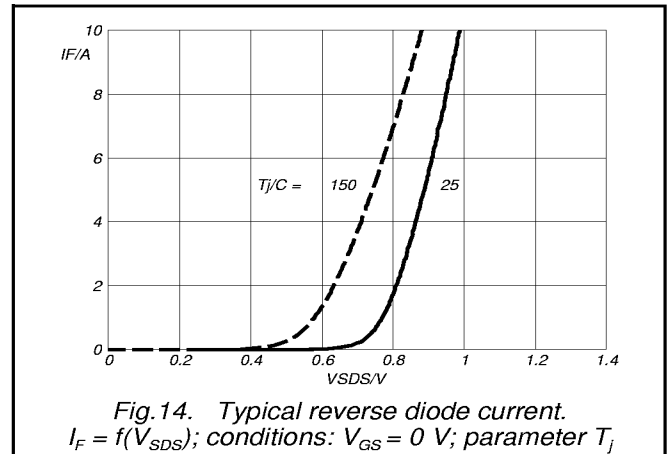
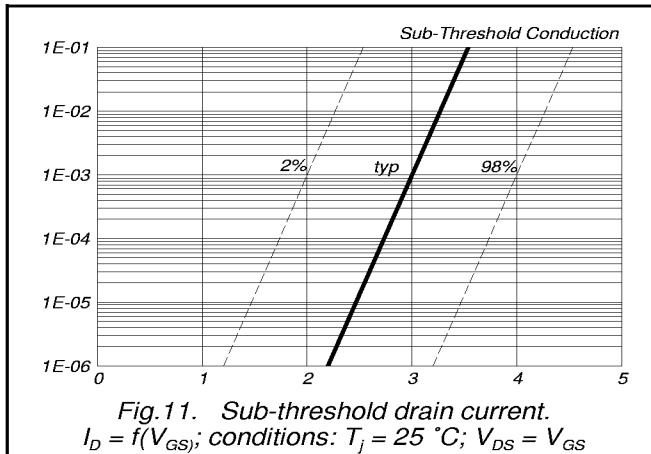
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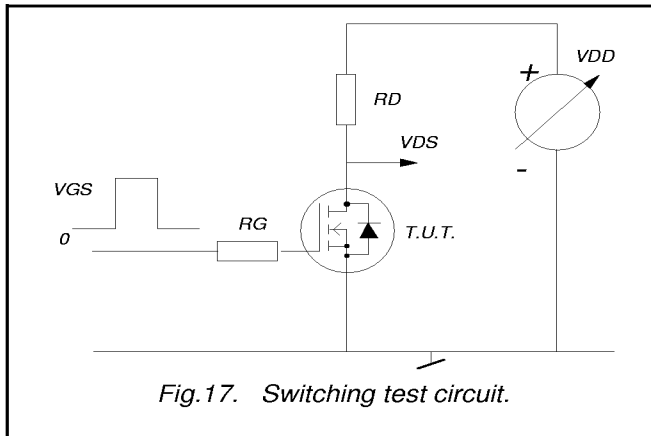
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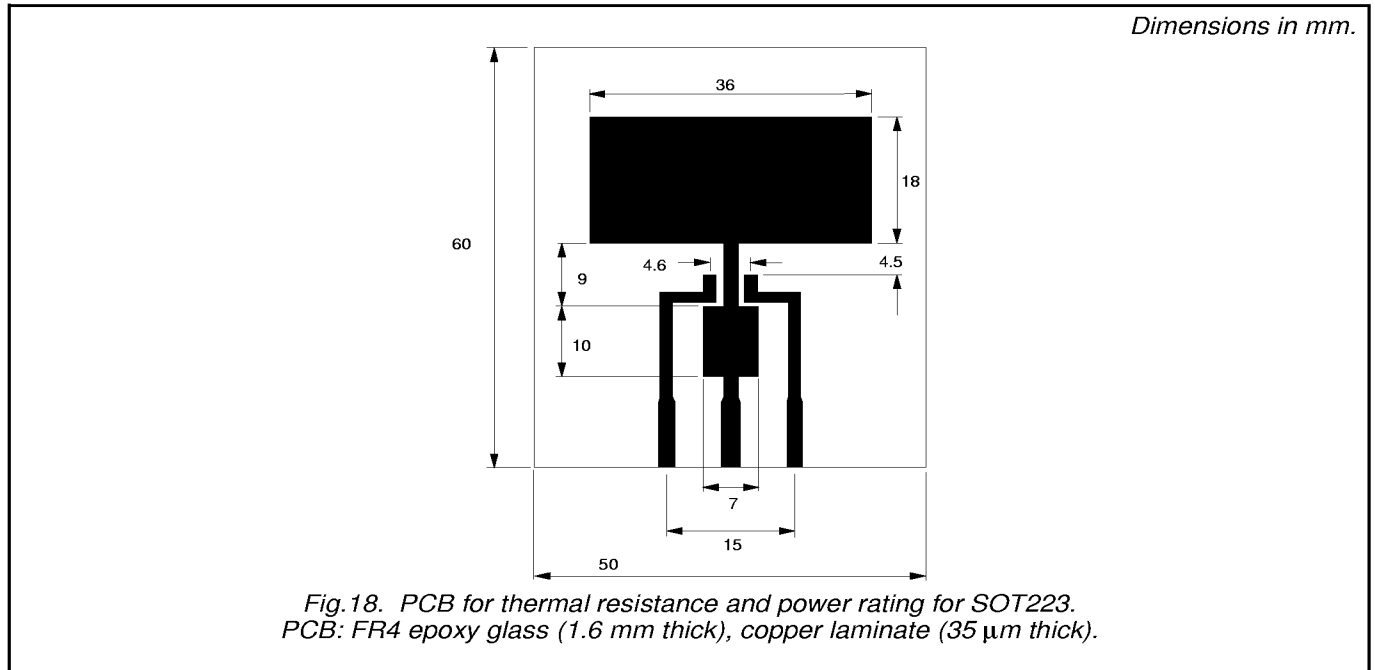
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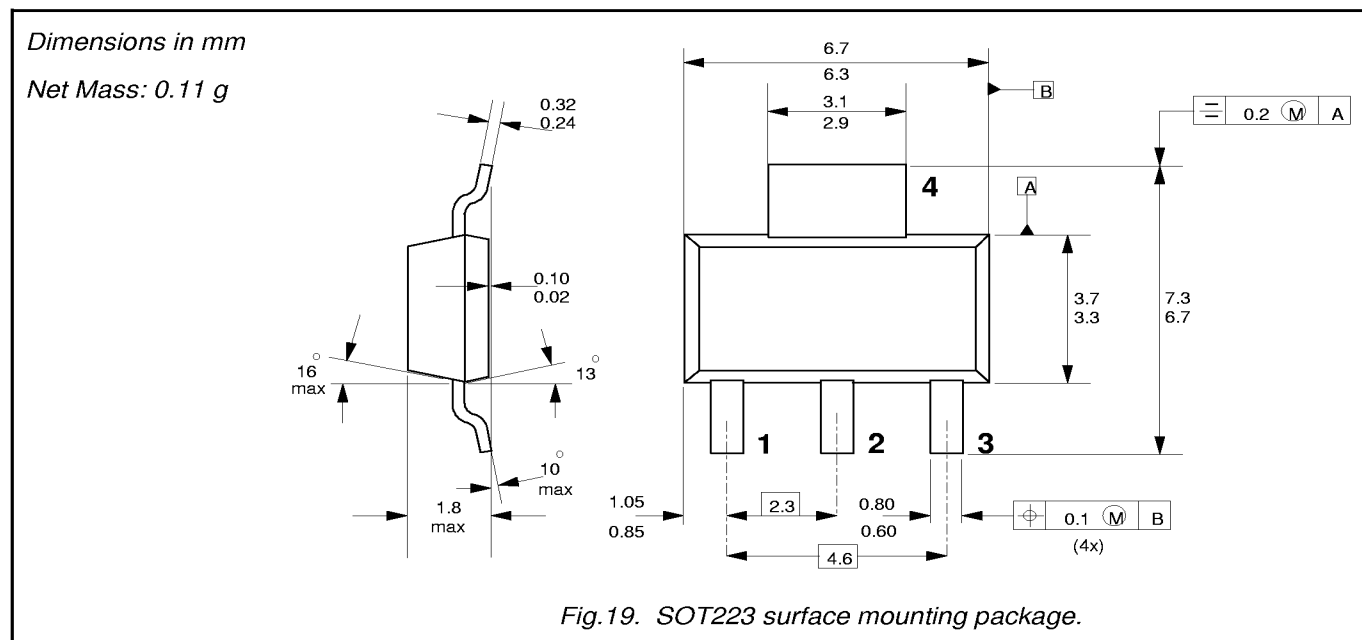
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TrenchMOS™ transistor
Standard level FET**BUK78150-55****PRINTED CIRCUIT BOARD**

TrenchMOS™ transistor
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MECHANICAL DATA



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".