Integrated Device Technology, Inc.

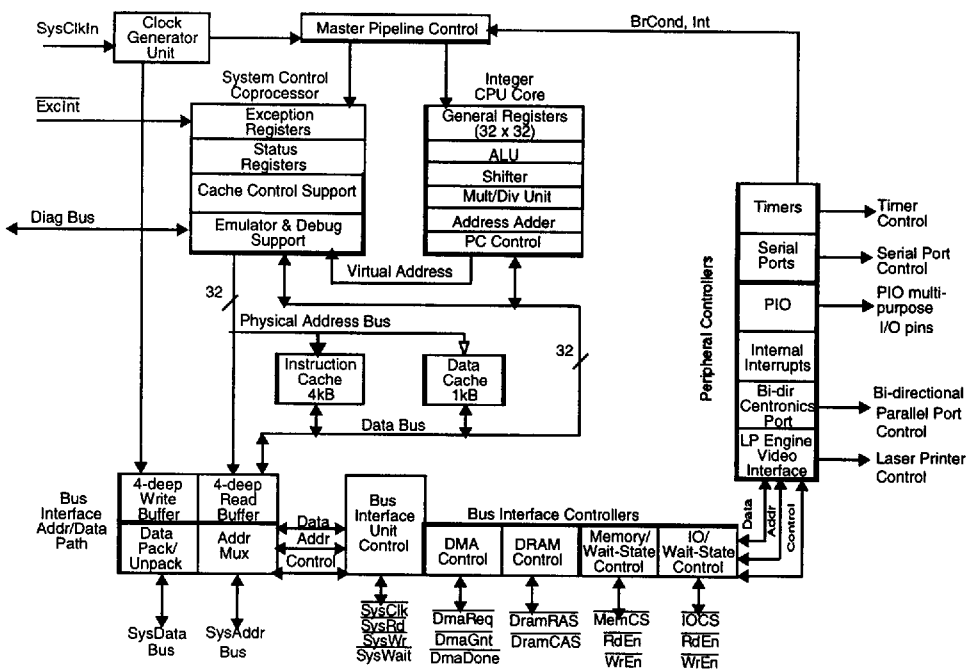
IDT79R36100™ HIGHLY INTEGRATED RISController™

IDT79R36100™ Advanced Information

FEATURES

- Instruction set compatible with the IDT RISController Family MIPS RISC CPUs
- System-level integration minimizes system cost
  - 32-bit RISC CPU
  - 4KB instruction cache on-chip
  - 1KB data cache on-chip
  - Memory, DMA and I/O controllers
  - System peripherals
- 24 MIPS/ 42K Dhrystone-2.1 at 25 MHz
- Improved cache control and cache locking
- Flexible bus interface allows simple, low cost designs
  - De-multiplexed address bus and data bus
  - On-chip 4-deep Read/Write buffer
  - Programmable bus width (8-,16-, and 32-bit)
- On-chip DRAM controller with Address Multiplexer
  - Supports optional interleaved DRAMs
- On-chip memory and I/O controller
  - Chip selects, wait-state generator
  - Supports optional interleaved ROMs
  - Supports PCMCIA Master protocol
- On-chip DMA controller
  - 4 internal channels, 2 external channels
- On-chip bi-directional IEEE 1284 Centronics™ Parallel Port interface
- On-chip laser printer video raster engine interface
- Built-in debug/emulator support
- 3.3V and 5V versions, MQUAD-208 packaging
- Supports interrupt steering to internal DMA
- On-chip dual-channel serial communications controller
- On-chip timers and interrupt controller

BLOCK DIAGRAM



DESCRIPTION

The IDT79R36100 is a highly integrated member of the IDT RISController family. The R36100 implements a "system on a chip" including the CPU core, cache memory, system logic functions and application specific peripherals. The 36100 is well-suited to a wide variety of very cost sensitive and board space constrained embedded applications. The high level of integration also greatly reduces the system design challenge, substantially reducing design risk and time to market.

The R36100 RISController is based upon the general purpose R3000A MIPS RISC CPU core and integrates substantial amounts of on-chip instruction cache and data cache memory. In addition to the CPU core and cache memory, the R36100 integrates all necessary system logic functions on-chip, including DRAM, ROM, I/O and DMA controllers; counter/timers; interrupt controllers; general purpose parallel I/O and debug support circuitry. The R36100 also integrates printer and data communication peripherals including an IEEE 1284 parallel port, laser printer video rasterizer, and two serial communications ports.

The R36100 RISController is software compatible with all members of the IDT RISController family, including the family of low-cost 32-bit R30xx RISControllers and the Orion family of high-performance 64-bit embedded controllers. The common instruction set architecture (ISA) enables the same applications software to be used across a wide variety of price/performance points.

The R36100 RISController has four on-chip bus controllers allowing seamless interfaces with a wide variety of standard memories and peripherals, including:

- Standard page mode DRAMs
- EPROMs, FLASH, SRAM, Dual-Port SRAM
- FIFOs, SCSI, A/D, and other I/O peripherals
- Ethernet, data compression, and other coprocessors

The R36100 RISController integrates an IEEE 1284 parallel port, RS-232C and Local Talk serial ports, and a laser printer video rasterizer to serve printer system applications, including:

- monochrome laser and ink-jet printers
- host-based printer cards
- multi-function laser/fax printer systems

In addition, the R36100 RISController integrates asynchronous and synchronous serial controller channels and multiple timers to serve data communications applications, such as:

- Local Area Network (LAN) interface cards
- CSU/DSU SDLC/HDLC line driver cards
- Router, switcher, and data compression cards

Device Overview

The R36100 RISController shown in the figure on page 1 is a block level representation of the functional units. The R36100 can be viewed as a "system on a chip"—the embodiment of a discrete system built around the R3000A CPU. By integrating the system functionality onto a single chip, dramatic cost, size, and power reductions are achieved. Thus the overall system complexity is reduced and system development time is minimized.

CPU Core

The R36100 RISController is based on the R3000A CPU core. The R3000A is a full 32-bit RISC integer execution engine, capable of sustaining a peak single cycle execution rate by using its five-stage pipeline. The CPU core contains an integer ALU unit and bit shifter with a separate integer multiplier/divider unit, address adder and program counter generator, and 32 orthogonal 32-bit registers. The R36100 execution core implements the MIPS-I instruction set architecture (ISA). Thus, the R36100 is binary compatible with all other MIPS CPU engines, including the low-cost R30xx family and the high-speed R4600 Orion family.

System Control Co-Processor

The R36100 RISController also integrates a System Control Co-processor (CPO) on chip. CP0 manages the exception handling capability of the R36100, the virtual to physical address memory mapping of the R36100, and the various programmable bus-to-cache interface capabilities of the R36100. These topics are discussed in the *Hardware User's Manual.*

The R36100 does not include the optional TLB found in other members of the IDT RISController family, but instead performs the same virtual to physical address mapping of the Base Versions of the R30xx family. These Base Version devices still support distinct kernel and user mode operation, but do not require page management software or an on-chip TLB, leading to a simpler operating system software model and a lower cost processor.

Clock Generator Unit

The R36100 RISController is driven from a single, double frequency input clock. An on-chip clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line that was required in discrete R3000A based systems.

Instruction Cache

The R36100 RISController integrates 4kB of on-chip instruction cache, which is organized with a line size of 16 bytes (four 32-bit entries). This relatively large cache substantially contributes to the high performance inherent in the R36100, and allows systems based on the R36100 to achieve high performance even from low-cost memory systems. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The

cache is implemented using physical addresses and physical tags (rather than virtual addresses or tags), and thus does not require flushing on context switches.

The R36100 instruction cache supports a cache locking mechanism to improve real-time performance. Each cache can be split into two halves or four quarters, each half or quarter servicing a different area of the large address space. This enables the system software to "lock" time-critical code (e.g., router address hash-table lookup algorithms and interrupt service routines), into one of the halves or quarters, and allow other tasks to utilize the other half or quarters without disrupting the locked-time critical code. This technique allows software to perform instruction cache locking, which ensures deterministic response.

Data Cache

The R36100 RISController incorporates an on-chip data cache of 1kB, which is organized as a line size of 4 bytes (one word). This relatively large data cache contributes substantially to the high performance inherent in the R36100. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write through cache to insure that main memory is always consistent and coherent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer that captures address and data at the processor execution rate. This allows the data to be retired to main memory at a much slower rate without impacting the performance of the internal CPU pipeline.

The R36100 supports data cache locking with the same mechanism as the instruction cache. The 36100 allows the data cache to be split into two halves or quarters, each half or quarter servicing a different area of the large address space. This enables the system software to "lock" time-critical data (e.g., routing address information tables and the interrupt stack) into one of the halves or quarters, and allows other tasks to utilize the other half or quarter without disrupting the critical data. This technique allows software to perform data cache locking without requiring memory management support.

Bus Interface Unit

The R36100 RISController uses its large internal caches to provide the majority of its memory bandwidth requirements to/from the execution engine. The execution engine pipeline can access both one instruction and one data load/store per clock cycle. Only on the relatively rare cache miss or on writes does the R36100 require access to main memory. Thus, the R36100 can utilize a simple bus interface that connects to slow memory devices without sacrificing performance.

The R36100 bus interface utilizes a de-multiplexed address and data bus. This interface readily connects to memory subsystems that are 8-, 16-, or 32-bits wide, and/or interleaved.

The R36100 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture the processor's address and data information during internal store operations and process as FIFO at a rate of up to one per clock. The write buffer then presents the bus interface write transactions at the rate the memory system can accommodate.

During main memory writes, the R36100 can break a large datum (e.g. 32-bit word) into a series of smaller transactions (e.g. bytes), according to the width of the memory port being written. This operation is transparent to the software that initiated the store. This insures that the same software can run across multiple platforms having differing memory system configurations.

The R36100 read interface performs both single datum reads and quad word reads. In order to accommodate slower reads, the R36100 incorporates a 4-deep read buffer FIFO, so that the external interface can queue data within the processor before releasing it to perform a burst fill of the internal caches.

In addition, the R36100 can perform on-chip data packing when performing large datum reads (e.g., quad words) from narrower memory systems (e.g., 16-bits). Once again, this operation is transparent to the actual software, which simplifies migration of software to higher performance (true 32-bit) systems, and simplifying field upgrades to wider memory. Since this capability works for either instruction or data reads, the R36100 easily supports the use of 8-, 16-, 32-bit, or interleaved boot PROMs.

Memory Controller

The R36100 RISController uses the on-chip memory controller to gluelessly attach external ROM (including FLASH) and/or SRAM, in a number of system configurations. For example, the memory controller supports interleaved ROM and/or SRAM, 8-bit boot ROM, 32-bit burst ROMs, as well as a simple 32-bit wide EPROM array. The memory controller integrates all of the control signals as well as managing the access timing and wait-state generation for multiple banks, all under the control of boot software.

DRAM Controller

The R36100 RISController integrates an on-chip DRAM controller. The DRAM controller directly controls up to four banks of standard page mode DRAMs in a number of configurations, including systems with varying densities of DRAM, 32-bit wide, interleaved DRAM, and 16-bit wide DRAM subsystems.

I/O Controller

The R36100 RISController has an on-chip I/O controller that performs all necessary address decoding and wait-state generation for external I/O devices. In addition, the on-chip I/O controller readily interfaces as a master to PCMCIA, including support of the large address space required and the PCMCIA chip-select protocol and timing.

DMA Control

The R36100 RISController provides on-chip DMA control for internal peripherals, external peripherals, and external memory. Multiple internal channels allow block moves of data between any combination of memory and I/O. Each channel can also be interrupt controlled, which allows an I/O peripheral like the serial port to regulate the individual transactions of a block move.

The R36100 RISController also supports external DMA masters, which take over the external system bus via a bus request and grant handshake. Once in control of the system bus, the external DMA master can read and write to memory, I/O, and internal peripherals via the R36100's bus controllers.

Counter/Timers

The R36100 RISController contains 3 general purpose timers. Each timer consists of a 16-bit count register as well as a 16-bit compare register. The count register resets to 0 and then counts upward until it equals the compare register. When the count register equals the compare register, the TCN output is asserted and the count is reset back to 0. In order to support intervals longer than 2^{16} ticks, the timers use a common 16-bit prescaler counter. Each timer is programmable to select a power-of-2 divisor of the prescaler. Using these features, each timer can be used as a general purpose real-time clock, bus timeout timer, watch dog timer, PWM/square wave/baud rate generator or gated clock external event counter.

PIO Interface

The R36100 RISController has a Parallel Input/Output (PIO) interface for controlling multi-purpose utility pins. The PIO pins can be programmed to act as general purpose inputs or outputs. Each PIO pin is also multiplexed with other controllers' inputs or outputs. This flexible arrangement allows system designers to customize the R36100 resources according to their needs. Thus, designs needing a special purpose controller--such as the laser printer video controller--can allocate the laser printer video pins for that purpose. Other applications, such as Datacom, which do not need the laser printer video, can use those pins for general purpose inputs or outputs.

Serial Communications Controller

The R36100 RISController integrates a dual channel serial port. This peripheral controller can perform a variety of synchronous and asynchronous protocols, including RS-232C, LocalTalk, SDLC, and HDLC. To maximize throughput, the on-chip serial port is optionally serviced by the auto-initiated on-chip DMA controller which can automatically block move data to and from the port.

Interrupt Controller

The R36100 RISController integrates an on-chip interrupt controller to manage both external interrupts and interrupts signaled from the on-chip peripherals. The interrupt controller improves internal interrupt servicing speed and assists in interrupt prioritization and nesting, as well as interfacing with the auto-initiated DMA.

IEEE 1284 Bi-directional Parallel Port

The R36100 RISController includes an internal IEEE1284 parallel port peripheral, which implements a true bi-directional port. Features include:

- 8-bit input Target Compatible protocol (for backward compatibility with legacy PCs)
- nibble and byte mode output protocol (for backward compatibility with most PCs)
- ECP protocol (for the emerging Laser Printer PC standard)
- EPP protocol (for datacom applications)
- External transceiver interface control pins
- Auto-initiated DMA via internal interrupts

Laser Printer Video Interface

The R36100 RISController integrates an on-chip laser printer video/control interface. This peripheral provides support for the following:

- 1-bit serial stream laser printer or raster engine interface
- On-chip FIFO
- Programmable margin widths and page lengths
- Auto-initiated DMA via internal interrupts

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Performance Overview

The R36100 RISController achieves a very high-level of performance. This performance is due to the following features:

- An efficient execution engine. The CPU performs ALU operations and store operations in a single cycle, has an effective load time of 1.3 cycles and branch execution rate of 1.5 cycles based on the ability of the compilers to avoid software interlocks. Thus, the R36100 achieves over 24 dhrystone MIPS performance at 25MHz.
- Large on-chip caches. The R36100 contains caches that are substantially larger than most embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the R36100 to achieve actual sustained performance that is very close to its peak execution rate, even with low cost memory systems.
- Autonomous multiply and divide operations. The R36100 features an on-chip integer multiplier/divide unit that is separate from the other ALU. This allows the R36100 to perform multiply or divide operations in parallel with other integer operations by using a single multiply or divide instruction rather than "step" operations.
- Integrated write buffer. The R36100 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires them to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- Burst read support. The R36100 enables the system designer to utilize page, static, or nibble mode RAMs when performing read operations. This minimizes the main memory read penalty and increase the effective cache hit rates.
- Tightly coupled memory system. System resources can be accessed and managed efficiently for the needs of the execution core when memory controllers are integrated on-chip.

Selectable Features

Boot-time selectable features are:8/16 or 32-bit PROM support and Big/Little Endian selection. Other selectable, register-configurable features are:

- Number of wait states for different memory and I/O controllers
- Memory and I/O map configuration
- 16 or 32-bit DRAM and 8/16 or 32-bit memory and I/O
- Interleaved or non interleaved memory/DRAM
- Programmable control signals timing for all controllers
- Selectable PIO
- Selectable transceivers type for all controllers (FCT 260/FCT245/FCT543)
- Selectable I/O style (Motorola/Intel/PCMCIA)

Development Support

The R36100 is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis and emulator tools, and sub-system modules.

Figure 1 is an overview of the system development process typically used when developing R36100 applications. The R36100 family is supported in all phases of project development. These tools allow timely, parallel development of hardware and software for R36100 based applications, and include tools such as the following:

- IDT/c compiler, based on the GCC/GNU tool chain.
- Cross development tools, available for a variety of development environments.
- High-performance IDT floating point emulation library software.
- IDT Evaluation Boards, which include RAM, EPROM, I/O, and the IDT PROM Monitor.
- IDT laser printer system boards, which directly drive a low-cost print engine.
- Adobe PostScript Page Description Language running on the IDT R3051 family.
- IDT/sim PROM Monitor, which implements a full PROM monitor, including diagnostics, remote debug support, and peek/poke.
- IDT/kit™ (Kernel Integration Toolkit), which provides library support and a framework for the system run-time environment.
- Logic analyzer and in-circuit emulator support for fast debugging and hardware/software integration.

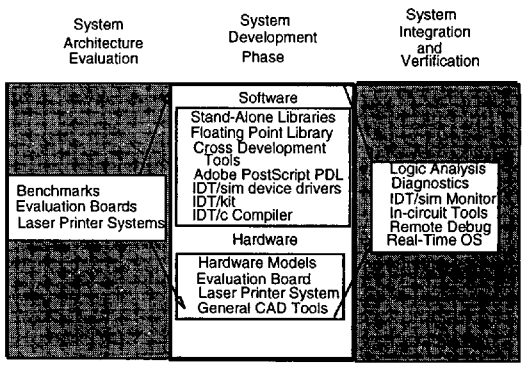

Figure 1. Development Support

System Usage

The IDT R36100 RISController is specifically designed to easily implement low-cost memory systems. Typical low-cost memory systems use EPROMs, DRAMs, as well as application specific peripherals. Some embedded systems also optionally contain or substitute DRAM with static RAMs.

Figure 2 demonstrates the low-system cost inherent in the R36100. In this example system, which is typical of a low-cost laser printer, a 32-bit PROM interface is used due to the size of the PDL interpreter. Other embedded systems could optionally use an 8-bit or a 16-bit PROM, or even an interleaved 64-bit interface. A 16-bit font cartridge interface is provided through PCMCIA for add-in cards and a 32-bit page buffer DRAM is used for high-resolution.

In this example, a field or manufacturing upgrade to a larger page buffer is supported by the boot software and DRAM controller. Such a system features a very low entry price, with a range of field upgrade options. Note that the performance of the R36100 allows software frame buffer compression to be effective in reducing system DRAM while maintaining expected performance.

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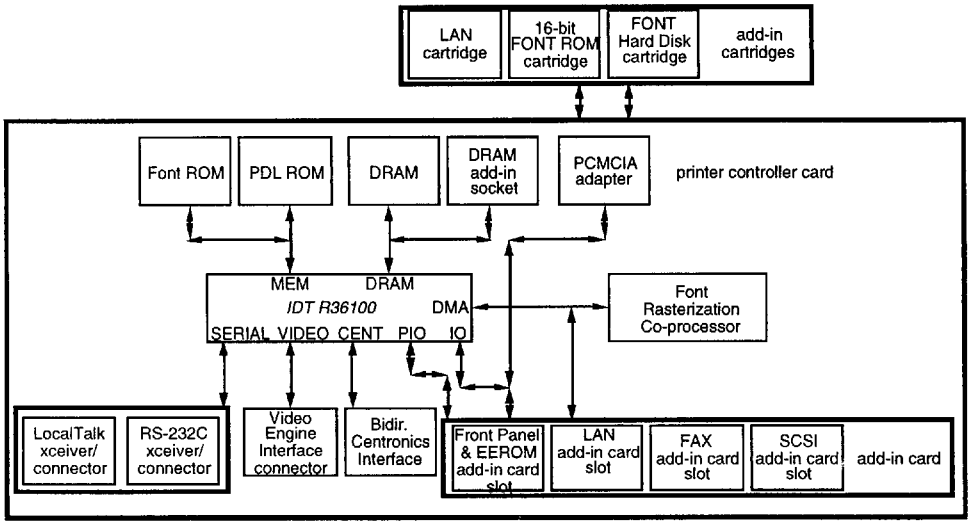

Figure 2. R36100-based Printer System

Pin Description

The following is a list of interface, interrupt, and miscellaneous pins available on the R36100. Pins marked with one asterisk are active when low.

Pin Name	Type	Description
System Bus Interface:		
SysAddr(25:0)	Output	System Address Bus. Also serves as the DramAddr(13:2) Bus.
SysData(31:0)	Input/Output	System Data Bus.
SysClkInInput	Input	System Clock Input. Twice (2x) the internal CPU frequency.
SysClk	Output	System Clock Output. All other outputs are referenced to this system clock.
SysReset	Input	System Reset. Initializes entire chip, except for JTAG circuitry.
SysWait	Input	System Way. Extends current bus transaction.
SysBusError	Input	System Bus Error. Terminates current bus transaction.
SysALEn	Out-put/Input(DMA)	System Address Latch Enable. Indicates valid address at the beginning of a bus transaction.
SysBurstFrame	Out-put/Input(DMA)	System Burst Frame. First indicates the beginning of a bus transaction. Then indicates if the bus transaction is a burst and if the next datum is the last datum.
SysData Rdy	Output	System Data Ready. Indicates valid data during each datum of a bus transaction (except when SysWait is asserted).
SysRd	Out-put/Input(DMA)	System Read. Indicates current bus transaction is a read.
SysWr	Out-put/Input(DMA)	System Write. Indicates current bus transaction is a write.
DRAM Controller Pins		
DramRAS(3:0)	Output	DRAM Row Address Strobe.
DramCAS(3:0)	Output	DRAM Column Address Strobe.
DramRDEnEven	Output	DRAM Read Enable for Even FCT245/543 Type Banks. On FCT260 type banks, it is the read enable for both.
DramRdEnOdd	Output	DRAM Read Enable for Odd FCT245/543 Type Banks. On FCT260 Type Banks, it is the path select.
DramWrEnEven	Output	DRAM Write Enable for Even Banks.
DramWrEnOdd	Output	DRAM Write Enable for Odd Banks.

Pin Name	Type	Description
Memory Controller:		
MemCS/IoCS(7:0)	Output	Memory or I/O Chip Selects. MemCS(0) and optionally MemCS(1) are reserved for the Boot PROM. IoCS(6) and/or IoCS(7) are optionally reserved for the Centronics Port if used.
MemRdEnEven	Output	Memory Read Enable for Even FCT245/543 Type Banks. On FCT260 Type banks, it is the read enable for both even and odd banks.
MemRdEnOdd	Output	Memory Read Enable for Even FCT245/543 Type Banks. On FCT260 Type Banks, it is the path select.
MemWrEn(3:0)	Output	Memory Write Enable for each byte lane.
IoRdEn/DStrobe	Output	I/O Read Enable or I/O Data Strobe.
IoWrEn/RdWr	Output	I/O Write Enable or I/O Read/Write.
DMA Controller:		
DmaBusGnt(1:0)	Output	DMA Bus Grant Indicates that the CPU has tri-stated the bus and other DMA related signals.
DmaBusReq(1:0)	Input	DMA Bus Request. Indicates that external DMA agent would like control of the bus and other DMA related signals.
DmaDone	Input/Output	DMA transaction done
Serial Port Pins:		
SerialPClkIn(1:0)	Input	Optional Prim ary Serial Clock Input.
SerialSClk(1:0)	Input/Output	Optional Secondary Serial Clock Input or Output.
SerialRxData(1:0)	Input	Serial Receiver Data Stream.
SerialTxData(1:0)	Output	Serial Transmitter Data Stream.
SerialCTS(1:0)	Input	Serial Clear To Send.
SerialRTS(1:0)	Output	Serial Request To Send.
Serial Sync(1:0)	Input/Output	Serial Frame Sync.
Serial DCD(1:0)	Input	Serial Data Carrier Detect.
SerialDTR(1:0)	Output	Serial Data Terminal Ready.
Timer:		
TimerTC(2:0) /TimerGate(2:0)	Input/Output	Timer Terminal count output or Timer Count Gate Enable input. Terminal count asserts when Timer Count equals 0. Timer Gate enables counter to count upward or to stop.
PIO:		
PIO(31:0)	Input/Output	Parallel inputs or Parallel Outputs. Parallel inputs and parallel outputs are multiplexed with various peripheral inputs and peripheral outputs. If the peripheral is unused, the input or output pin can be reconfigured to be a general purpose input or output, respectively.

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Pin Name	Type	Description
Bi-Directional Centronics Interface:		
CentStrobe	Input	Centronics Strobe. In compatible mode, strobes data into the printer. Has other uses for other modes.
CentAck	Output	Centronics Acknowledge. In compatible mode, acknowledges a strobe. Has other uses for other modes.
CentBusy	Output	Centronics Busy. In compatible mode, delays the host from sending more data. Has other uses for other modes.
CentPaperError	Output	Centronics Paper Out/Jam Error. In Compatible mode, indicates that the printer has a paper error when asserted with CentFault. Has other uses for other modes.
CentSelect	Output	Centronics Select. In Compatible mode, used to indicate that this printer is on-line. Has other uses for other modes.
CentAutoFeed	Input	Centronics Auto Page Feed. In compatible mode, sends a paper feed to the printer. Has other uses for other modes.
CentInit	Input	Centronics Initialization/Reset. In Compatible mode, resets the printer. Has other uses for other modes.
CentFault	Output	Centronics Fault. In Compatible mode, indicates that the printer has a problem. Has other uses for other modes.
CentSelectIn	Input	Centronics Select In. In Compatible mode, indicates that the Host wants to select this printer on a shared cable. Has other uses for other modes
CentHostStrobe	Output	Centronics Host Strobe. Used to latch Host data on the external FCT952/374 data transceiver during a Host write.
CentHostOEn	Output	Centronics Host Output Enable. Used to enable the external FCT952/374 data transceiver during a Host read.
Laser Engine Interface:		
LaserVideoData	Output	Laser Video Data Stream.
LaserVideoClkIn	Input	Laser Video Clock Input. Accepts either the (1x) Video Data Stream frequency or 8 times (8x) the PLL frequency.
LaserLineSync	Input	Laser Line Sync. Indicates that the laser drum is ready to start accepting data for a new line.
LaserPageSync	Input	Laser Page Sync. Indicates that the laser drum is ready to start a new page.
Debug/Emulator Interface:		
JtagClkIn	Input	JTAG Clock Input (TCK). Test mode serial boundary scan input clock.

Pin Name	Type	Description
Debug/Emulator Interface:		
JtagModeSelect	Input	JTAG Mode Select (TSEL). Test mode serial boundary scan command data. In normal operating mode, JtagModeSelect should be left unasserted high.
JtagDataIn	Input	JTAG Data In (TDI). Test mode serial boundary scan register data input.
JtagDataOut	Output	JTAG Data Out (TDO). Test mode serial boundary scan register data output.
JtagReset	Input	TAG Reset (TRES*). Resets the JTAG test circuitry. Does not reset any other chip functions.In normal operating mode, JtagReset should be left asserted low.
Diagnostic Pins		
DiagC/UnC	Output	Diagnostic Cached versus Uncached. On read bus transactions indicates whether the read is cached or uncached.
DiagInst/Data	Output	Diagnostic Instruction versus Data. On read bus transactions indicates whether the read is for instructions or data.
DiagRun	Output	Diagnostic Run. Indicates an internal pipeline run cycle. This pin has iso-synchronous timing.
DiagBranchTaken	Output	DiagBranchTaken Indicates that a branch, jump, or exception has been taken. This pin has asynchronous timing.
DiagJRorExe	Output	Diagnostic Jump Register or Exception occurring. Indicates that a jump register or exception is executing. This pin has asynchronous timing.
DiagInternalWr	Output	Diagnostic Internal Write. Indicates that a MTCO to CP0 register $3 is occurring.
DiagInstCacheWrDis	Output	Diagnostic Cache Write Disable. Disables writes to the instruction and data cache. This pin has iso-synchronous timing and is not recommended for functional use.
DiagTriState	Input	Diagnostic Tri-State all outputs. All outputs are tri-stated including SysClk. This pin is asynchronous such that tri-stating asserts or de-asserts output enables immediately.
DiagFCM	Input	Diagnostic Force Cache Miss. This pin has iso-synchronous timing. If used for functional board tests, it is recommended that it be (de-)asserted statically at reset time and left (de-)asserted.
DiagIntDis	Input	Diagnostic Interrupt Disable.
DiagNoCS	Output	Diagnostic No Chip Select. No internal or external chip select has occurred for the current bus transaction, therefore an external state machine should handle the bus transaction.
DiagInternalDMA	Output	Diagnostic Internal DMA. Asserts whenever any of the Internal DMA channels is generating the current bus transaction.

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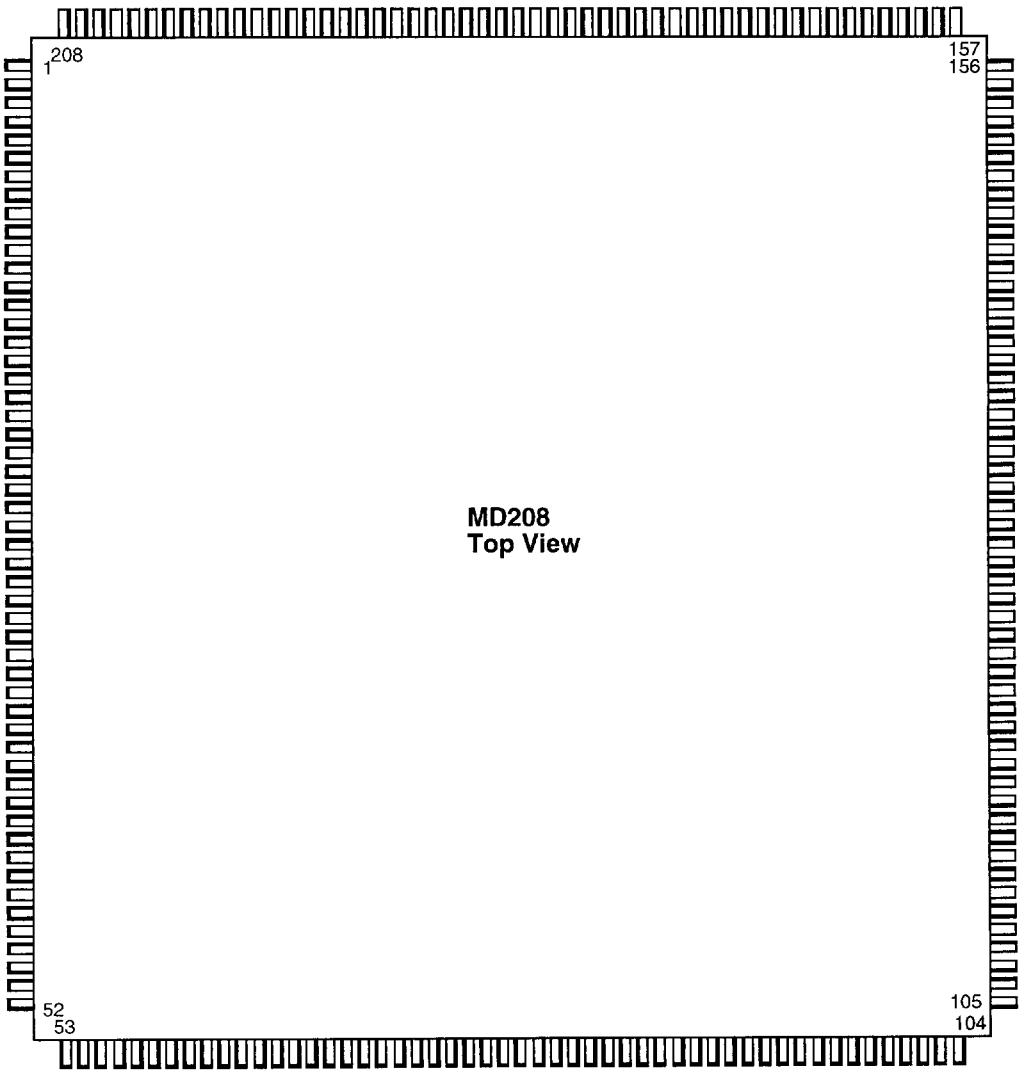
Pin Name	Type	Description
Exception Handling:		
ExcSInt(2:0)	Input	Exception Synchronized Interrupts. Also used as the reset initialization vector for 2:Boot16, 1:Boot8, and 0:BigEndian modes.
ExcInt(4:3)	Input	Exception Interrupts.
ExcSBrCond(3:2)	Input	Exception Synchronized Branch Condition inputs.
Power/Ground:		
Vcc	Input	Power pin. All power pins must be connected. 5V or 3.3V depending on part type.
Gnd	Input	Ground pin (VSS). All ground pins must be connected. 0V.

Physical Specifications



MD208
Top View

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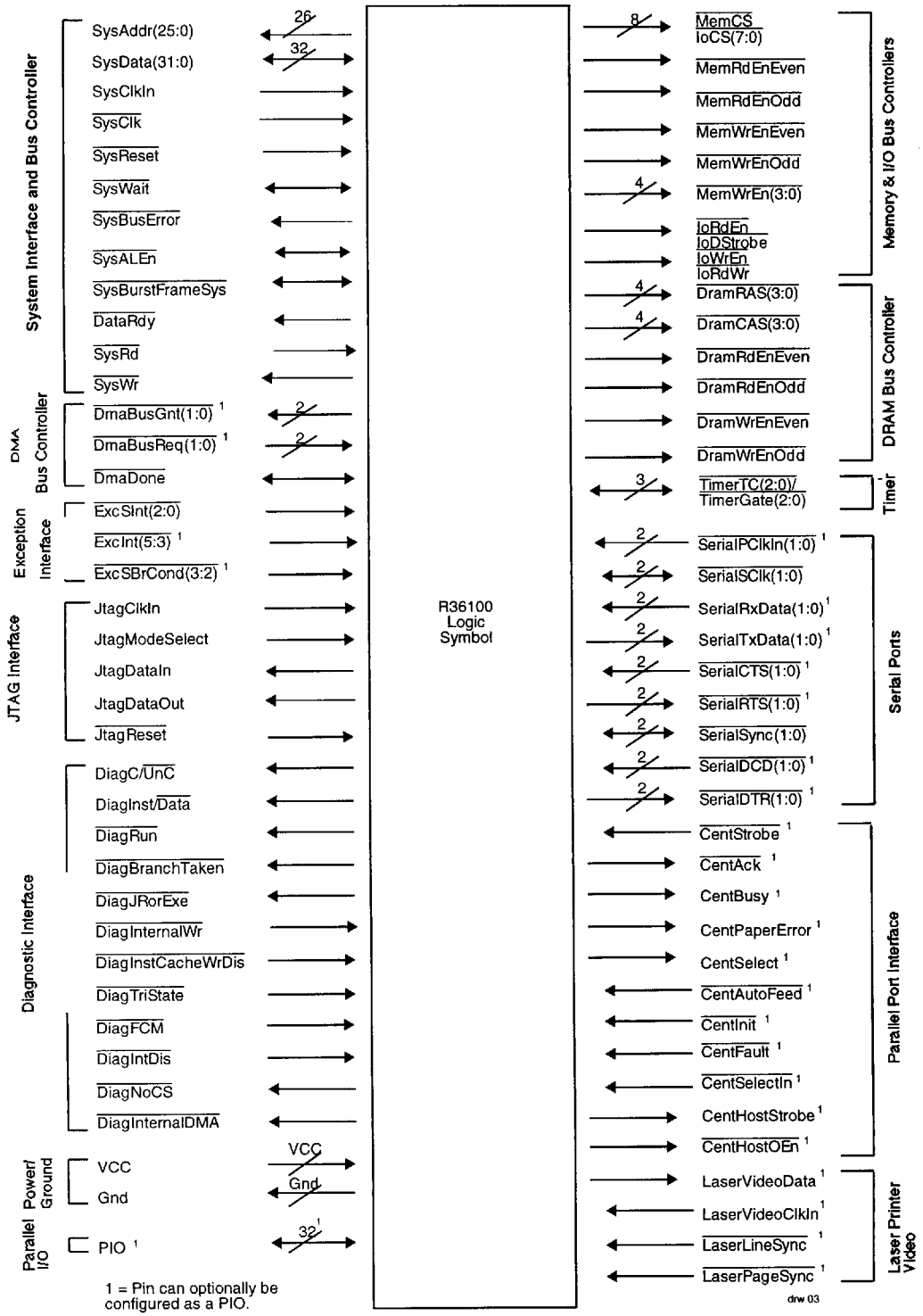
36100 Advance Pin-Out

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	Test1N	53	JtagDataOut	105	N/C	157	SerialTxData(0)
2	SysAddr(0)	54	SysData(0)	106	DramRASN(2)	158	SerialCTSN(0)
3	SysAddr(1)	55	SysData(1)	107	DramRASN(3)	159	SerialRTSN(0)
4	DiagC_UnCN	56	SysData(2)	108	DramCASN(0)	160	SerialTxClkN(0)
5	SysAddr(2)	57	SysData(3)	109	DramCASN(1)	161	SerialSycnN(0)
6	vcc	58	vcc	110	vcc	162	vcc
7	vss	59	vss	111	vss	163	vss
8	SysAddr(3)	60	SysData(4)	112	DramCASN(2)	164	SerialDTRN(0)
9	SysAddr(4)	61	SysData(5)	113	DramCASN(3)	165	SerialDCDN(0)
10	DiagRunN	62	SysData(6)	114	DramRdEnEvenN	166	SerialClkInN(1)
11	DiagBranchTakenN	63	SysData(7)	115	DramRdEnOddN_TrN	167	SerialTxClkN(1)
12	DiagJRorExeN	64	SysData(8)	116	MemCSN_IoCSN(0)	168	SerialSyncN(1)
13	DiagInternalWrN	65	SysData(9)	117	MemCSN_IoCSN(1)	169	SerialRxData(1)
14	SysAddr(5)	66	SysData(10)	118	MemCSN_IoCSN(2)	170	SerialTxData(1)
15	SysAddr(6)	67	SysData(11)	119	MemCSN_IoCSN(3)	171	SerialCTSN(1)
16	vcc	68	vcc	120	vcc	172	vcc
17	vss	69	vss	121	vss	173	vss
18	SysAddr(7)	70	SysData(12)	122	MemCSN_IoCSN(4)	174	SerialRTSN(1)
19	SysAddr(8)	71	SysData(13)	123	MemCSN_IoCSN(5)	175	SerialDCDN(1)
20	DiagInst-CacheWrDisN	72	SysData(14)	124	MemCSN_IoCSN(6)	176	SerialDTRN(1)
21	DiagTriStateN	73	SysData(15)	125	MemCSN_IoCSN(7)	177	TimerTCN(0)
22	DiagFCMN	74	SysData(16)	126	MemRdEnEvenN	178	TimerTCN(1)
23	DiagIntDisN	75	SysData(17)	127	MemRdEnOddN	179	TimerTCN(2)
24	SysAddr(9)	76	SysData(18)	128	MemWrEnN(0)	180	CentStrobeN
25	SysAddr(10)	77	SysData(19)	129	MemWrEnN(1)	181	CentAckN
26	vcc	78	vcc	130	vcc	182	vcc
27	vss	79	vss	131	vss	183	vss
28	SysAddr(11)	80	SysData(20)	132	MemWrEnN(2)	184	CentBusy
29	SysAddr(12)	81	SysData(21)	133	MemWrEnN(3)	185	CentPaperError
30	DiagNoCSN	82	SysData(22)	134	IoRdEnN_DStrobeN	186	CentSelect
31	Diaginst_DataN	83	SysData(23)	135	IoWrEnN_RdWrN	187	CentAutoFeedN
32	SysAddr(13)	84	SysData(24)	136	N/C	188	CentInitN
33	SysAddr(14)	85	SysData(25)	137	N/C	189	CentFaultN
34	SysAddr(15)	86	SysData(26)	138	LaserVideoData	190	CentSelectInN
35	SysAddr(16)	87	SysData(27)	139	LaserVideoClk	191	CentHostStrobeN
36	vcc	88	vcc	140	vcc	192	vcc
37	vss	89	vss	141	vss	193	vss
38	SysAddr(17)	90	SysData(28)	142	LaserLineSyncN	194	CentHostOEnN
39	SysAddr(18)	91	SysData(29)	143	LaserPageSyncN	195	DmaBusGntN(0)
40	SysAddr(19)	92	SysData(30)	144	ExcSintN(0)	196	DmaBusGntN(1)
41	SysAddr(20)	93	SysData(31)	145	ExcSintN(1)	197	DmaBusReqN(0)
42	SysAddr(21)	94	SysClkIn	146	ExcSintN(2)	198	DmaBusReqN(1)
43	SysAddr(22)	95	SysResetN	147	ExcIntN(3)	199	DmaDoneN
44	SysAddr(23)	96	DramWrEvenN	148	ExcIntN(4)	200	SysAleN
45	SysAddr(24)	97	N/C	149	DiagIntDmaN	201	SysDataRdyN
46	vcc	98	vcc	150	vcc	202	vcc
47	vss	99	vss	151	vss	203	vss
48	SysAddr(25)	100	DramWrOddN	152	SysWaitN	204	SysRdN
49	JtagModeSelect	101	N/C	153	SysBusErrorN	205	SysWrN
50	JtagResetN	102	DramRASN(0)	154	SysClkN	206	SysBurstFrameN
51	JtagClkIn	103	DramRASN(1)	155	SerialClkInN(0)	207	ExcSBrCond(2)
52	JtagDataIn	104	Test0N	156	SerialRxData(0)	208	ExcSBrCond(3)



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