SUN MICROELECTRONICS

STP4020QFP

July 1997

PCMCIA

DATA SHEET — Controller Interface

DESCRIPTION

The STP4020 PCMCIA controller bridges the SBus standard in SPARC microprocessor-based systems, to the PCMCIA Card Standard Interface. PCMCIA compatible peripheral cards provide a standard interface and form factor for mass storage and input/output capabilities.

The STP4020 contains a fully-compliant IEEE P1496-1993 SBus slave interface. It supplies a direct interface to the PCMCIA standard for Type I, Type II, and Type III devices. The STP4020 supports up to two PCMCIA Cards in a single SBus slot.

Features

- Single chip design provides direct connect, fully compliant SBus slave interface
- SBus Interface supports optional FCode PROM
- Fully compliant PCMCIA Card Standard Interface (Release 2.01)
- Supports two 68-pin Standard PCMCIA Cards
- Supports Type I, Type II, and Type III PCMCIA peripherals
- Programmable access timing to support various types of PCMCIA Memory Cards
- Interrupt support for card insertion/removal, battery failure, and I/O Card Interrupt
- Power Control for V_{CC}, V_{PP1}, and V_{PP2} to each of the PCMCIA Cards
- 8.33 Mbyte/sec maximum data bandwidth
- IEEE P1149 JTAG Standard for internal and boundary scan
- 208-pin Plastic Quad Flat Pack (PQFP)

Benefits

- Ease of design and reliability
- Ease of system configuration
- Interfaces to Industry Standard devices
- Flexibility
- Maximum utilization of available memory and I/O devices
- Flexibility to support numerous PCMCIA peripherals
- Flexibility, reliability, and ease of use for non-technical users
- Intelligent PCMCIA card management
- High bandwidth data flow
- Improved chip and board level testability
- Low cost packaging

BLOCK, LOGIC, AND APPLICATION DIAGRAMS

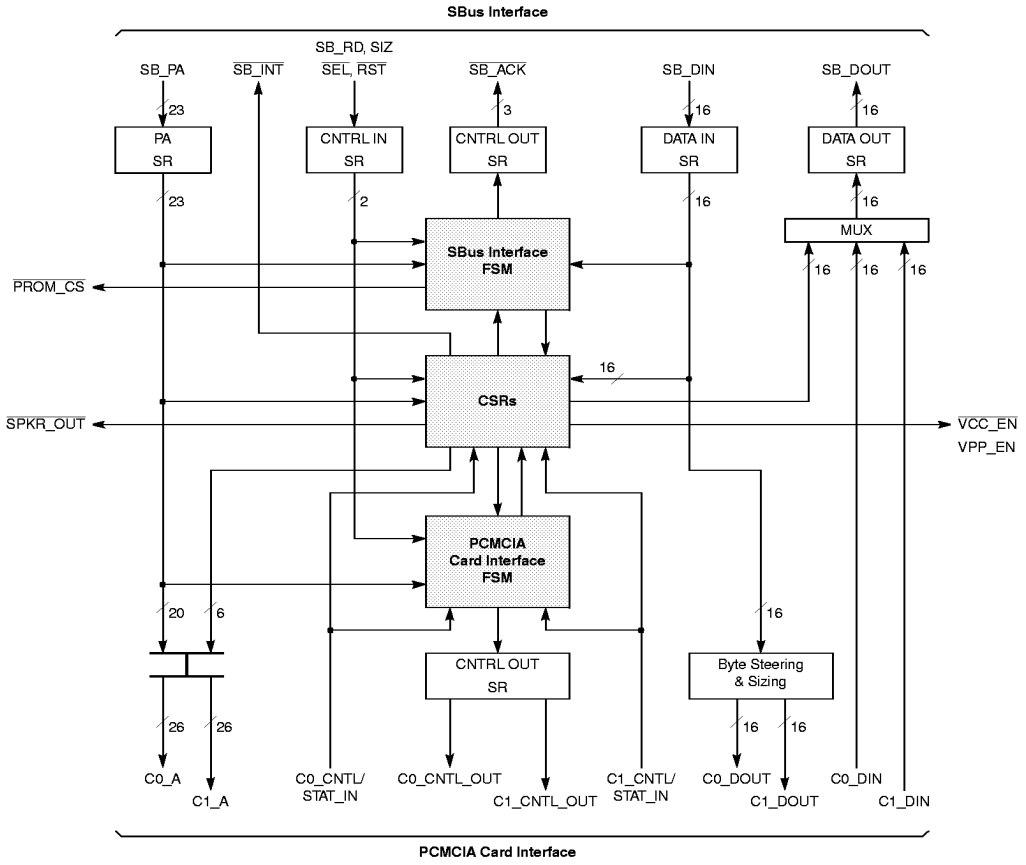


Figure 1. STP4020 Block Diagram

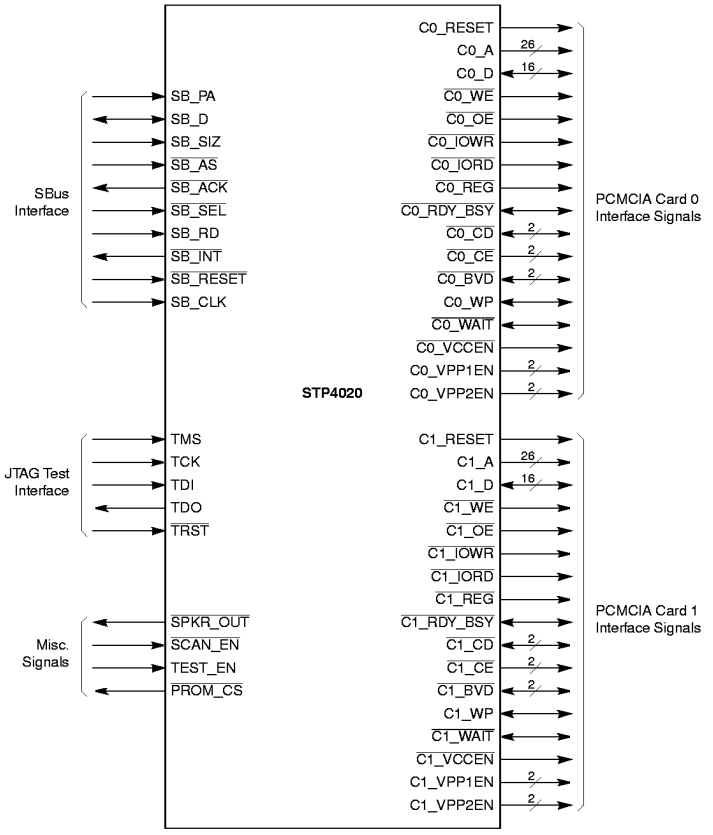


Figure 2. STP4020 Logical Connections

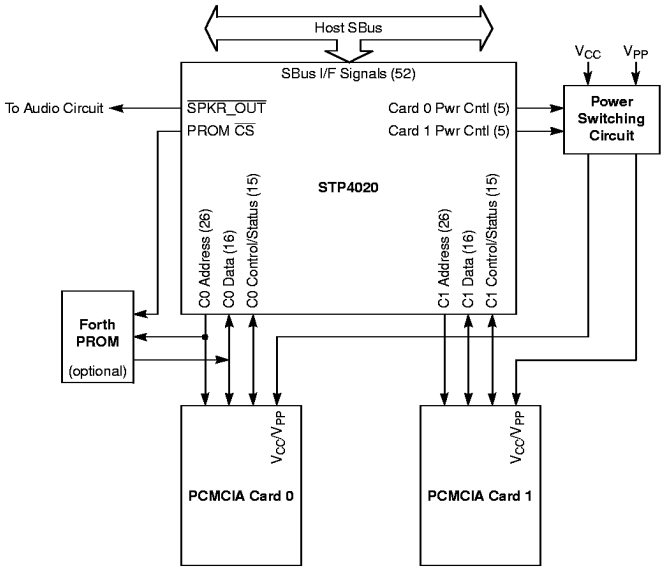


Figure 3. Typical STP4020 Application Diagram

SIGNAL DESCRIPTIONS

SBus Interface Signals

Signal	Type	Description
SB_PA [22:0]	Input	SBus Physical Address
SB_D [31:16]	I/O	SBus Data
SB_SIZE [2:0]	Input	SBus Transfer Size
$\overline{\text{SB\_AS}}$	Input	SBus Address Strobe
$\overline{\text{SB\_ACK}}$ [2:0]	Output	SBus Transfer Acknowledge
$\overline{\text{SB\_SEL}}$	Input	SBus Slave Select
$\overline{\text{SB\_INT}}$ [1:0]	Output	SBus Interrupt Request
$\overline{\text{SB\_RESET}}$	Input	SBus Reset
SB_CLK	Input	SBus Clock
SB_RD	Input	SBus Transfer Direction

JTAG Test Interface Signals

Signal	Type	Description
TMS	Input	JTAG Test Mode Select
TCK	Input	JTAG Test Clock
TDI	Input	JTAG Test Data In
TDO	Output	JTAG Test Data Out
TRST	Input	JTAG Test Reset

Miscellaneous Signals

Signal	Type	Description
$\overline{\text{SPKR\_OUT}}$	Output	Audio Out
$\overline{\text{SCAN\_EN}}$	Input	Internal Scan Enable
TEST_EN	Input	Test Enable
$\overline{\text{PROM\_CS}}$	Output	PROM Chip Select

PC Card 0 Interface Signals

Signal	Type	Description
$\overline{\text{C0\_RDY\_BSY}}$	I/O	PCMCIA Card 0 Ready/Busy
$\overline{\text{C0\_CD}}$ [2]	I/O	PCMCIA Card 0 Card Detect 2
$\overline{\text{C0\_CD}}$ [1]	I/O	PCMCIA Card 0 Card Detect 1
$\overline{\text{C0\_CE}}$ [2:1]	Output	PCMCIA Card 0 Card Enables

PC Card 0 Interface Signals (Continued)

Signal	Type	Description
$\overline{\text{C0\_BVD}}$ [2:1]	I/O	PCMCIA Card 0 Battery Voltage Detects
$\overline{\text{C0\_WAIT}}$	I/O	PCMCIA Card 0 Extend Bus Cycle
C0_RESET	Output	PCMCIA Card 0 Reset
C0_WP	I/O	PCMCIA Card 0 Write Protect
$\overline{\text{C0\_VCCEN}}$	Output	PCMCIA Card 0 V_{CC} Enable
C0_VPP1EN [1:0]	Output	PCMCIA Card 0 V_{PP1} Enables
C0_VPP2EN [1:0]	Output	PCMCIA Card 0 V_{PP2} Enables
C0_A [25:0]	Output	PCMCIA Card 0 Address
C0_D [15:0]	I/O	PCMCIA Card 0 Data
$\overline{\text{C0\_WE}}$	Output	PCMCIA Card 0 Write Enable
$\overline{\text{C0\_OE}}$	Output	PCMCIA Card 0 Output Enable
$\overline{\text{C0\_IOWR}}$	Output	PCMCIA Card 0 IO Write
$\overline{\text{C0\_IORD}}$	Output	PCMCIA Card 0 I/O Read
$\overline{\text{C0\_REG}}$	Output	PCMCIA Card 0 Attribute Memory Select

PC Card 1 Interface Signals

Signal	Type	Description
$\overline{\text{C1\_RDY\_BSY}}$	I/O	PCMCIA Card 1 Ready/Busy
$\overline{\text{C1\_CD}}$ [2]	I/O	PCMCIA Card 1 Card Detect 2
$\overline{\text{C1\_CD}}$ [1]	I/O	PCMCIA Card 1 Card Detect 1
$\overline{\text{C1\_CE}}$ [2:1]	Output	PCMCIA Card 1 Card Enables
$\overline{\text{C1\_BVD}}$ [2:1]	I/O	PCMCIA Card 1 Battery Voltage Detects
$\overline{\text{C1\_WAIT}}$	I/O	PCMCIA Card 1 Extend Bus Cycle
C1_RESET	Output	PCMCIA Card 1 Reset
C1_WP	I/O	PCMCIA Card 1 Write Protect
$\overline{\text{C1\_VCCEN}}$	Output	PCMCIA Card 1 V_{CC} Enable
C1_VPP1EN [1:0]	Output	PCMCIA Card 1 V_{PP1} Enables
C1_VPP2EN [1:0]	Output	PCMCIA Card 1 V_{PP2} Enables
C1_A [25:0]	Output	PCMCIA Card 1 Address
C1_D [15:0]	I/O	PCMCIA Card 1 Data
$\overline{\text{C1\_WE}}$	Output	PCMCIA Card 1 Write Enable
$\overline{\text{C1\_OE}}$	Output	PCMCIA Card 1 Output Enable
$\overline{\text{C1\_IOWR}}$	Output	PCMCIA Card 1 IO Write
$\overline{\text{C1\_IORD}}$	Output	PCMCIA Card 1 I/O Read
$\overline{\text{C1\_REG}}$	Output	PCMCIA Card 1 Attribute Memory Select

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Symbol	Name	Rating	Units
V_{CC}	Power supply voltage	+7.0	V
V_{IN}	Input voltage (any pin)	GND ð V_{IN} ð V_{CC}	V
P_D	Continuous power dissipation	500	mW
T_J	Operating junction temperature	0 to +100	°C
T_S	Storage temperature	-40 to +125	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Name	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{IN}	DC input voltage	0	–	V_{CC}	V
T_A	Operating Free-Air Temperature	0	–	70	°C

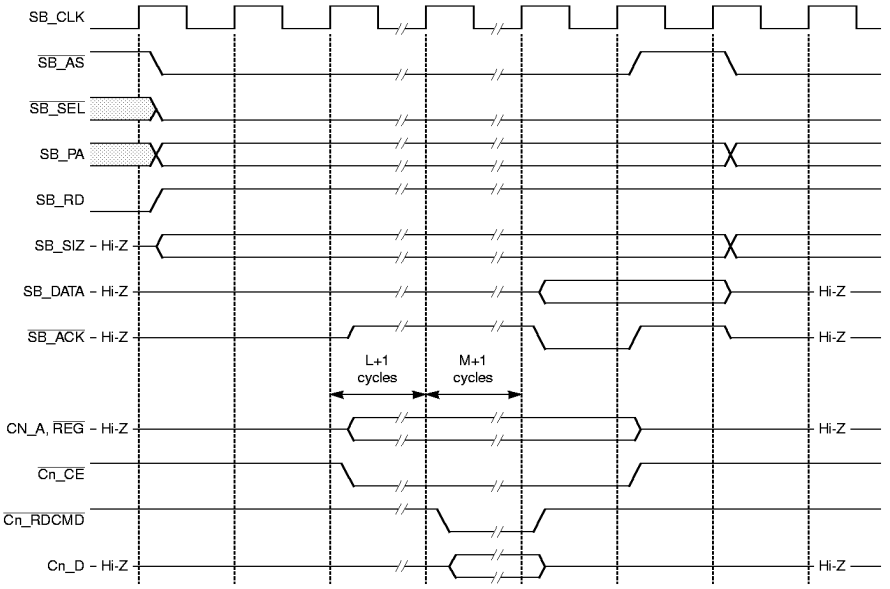
DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0	–	–	V
V_{IL}	Low Level Input Voltage		–	–	0.8	V
V_{OH}	High Level Output Voltage	4 mA Buffer, I_{OH} = -4 mA	2.4	–	–	V
		10 mA Buffer, I_{OH} = -10 mA	2.4	–	–	V
		24 mA Buffer, I_{OH} = -24 mA	2.4	–	–	V
V_{OL}	Low Level Output Voltage	4 mA Buffer, I_{OL} = 4 mA	–	–	0.4	V
		10 mA Buffer, I_{OL} = 10 mA	–	–	0.4	V
		24 mA Buffer, I_{OL} = 24 mA	–	–	0.4	V
I_{IL}	Input Leakage Current		–	–	10	µA
I_{OL}	Output Leakage Current		–	–	10	µA
C_{OUT}	Output Capacitance		–	–	5	pF
C_{IN}	Input Capacitance		–	–	5	pF

AC Characteristics: PCMCIA Interface

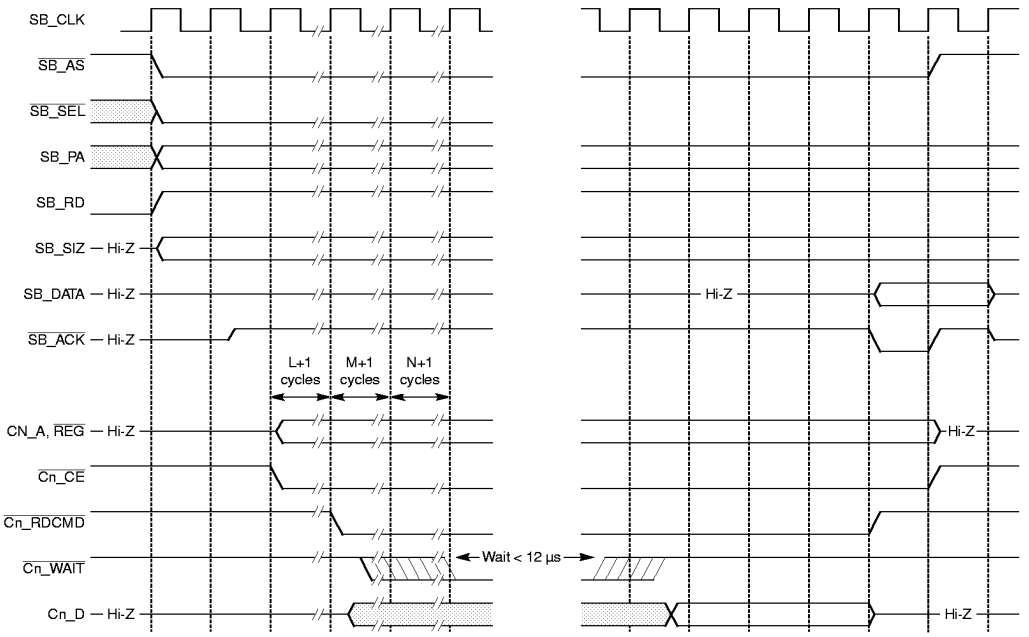
Parameter	Description	Min	Typ	Max	Units
T1	SBus CLK ↑ to Cn_A, $\overline{\text{Cn\_REG}}$ HiZ-to-valid	15.9	25.8	48.4	ns
T2	SBus CLK ↑ to $\overline{\text{Cn\_CE1}}$, $\overline{\text{Cn\_CE2}}$ high-to-low	9.3	15.3	29.5	ns
T3	SBus CLK ↑ to $\overline{\text{Cn\_OE}}$ high-to-low	9.4	15.3	28.9	ns
T4	SBus CLK ↑ to $\overline{\text{Cn\_WE}}$ high-to-low	9.7	15.4	29.8	ns
T5	SBus CLK ↑ to $\overline{\text{Cn\_IORD}}$ high-to-low	9.3	14.8	28.7	ns
T6	SBus CLK ↑ to $\overline{\text{Cn\_IOWR}}$ high-to-low	9.8	15.7	30.1	ns
T7	SBus CLK ↑ to Cn_D HiZ-to-valid write data	14.5	23.9	48.5	ns
T8	SBus CLK ↑ to Cn_A, $\overline{\text{Cn\_REG}}$ valid-to-HiZ	11.3	18.9	34.9	ns
T9	SBus CLK ↑ to $\overline{\text{Cn\_CE1}}$, $\overline{\text{Cn\_CE2}}$ low-to-high	8.3	13.5	29.5	ns
T10	SBus CLK ↑ to $\overline{\text{Cn\_OE}}$ low-to-high	8.4	14.0	27.0	ns
T11	SBus CLK ↑ to $\overline{\text{Cn\_WE}}$ low-to-high	8.9	14.1	27.2	ns
T12	SBus CLK ↑ to $\overline{\text{Cn\_IORD}}$ low-to-high	8.2	13.1	25.6	ns
T13	SBus CLK ↑ to $\overline{\text{Cn\_IOWR}}$ low-to-high	8.9	14.3	27.6	ns
T14	SBus CLK ↑ to Cn_D valid write data-to-HiZ	8.9	15.0	48.5	ns
T15	Cn_D valid read data setup to SBus CLK ↑	8.1	–	–	ns

TIMING DIAGRAMS



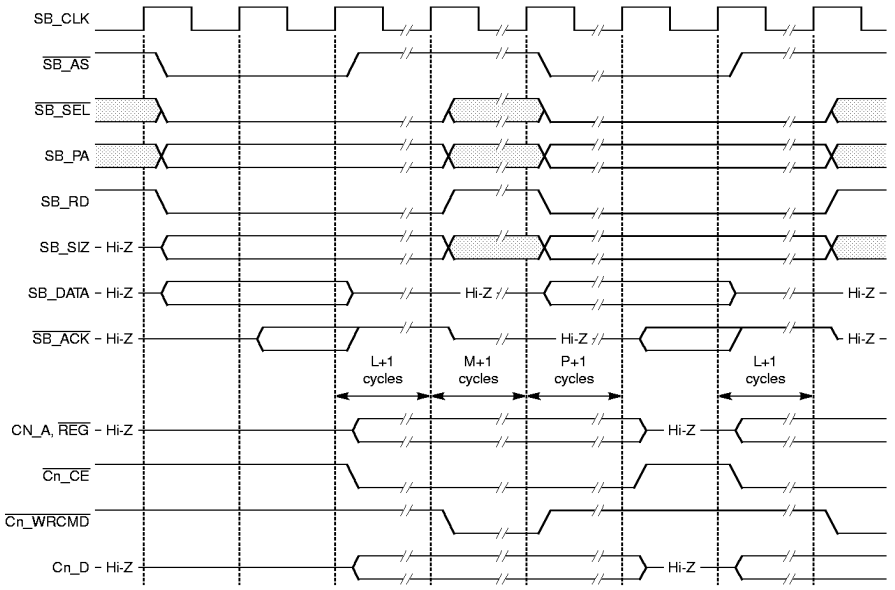
Notes: 1. n = 0 for PCMCIA Card 0 access, n = 1 for PCMCIA Card 1 access.
2. Cn_REG = 0 for Attribute Memory & I/O access, Cn_REG = 1 for Common Memory access.
3. Cn_RDCMD = Cn_OE for Attribute & Common Memory access, Cn_RDCMD = Cn_IORD for I/O access.
4. L = value of CMDDLY bits; M = value of CMDLNG bits.

Figure 4. PCMCIA Card Read Access without Wait



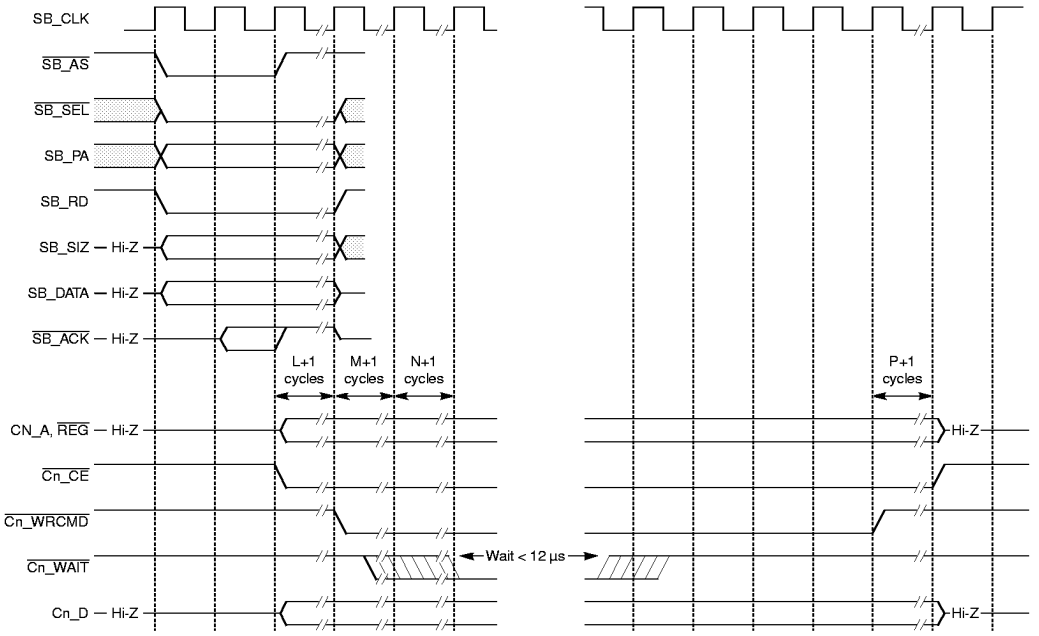
Notes: 1. n = 0 for PCMCIA Card 0 access, n = 1 for PCMCIA Card 1 access.
2. Cn_REG = 0 for Attribute Memory & I/O access, Cn_REG = 1 for Common Memory access.
3. Cn_RDCMD = Cn_OE for Attribute & Common Memory access, Cn_RDCMD = Cn_IORD for I/O access.
4. L = value of CMDDLY bits; M = value of CMDLNG bits, N = value of WAITDLY bits.

Figure 5. PCMCIA Card Read Access with Wait



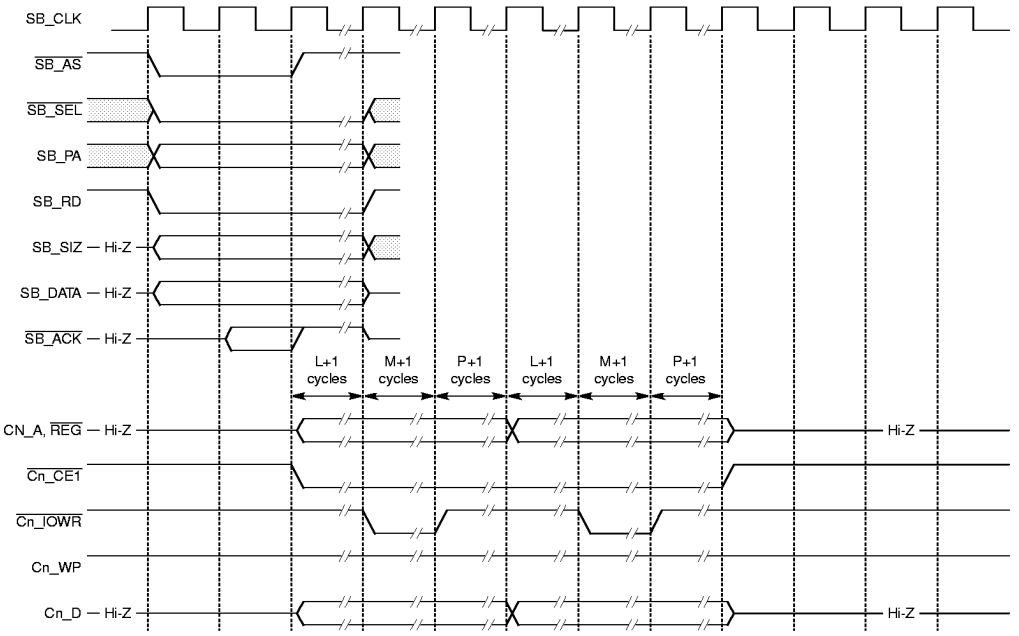
Notes: 1. n = 0 for PCMCIA Card 0 access, n = 1 for PCMCIA Card 1 access.
2. Cn_REG = 0 for Attribute Memory & I/O access, Cn_REG = 1 for Common Memory access.
3. Cn_WRCMD = Cn_WE for Attribute & Common Memory access, Cn_WRCMD = Cn_IOWR for I/O access.
4. L = value of CMDDLY bits; M = value of CMDLNG bits; P = value of RECDLY bits.

Figure 6. PCMCIA Card Write Access without Wait



Notes: 1. n = 0 for PCMCIA Card 0 access, n = 1 for PCMCIA Card 1 access.
2. Cn_REG = 0 for Attribute Memory & I/O access, Cn_REG = 1 for Common Memory access.
3. Cn_WRCMD = Cn_WE for Attribute & Common Memory access, Cn_WRCMD = Cn_IOWR for I/O access.
4. L = value of CMDDLY bits; M = value of CMDLNG bits, N = value of WAITDLY bits; P = value of RECDLY bits.

Figure 7. PCMCIA Card Write Access with Wait



Notes: 1. n = 0 for PCMCIA Card 0 access, n = 1 for PCMCIA Card 1 access.
2. Cn_REG = 0 for Attribute Memory & I/O access, Cn_REG = 1 for Common Memory access.
3. Cn_WP (Cn_IOIS16) is asserted high by PC Card n indicating that 16-bit data must be transferred in two separate byte accesses.
4. L = value of CMDDLY bits; M = value of CMDLNG bits; P = value of RECDLY bits.
5. Cn_CE2 is asserted high for both byte write accesses.

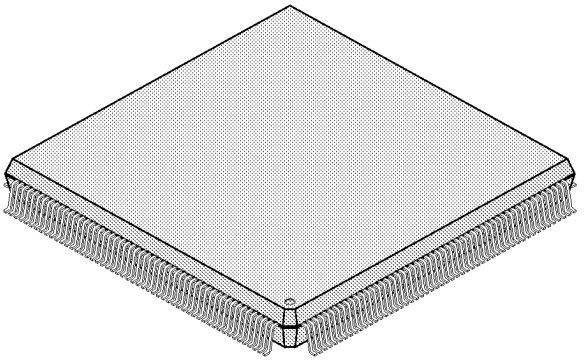
Figure 8. PCMCIA Card Write Access With Byte-Sizing (without Wait)

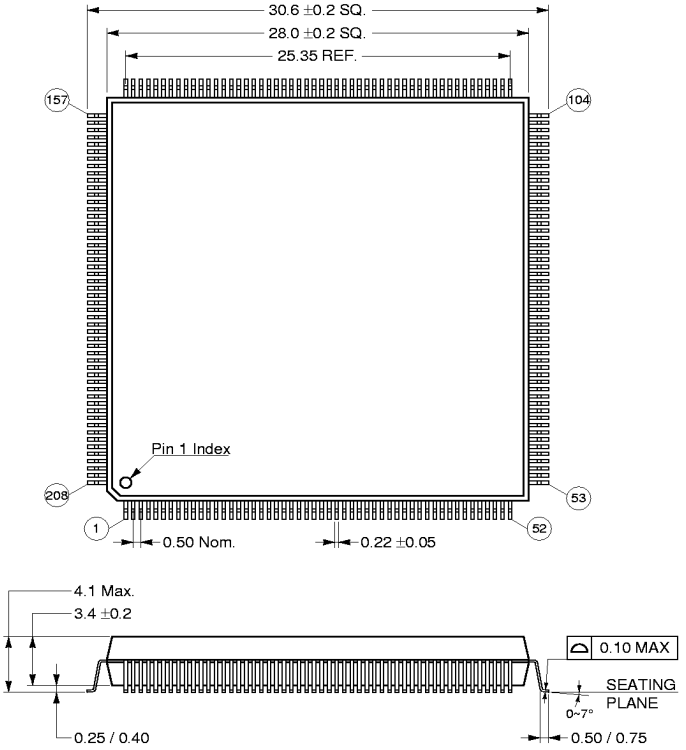
PACKAGE INFORMATION

208-Pin PQFP - Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	36	C1_D [14]	71	C0_VPP2_EN0	106	C0_A [25]	141	C0_RESET	176	GND
2	$\overline{\text{SB\_ACK}}$ [1]	37	C0_D [15]	72	$\overline{\text{C0\_RDY\_BSY}}$	107	C1_A [25]	142	C1_RESET	177	SB_D [30]
3	$\overline{\text{SB\_ACK}}$ [2]	38	GND	73	$\overline{\text{C0\_CD2}}$	108	C0_A [6]	143	$\overline{\text{C0\_REG}}$	178	SB_D [31]
4	$\overline{\text{PROM\_CS}}$	39	C1_D [15]	74	$\overline{\text{C0\_CD1}}$	109	C1_A [6]	144	$\overline{\text{C1\_REG}}$	179	$\overline{\text{SB\_INT}}$ [1]
5	$\overline{\text{SPKR\_OUT}}$	40	C0_A [10]	75	$\overline{\text{C0\_BVD2}}$	110	C0_A [5]	145	TDO	180	SB_RD
6	$\overline{\text{SCAN\_EN}}$	41	C1_A [10]	76	$\overline{\text{C0\_BVD1}}$	111	C1_A [5]	146	TMS	181	SB_PA [0]
7	$\overline{\text{SB\_RESET}}$	42	C0_A [11]	77	$\overline{\text{C0\_WAIT}}$	112	C0_A [4]	147	TCK	182	GND
8	TEST_EN	43	C1_A [11]	78	C0_WP	113	C1_A [4]	148	$\overline{\text{TRST}}$	183	SB_PA [1]
9	$\overline{\text{C0\_CE1}}$	44	C0_A [9]	79	GND	114	C0_A [3]	149	SB_CLK	184	SB_PA [2]
10	$\overline{\text{C1\_CE1}}$	45	C1_A [9]	80	$\overline{\text{C1\_RDY\_BSY}}$	115	C1_A [3]	150	TDI	185	SB_PA [3]
11	$\overline{\text{C0\_CE2}}$	46	C0_A [8]	81	$\overline{\text{C1\_CD2}}$	116	C0_A [2]	151	$\overline{\text{SB\_AS}}$	186	SB_PA [4]
12	$\overline{\text{C1\_CE2}}$	47	C1_A [8]	82	$\overline{\text{C1\_CD1}}$	117	GND	152	$\overline{\text{SB\_SEL}}$	187	SB_PA [5]
13	$\overline{\text{C0\_OE}}$	48	C0_A [17]	83	$\overline{\text{C1\_BVD2}}$	118	C1_A [2]	153	SB_SIZ [0]	188	SB_PA [6]
14	$\overline{\text{C1\_OE}}$	49	C1_A [17]	84	$\overline{\text{C1\_BVD1}}$	119	C0_A [1]	154	SB_SIZ [1]	189	SB_PA [7]
15	$\overline{\text{C0\_IORD}}$	50	C0_A [13]	85	$\overline{\text{C1\_WAIT}}$	120	C1_A [1]	155	SB_SIZ [2]	190	SB_PA [8]
16	$\overline{\text{C1\_IORD}}$	51	C1_A [13]	86	C1_WP	121	C0_A [0]	156	GND	191	SB_PA [9]
17	C0_D [3]	52	GND	87	$\overline{\text{C1\_VCC\_EN}}$	122	C1_A [0]	157	V_{CC}	192	SB_PA [10]
18	C1_D [3]	53	V_{CC}	88	C1_VPP1_EN1	123	C0_D [0]	158	SB_D [16]	193	SB_PA [11]
19	C0_D [4]	54	C0_A [18]	89	C1_VPP1_EN0	124	C1_D [0]	159	SB_D [17]	194	SB_PA [12]
20	C1_D [4]	55	C1_A [18]	90	C1_VPP2_EN1	125	C0_D [8]	160	GND	195	SB_PA [13]
21	C0_D [11]	56	C0_A [14]	91	C1_VPP2_EN0	126	C1_D [8]	161	SB_D [18]	196	V_{CC}
22	C1_D [11]	57	C1_A [14]	92	C0_A [22]	127	C0_D [1]	162	SB_D [19]	197	SB_PA [14]
23	GND	58	C0_A [19]	93	C1_A [22]	128	C1_D [1]	163	SB_D [20]	198	SB_PA [15]
24	C0_D [5]	59	C1_A [19]	94	C0_A [15]	129	V_{CC}	164	SB_D [21]	199	SB_PA [16]
25	C1_D [5]	60	C0_A [20]	95	C1_A [15]	130	GND	165	GND	200	SB_PA [17]
26	C0_D [12]	61	C1_A [20]	96	C0_A [23]	131	C0_D [9]	166	SB_D [22]	201	SB_PA [18]
27	C1_D [12]	62	C0_A [21]	97	C1_A [23]	132	C1_D [9]	167	SB_D [23]	202	SB_PA [19]
28	V_{CC}	63	C1_A [21]	98	C0_A [12]	133	C0_D [2]	168	V_{CC}	203	SB_PA [20]
29	C0_D [6]	64	C0_A [16]	99	C1_A [12]	134	C1_D [2]	169	SB_D [24]	204	SB_PA [21]
30	C1_D [6]	65	C1_A [16]	100	C0_A [24]	135	C0_D [10]	170	SB_D [25]	205	SB_PA [22]
31	C0_D [13]	66	GND	101	C1_A [24]	136	C1_D [10]	171	GND	206	$\overline{\text{SB\_INT}}$ [0]
32	C1_D [13]	67	$\overline{\text{C0\_VCC\_EN}}$	102	C0_A [7]	137	$\overline{\text{C0\_IOWR}}$	172	SB_D [26]	207	$\overline{\text{SB\_ACK}}$ [0]
33	C0_D [7]	68	C0_VPP1_EN1	103	C1_A [7]	138	$\overline{\text{C1\_IOWR}}$	173	SB_D [27]	208	V_{CC}
34	C1_D [7]	69	C0_VPP1_EN0	104	V_{CC}	139	$\overline{\text{C0\_WE}}$	174	SB_D [28]		
35	C0_D [14]	70	C0_VPP2_EN1	105	GND	140	$\overline{\text{C1\_WE}}$	175	SB_D [29]		

208-Pin PQFP Package Dimensions





Dimensions in millimeters.

ORDERING INFORMATION

Part Number	Description
STP4020PQFP	PCMCIA Controller Interface, 208-Pin Plastic Quad Flat Pack (PQFP)

Document Part Number: 805-0738-02