TriTech Microelectronics

TR89103CS

Caller ID Receiver

Features

- Single 3.5-5.25V power supply
- Demodulates both V.23 and Bell 202 modes
- Compatible with:
  - Bellcore specification TR-NWT-00030 & SR-TSV-002476
  - UK SIN227 & SIN242 - TW/P&E/312
  - Austel standard TP01627.1
  - Singapore TAS TS PSTN1-A-CLIP: 1994
- High input sensitivity -48dBm
- Low power CMOS
- 8-pin SOIC package

General Description

The TriTech TR89103 is an integrated Caller ID receiver designed to operate in countries using FSK based Caller ID systems.

The TR89103 includes an FSK receiver which meets both the Bell 202 and V.23 requirements. The TR89103 is designed to offer superior flexibility and features over other CID devices available. The circuit is designed into an 8-pin small outline package for system cost savings.

Block Diagram

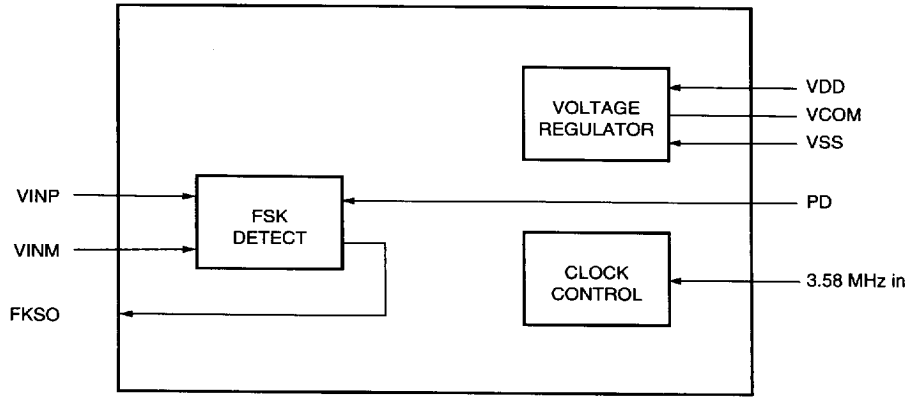
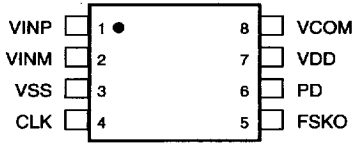


***Figure 1** • TR89103 Block Diagram*

Pin Configuration



8-pin SOIC, Top View

Pin Descriptions

Pin No	Pin Name	I/O	Description
1	VINP	I	Non-inverting input of the differential input buffer. Internally biased.
2	VINM	I	Inverting input of the differential input buffer. Internally biased.
3	VSS	—	Ground
4	CLK	I	3.58MHz TTL Clock input pin.
5	FSKO	O	FSK demodulator output. Delivers the digital data during the FSKO demodulation. Logic low when inactive.
6	PD	I	Power Down active high
7	VDD	—	VDD
8	VCOM	—	Reference voltage pin. Connect 0.1µF Capacitor to VSS.

Circuit Description

The Caller ID feature is an on-hook capability which provides the user with information about the caller before actually answering the call. The information is transmitted as 1200 bps FSK data during the silent interval between the first two ringing bursts.

FSK detector

The FSK detector's main function is to demodulate the incoming 1200 bps FSK signal which carries the CID data and generate a serial TTL data output (FSKO). The detector complies to the two different FSK standards used, namely Bell 202 for the US and ITU-T recommendation V.23 elsewhere. The detector has internally biased differential inputs (VINP, VINM) and the gain is set to accommodate low-level signals down to -48dBm. The filtered signal is applied to the FSK demodulator. The demodulated data stream can then be processed by a microcontroller.

Clock Input

The device uses a external oscillator connected to the pin CLK. The frequency at CLK must be 3.58MHz for correct operation of the device.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V	VDD Supply Voltage	-0.5	5.5	V
Vi	Input Voltage	-0.3	5.8	V
Vo	Output Voltage	-0.3	5.8	V
Ts	Storage Temperature	-40	125	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD	Supply Voltage	3.5	5.0	5.25	V
Ta	Ambient Temperature	0		70	°C
CLK	Clock input frequency		3.58		MHz

General Specifications

DC Characteristics (VDD = 5V, Ta = 25°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
IDD1	Supply Current			3.8		mA
IPD	Supply Current	PD=1 See note 1		0.2	1	µA
Iil	Input Leakage Current		-10		10	µA
Vil	Low Level Input Voltage				0.8	V
Vih	High Level Input Voltage		2.0			V
Vol	Low Level Output Voltage	|Iol|<4mA			0.4	V
Voh	High Level Output Voltage	|Ioh|<20µA	2.4			V

Note:

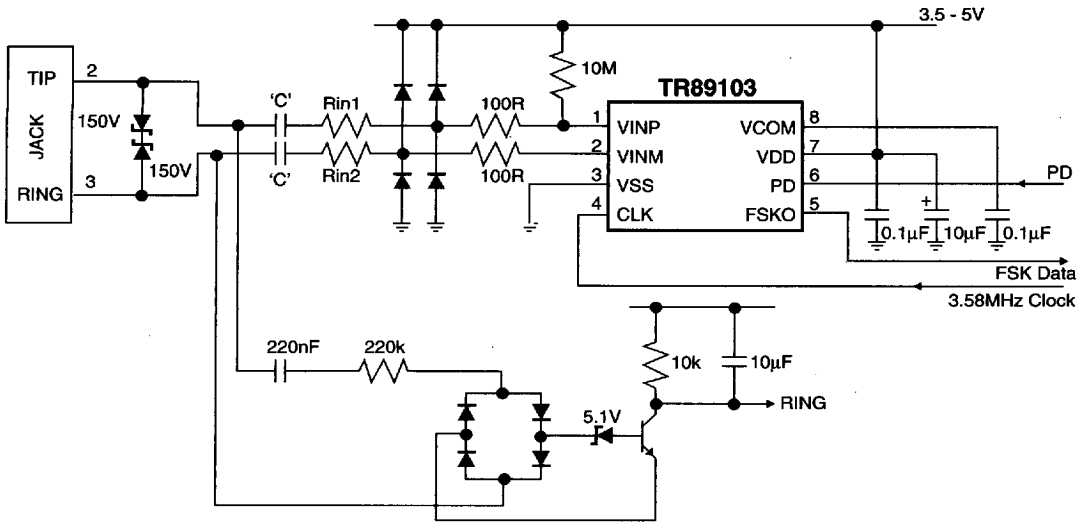
1. Ensure VinP has 10MΩ pull up resistor connected or power down current will be higher.

AC Characteristics

FSK Detection (1 dBm= 1mW into a load of 600Ω, VDD = 5V, Ta=25°C)

Parameter	Conditions	Min	Typ	Max	Units
Input Sensitivity for FSK Reception	See table	-48		-12	dBm
Logical 1 at FSKO	Bell V.23	1188 1280.5	1200 1300	1212 1319.5	Hz
Logical 0 at FSKO	Bell V.23	2188 2068.5	2200 2100	2222 2131.5	Hz

Typical Application



The resistors Rin1 and Rin2 are selected to optimise the input sensitivity based on the table below. The typical values for Rin1 and Rin2 are 220kΩ.

Input Range (dbm0)	Rin	'C'
-14 to -48	68kΩ	1nF
-12 to -46	150kΩ	0.5nF
-10 to -44	220kΩ	0.33nF
-8 to -42	330kΩ	0.22nF

Make sure that the 10MΩ pull-up resistor is installed as this will prevent the inputs from floating and minimise the current during power down to 0.2µA.

Mechanical Dimensions

8 Pin SOIC – Dimensions in inches (mm)