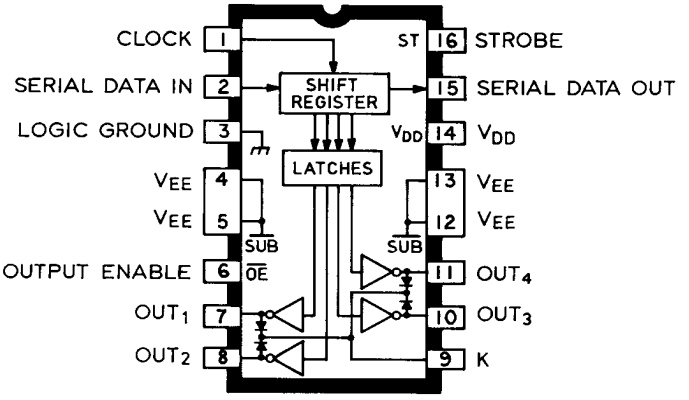
UCN-5825B AND UCN-5826B BiMOS II HIGH-CURRENT, SERIAL-INPUT, LATCHED DRIVERS

FEATURES

- 2 A Open Collector Outputs
- 60 V or 80 V Minimum Output Breakdown
- 35 V or 60 V Sustaining Voltage
- Output-Transient Protection
- Low-Power CMOS Logic and Latches
- Typical Data Input Rate > 5 MHz
- Internal Pull-Down Resistors
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Thermal Shutdown Circuitry



Dwg. No. A-12,557

UCN-5825B and UCN-5826B BiMOS II integrated circuits combine a 4-bit CMOS shift register, associated latches, control circuitry, and level shifting, with bipolar Darlington outputs and transient-suppression diodes for inductive load applications.

The high-current, serial-input, latched drivers can be used with relays, solenoids, stepper motors, LED displays, incandescent displays, and other high-power loads. Control circuitry for both devices includes STROBE and OUTPUT ENABLE functions, and an internal latch that disables outputs at power-up and provides thermal shutdown protection.

Except for output-voltage ratings, the UCN-5825B and UCN-5826B drivers are identical. The former is rated for operation to 60 V (35 V sustaining); the latter has a minimum output breakdown rating of 80 V (60 V sustaining).

The CMOS inputs cause minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to insure a proper input-logic high level. A CMOS serial data output enables cascade connections in applications requiring additional drive lines. With a 5 V supply, BiMOS II devices typically operate at data-input rates above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

Monolithic construction and a 16-pin dual in-line package with copper heat-sink contact tabs enable cost-effective and reliable systems designs supported by excellent package power dissipation rating, minimum size, and ease of installation. The package configuration is suitable for automatic insertion, allows easy attachment of an inexpensive heat sink, and fits a standard IC socket or printed wiring board layout.

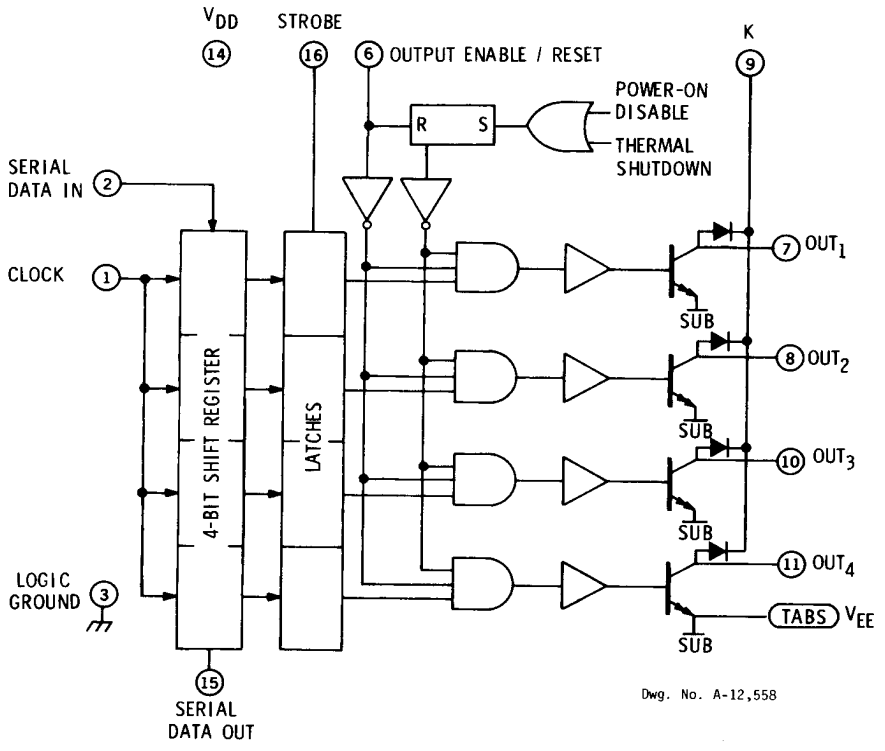
Both devices are rated for continuous operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, simultaneous operation of all drivers may require a reduction in duty cycle.

INTEGRATED CIRCUIT DIVISIONS
SPRAGUE ELECTRIC COMPANY
115 Northeast Cutoff, WORCESTER, MASS. 01606

UCN-5825B AND UCN-5826B
BiMOS II HIGH-CURRENT, SERIAL-INPUT, LATCHED DRIVERS

ENGINEERING BULLETIN
24185.3

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-12,558

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

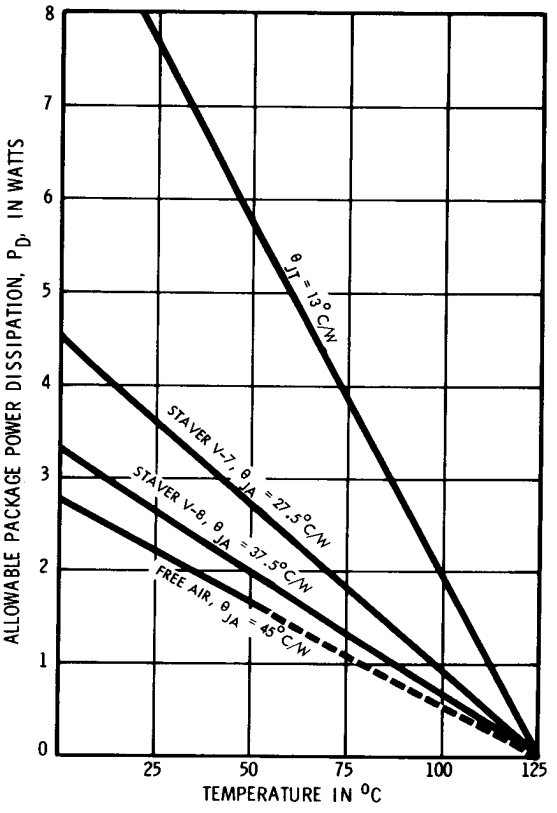
Output Voltage, V_{CE}
(UCN-5825B) ..... 60 V
(UCN-5826B) ..... 80 V
Output Voltage, $V_{CE(sus)}$
(UCN-5825B) ..... 35 V*
(UCN-5826B) ..... 60 V*
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 15 V
V_{DD} with reference to V_{EE} ..... 25 V
Emitter Supply Voltage, V_{EE} ..... −20 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} ..... 2 A
Allowable Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*For inductive load applications: The sum of the load supply voltage and clamping voltage(s).

Note: Output-current rating may be limited by duty cycle, ambient temperature, heat sinking, and a number of outputs conducting. Under any combination of conditions, do not exceed the specified maximum current rating and a junction temperature of +125°C.

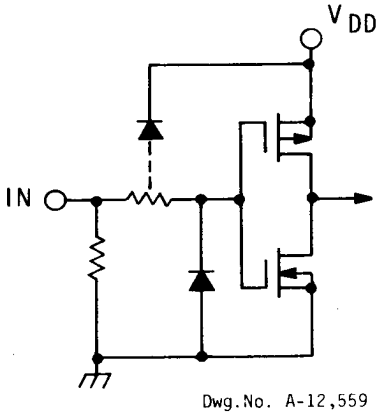
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



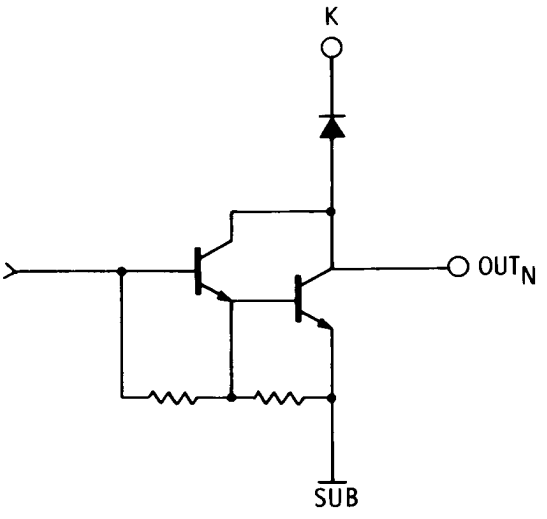
Dwg. No. A-12,560

TYPICAL INPUT CIRCUIT



Dwg.No. A-12,559

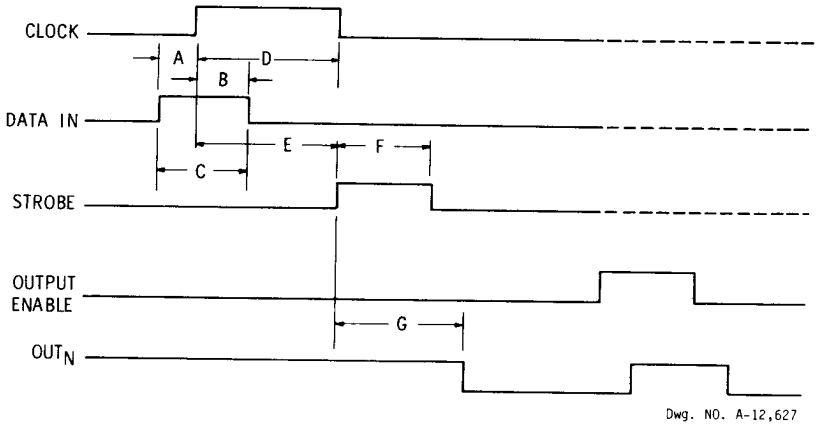
TYPICAL OUTPUT DRIVER



Dwg. No. A-12,561

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 60$ V, $V_{DD} = 5$ V to 12 V, $V_{EE} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UCN-5825B	$T_A = +25°C$	—	100	µA
			$T_A = +70°C$	—	500	µA
		UCN-5826B	$V_{CC} = 80$ V, $T_A = +25°C$	—	100	µA
			$V_{CC} = 80$ V, $T_A = +70°C$	—	500	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Both	$I_{OUT} = 1.75$A	—	1.75	V
Output Sustaining Voltage	$V_{CE(sus)}$	UCN-5825B	$I_{OUT} = 1.75$ A, L = 2 mH	35	—	V
		UCN-5826B	$I_{OUT} = 1.75$ A, L = 2 mH	60	—	V
Clamp Diode Leakage Current	I_R	UCN-5825B	$V_R = 60$ V	—	100	µA
		UCN-5826B	$V_R = 80$ V	—	100	µA
Clamp Diode Forward Voltage	V_F	Both	$I_F = 1.75$ A	—	2.0	V
Input Voltage	$V_{IN(1)}$	Both	$V_{DD} = 5.0$ V	3.5	5.3	V
			$V_{DD} = 12$ V	10.5	12.3	V
	$V_{IN(0)}$	Both	$V_{DD} = 5$ V to 12 V	−0.3	+0.8	V
Input Resistance	R_{IN}	Both	$V_{DD} = 5.0$ V	100	—	kΩ
			$V_{DD} = 12$ V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	Both	$V_{DD} = 5.0$ V	—	20	kΩ
			$V_{DD} = 12$ V	—	6.0	kΩ
Supply Current	I_{DD}	Both	All outputs OFF	—	3.0	mA
			All outputs ON	—	20	mA
Maximum Clock Frequency	f_C	Both		3.3	—	MHz
Turn-ON Delay	t_{PLH}	Both	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-OFF Delay	t_{PHL}	Both	0.5 E_{in} to 0.5 E_{out}	—	2.0	µs
Propagation Delay	t_{PD}	Both	0.5 E_{clock} to 0.5 E_{out}	—	100	ns



TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of the latches.

Two additional functions serve to protect the system and the device. Either power-up or overheating will set an internal latch that disables the outputs. With the latch set, data can be shifted and latched while the outputs are disabled. To resume normal operation, the latch must be reset by toggling OUTPUT ENABLE a minimum of 500 ns.

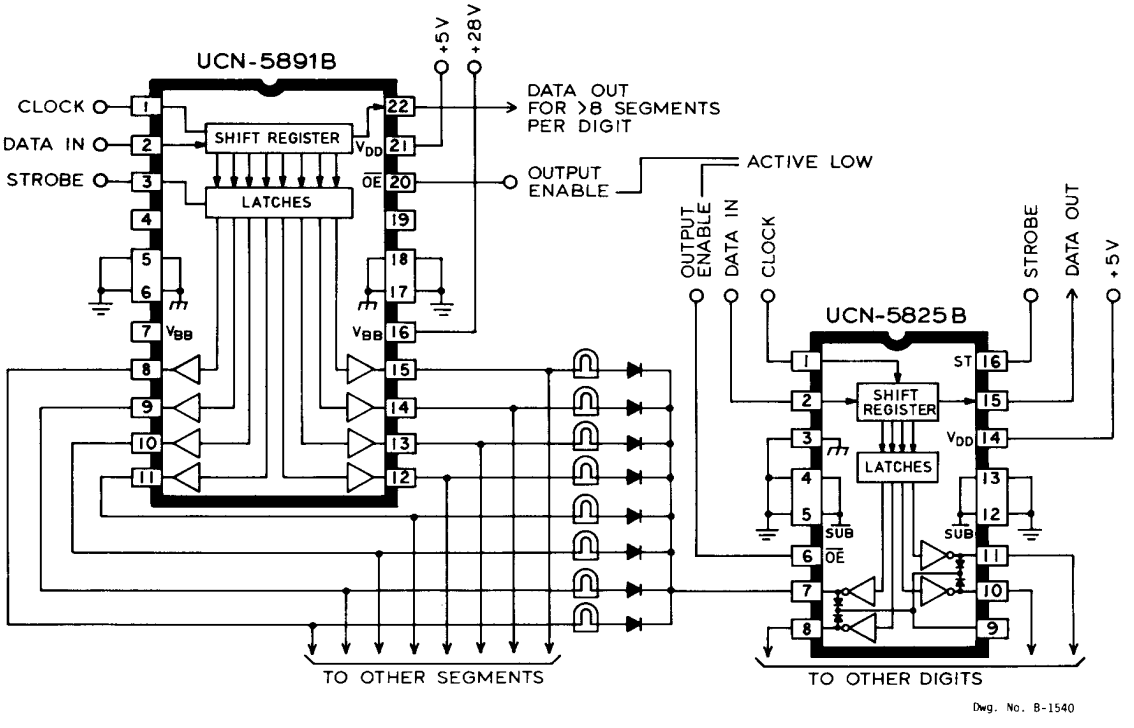
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents				Serial Data Output	Strobe Input	Latch Contents				Output Enable	Output Contents			
		I_1	I_2	I_3	I_4			I_1	I_2	I_3	I_4		I_1	I_2	I_3	I_4
H	↑	H	R_1	R_2	R_3	R_3										
L	↑	L	R_1	R_2	R_3	R_3										
X	↓	R_1	R_2	R_3	R_4	R_4										
		X	X	X	X	X	L	R_1	R_2	R_3	R_4					
		P_1	P_2	P_3	P_4	P_4	H	P_1	P_2	P_3	P_4	L	P_1	P_2	P_3	P_4
								X	X	X	X	H	H	H	H	H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

TYPICAL APPLICATION

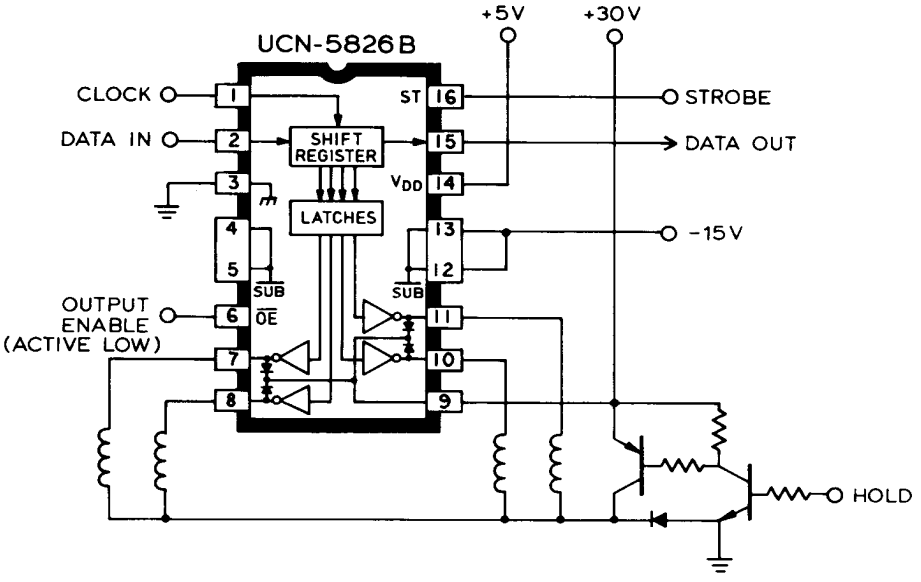
MULTIPLEXED INCANDESCENT LAMP DRIVE



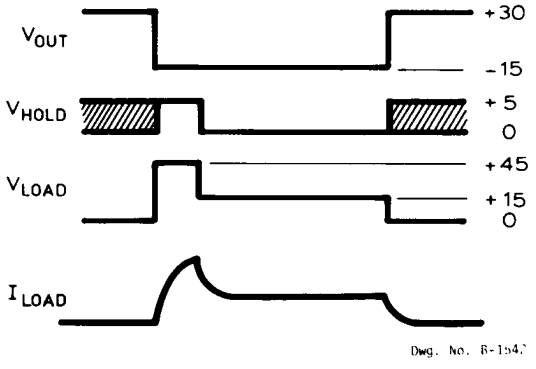
*Active Low

TYPICAL APPLICATION

HAMMER DRIVE

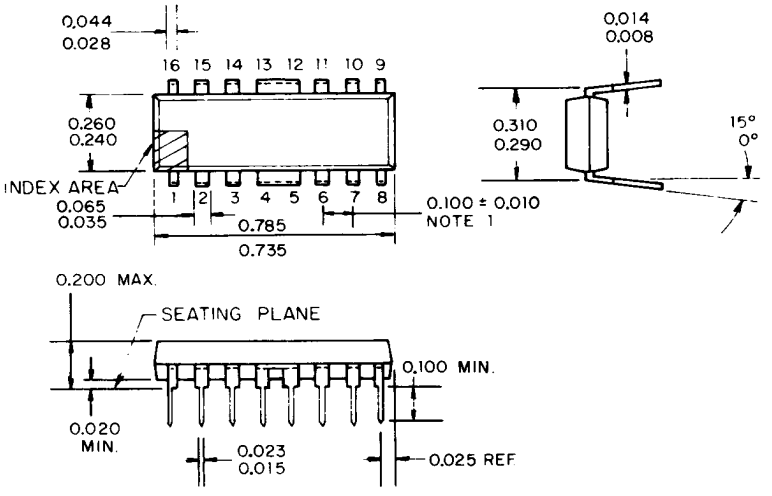


*Active Low



Dwg. No. B-1547

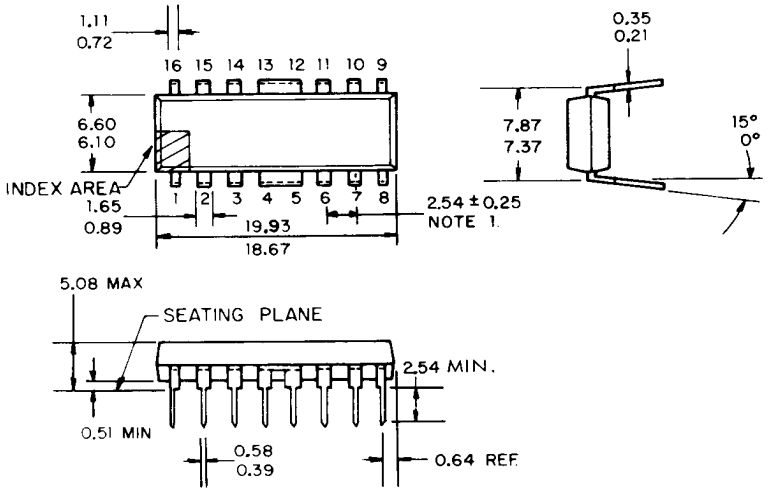
DIMENSIONS IN INCHES



Dwg. No. A-10,311C IN

DIMENSIONS IN MILLIMETRES

Based on 1" = 25.4 mm



Dwg. No. A-10,311C MM

NOTES:

1. Lead spacing tolerances is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead gauge plane is 0.030" (0.76 mm) max. below seating plane.

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In the construction of the components described, the full intent of the specification will be met. The Sprague Electric Company, however, reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the design of its products. Components made under military approvals will be in accordance with the approval requirements.

The information included herein is believed to be accurate and reliable. However, the Sprague Electric Company assumes no responsibility for its use; nor for any infringements of patents or other rights of third parties which may result from its use.

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