

## SWITCHING REGULATOR APPLICATIONS

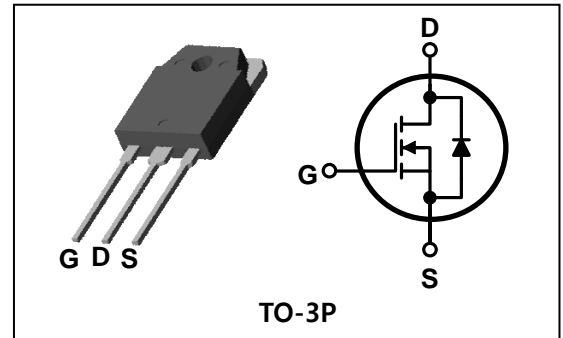
### Features

- High Voltage :  $BV_{DSS}=500V(\text{Min.})$
- Low  $C_{RSS}$  :  $C_{RSS}=27pF(\text{Typ.})$
- Low gate charge :  $Q_g=65nC(\text{Typ.})$
- Low  $R_{DS(on)}$  :  $R_{DS(on)}=0.26\Omega(\text{Max.})$

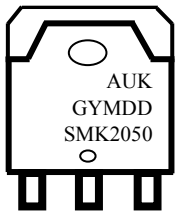
### Ordering Information

Type No.	Marking	Package Code
SMK2050CI	SMK2050	TO-3P

### PIN Connection



### Marking Diagram

	Column 1 : Manufacturer
	Column 2 : Production Information e.g.) GYMDD
	- G : Factory management code - YMDD : Date Code (year, month, date)
	Column 3 : Device Code

### Absolute maximum ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	500	V
Gate-source voltage	$V_{GSS}$	$\pm 30$	V
Drain current (DC) *	$I_D$	( $T_C=25^\circ\text{C}$ )	20
		( $T_C=100^\circ\text{C}$ )	12.6
Drain current (Pulsed) *	$I_{DM}$	80	A
Drain power dissipation	$P_D$	150	W
Avalanche current (Single) ②	$I_{AS}$	20	A
Single pulsed avalanche energy ②	$E_{AS}$	1000	mJ
Avalanche current (Repetitive) ①	$I_{AR}$	20	A
Repetitive avalanche energy ①	$E_{AR}$	28	mJ
Junction temperature	$T_J$	150	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	-55~150	

\* Limited by maximum junction temperature

Characteristic	Symbol	Typ.	Max.	Unit
Thermal resistance	Junction-case	-	0.83	$^\circ\text{C}/\text{W}$
	Junction-ambient	-	40	

## Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Drain-source breakdown voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0	500	-	-	V	
Gate threshold voltage	V <sub>GS(th)</sub>	I <sub>D</sub> =250μA, V <sub>DS</sub> =V <sub>GS</sub>	2	-	4	V	
Drain-source cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> =500V, V <sub>GS</sub> =0V	-	-	1	μA	
		V <sub>DS</sub> =400V, V <sub>GS</sub> =0V T <sub>C</sub> =125°C	-	-	100		
Gate leakage current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V	-	-	±100	nA	
Drain-source on-resistance ④	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	-	0.21	0.26	Ω	
Forward transfer conductance ④	g <sub>fs</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =10A	-	24.6	-	S	
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz	-	3120	-	pF	
Output capacitance	C <sub>oss</sub>		-	355	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	27	-		
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =250V, I <sub>D</sub> =20A R <sub>G</sub> =25Ω	-	95	-	ns	
Rise time	t <sub>r</sub>		-	375	-		
Turn-off delay time	t <sub>d(off)</sub>		③④	-	100		-
Fall time	t <sub>f</sub>		-	-	105		-
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> =400V, V <sub>GS</sub> =10V I <sub>D</sub> =20A	-	65	85	nC	
Gate-source charge	Q <sub>gs</sub>		-	17.6	-		
Gate-drain charge	Q <sub>gd</sub>		③④	-	18.4		-

## Source-Drain Diode Ratings and Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

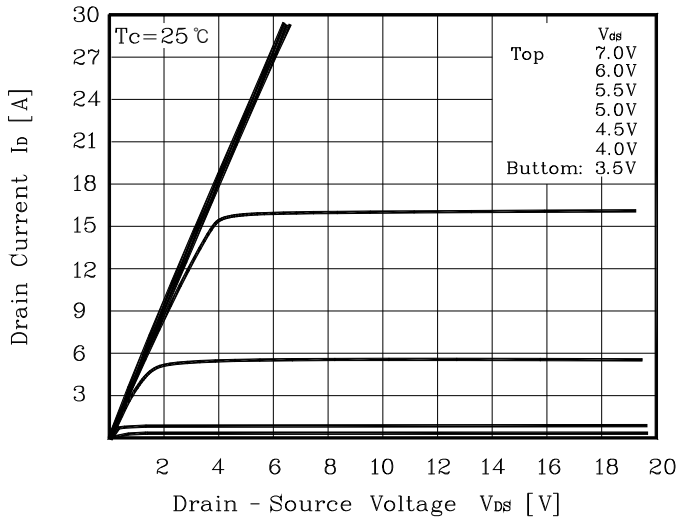
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I <sub>S</sub>	Integral reverse diode in the MOSFET	-	-	20	A
Source current (Pulsed) ①	I <sub>SP</sub>		-	-	80	
Forward voltage ④	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	-	1.4	V
Reverse recovery time	t <sub>rr</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V dI <sub>S</sub> /dt=100A/us	-	507	-	ns
Reverse recovery charge	Q <sub>rr</sub>		-	7.2	-	μC

Note ;

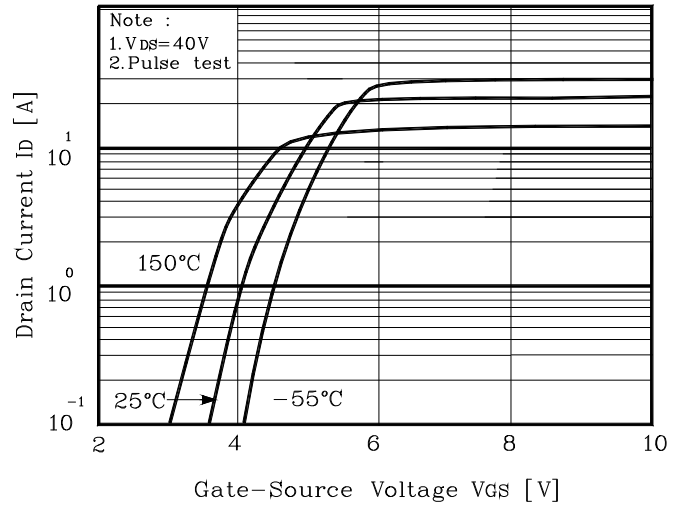
- ① Repetitive rating : Pulse width limited by maximum junction temperature
- ② L=4.5mH, I<sub>AS</sub>=20A, V<sub>DD</sub>=50V, R<sub>G</sub>=25Ω, Starting T<sub>J</sub>=25°C
- ③ Pulse Test : Pulse width≤300us, Duty cycle≤2%
- ④ Essentially independent of operating temperature

## Electrical Characteristic Curves

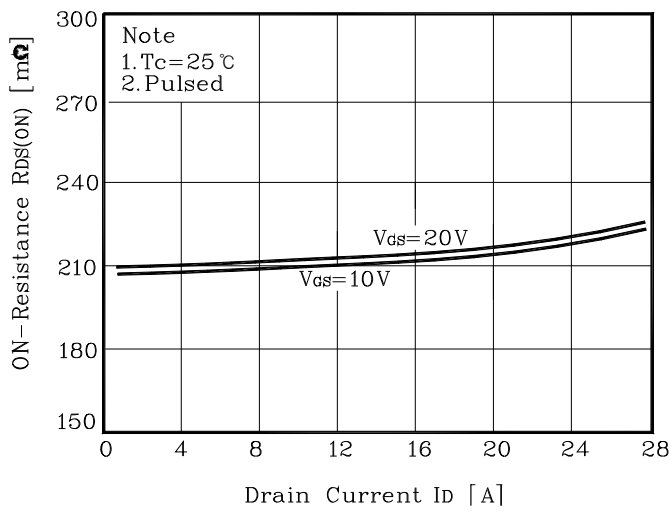
**Fig. 1  $I_D - V_{DS}$**



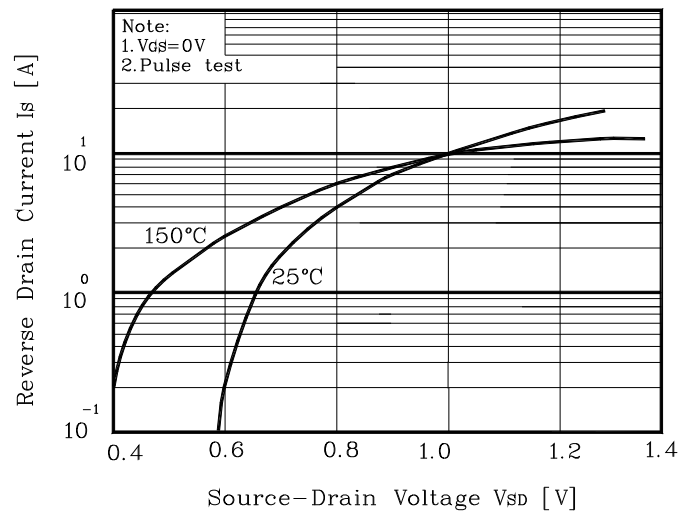
**Fig. 2  $I_D - V_{GS}$**



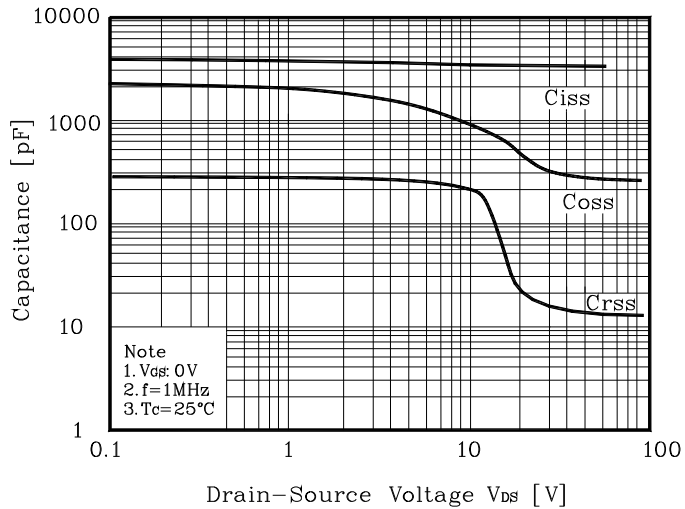
**Fig. 3  $R_{DS(on)} - I_D$**



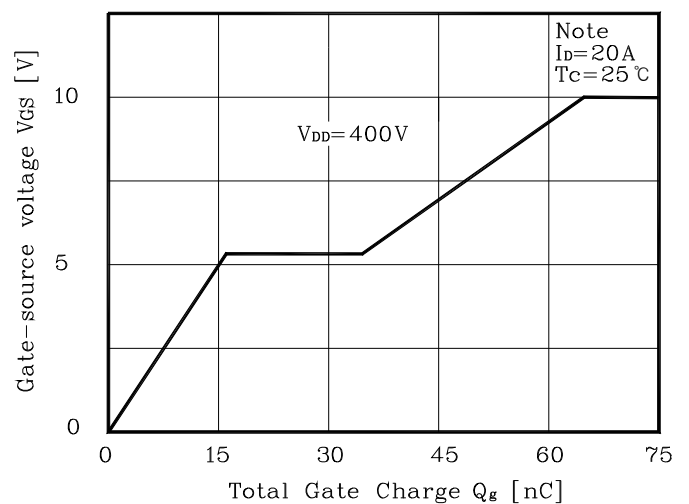
**Fig. 4  $I_S - V_{SD}$**



**Fig. 5 Capacitance -  $V_{DS}$**

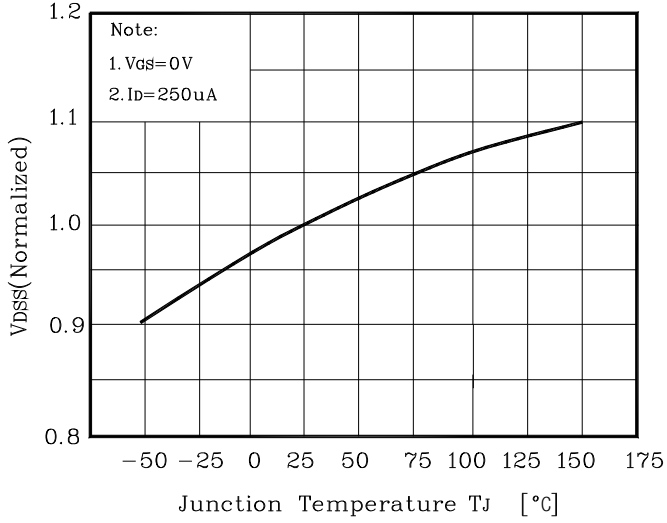


**Fig. 6  $V_{GS} - Q_G$**

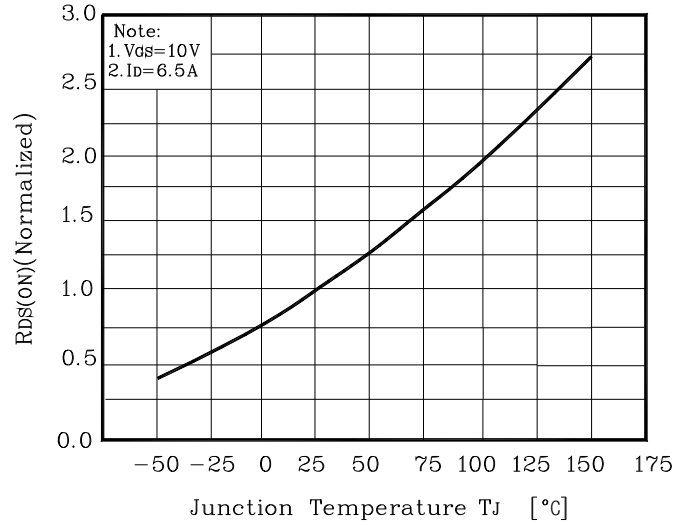


## Electrical Characteristic Curves

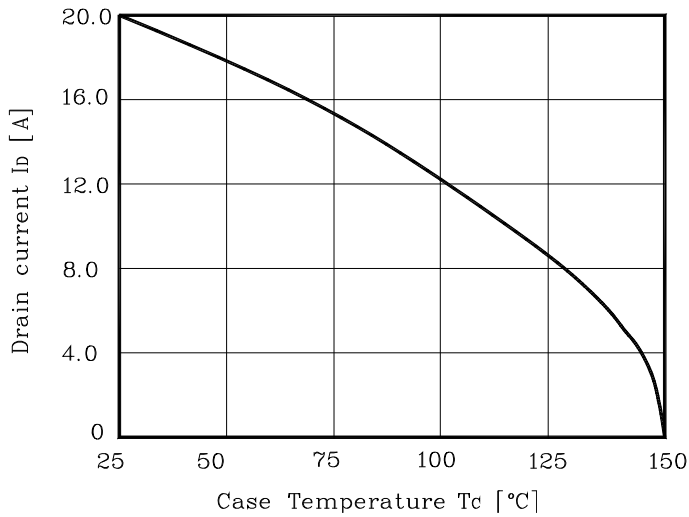
**Fig. 7  $V_{DSS} - T_J$**



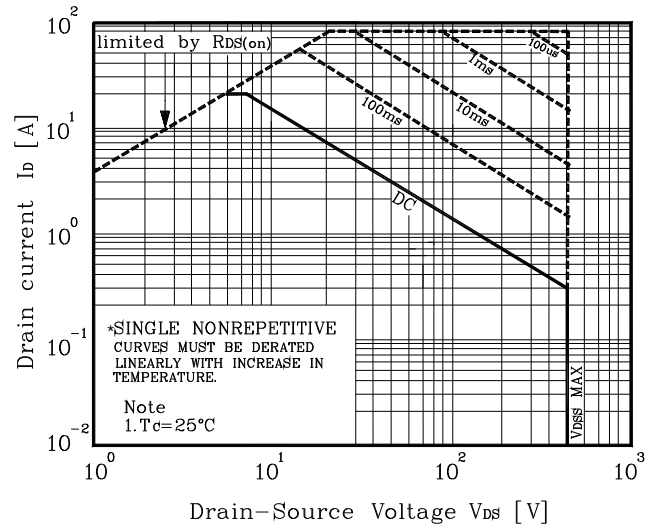
**Fig.8  $R_{DS(on)} - T_J$**



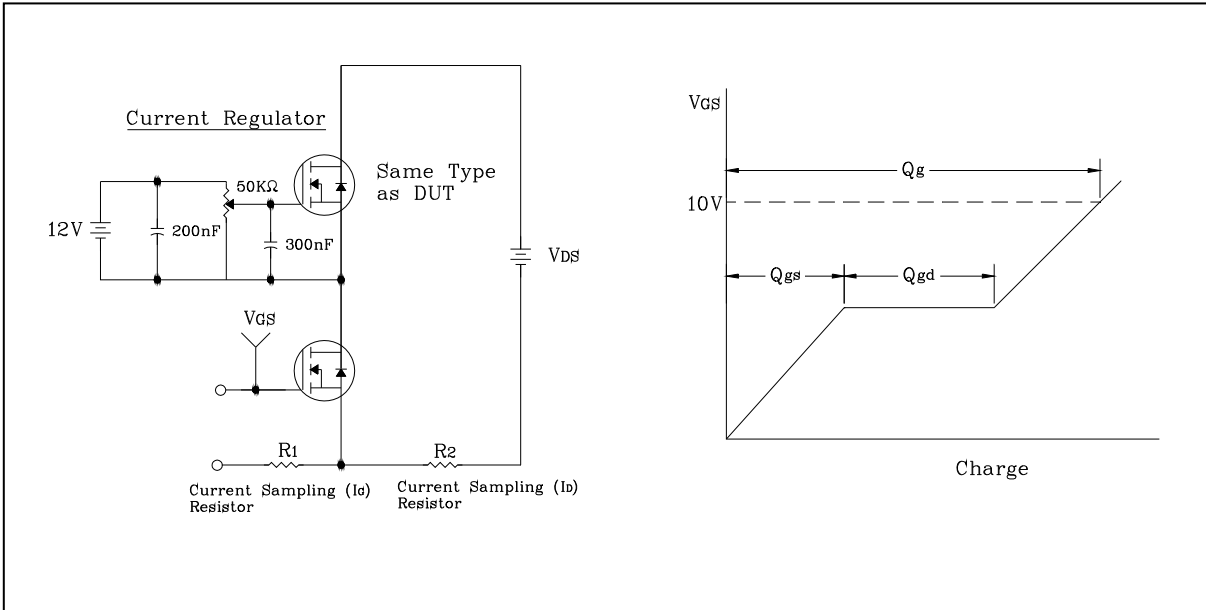
**Fig. 9  $I_D - T_C$**



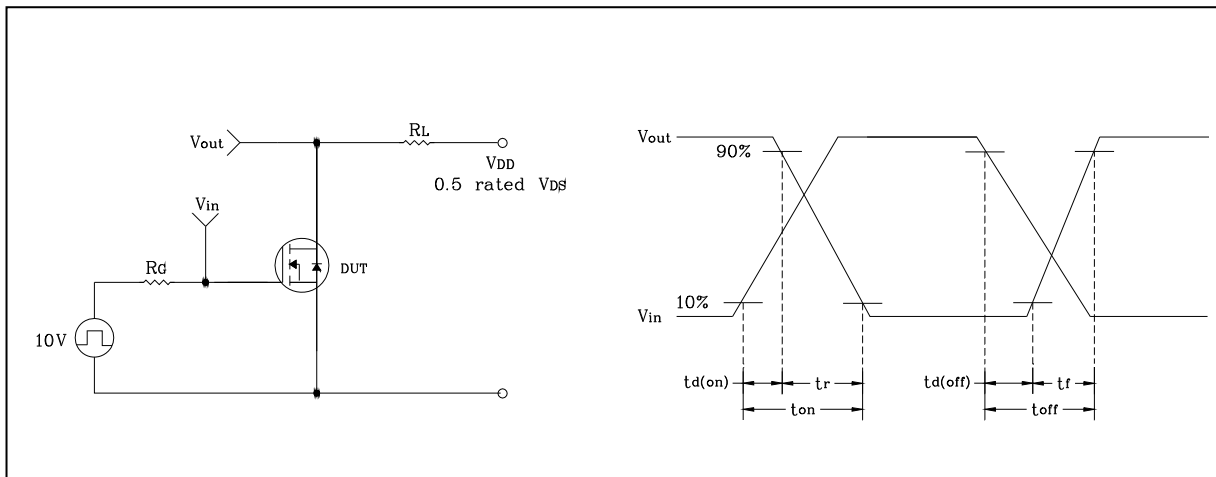
**Fig. 10 Safe Operating Area**



**Fig. 11 Gate Charge Test Circuit & Waveform**



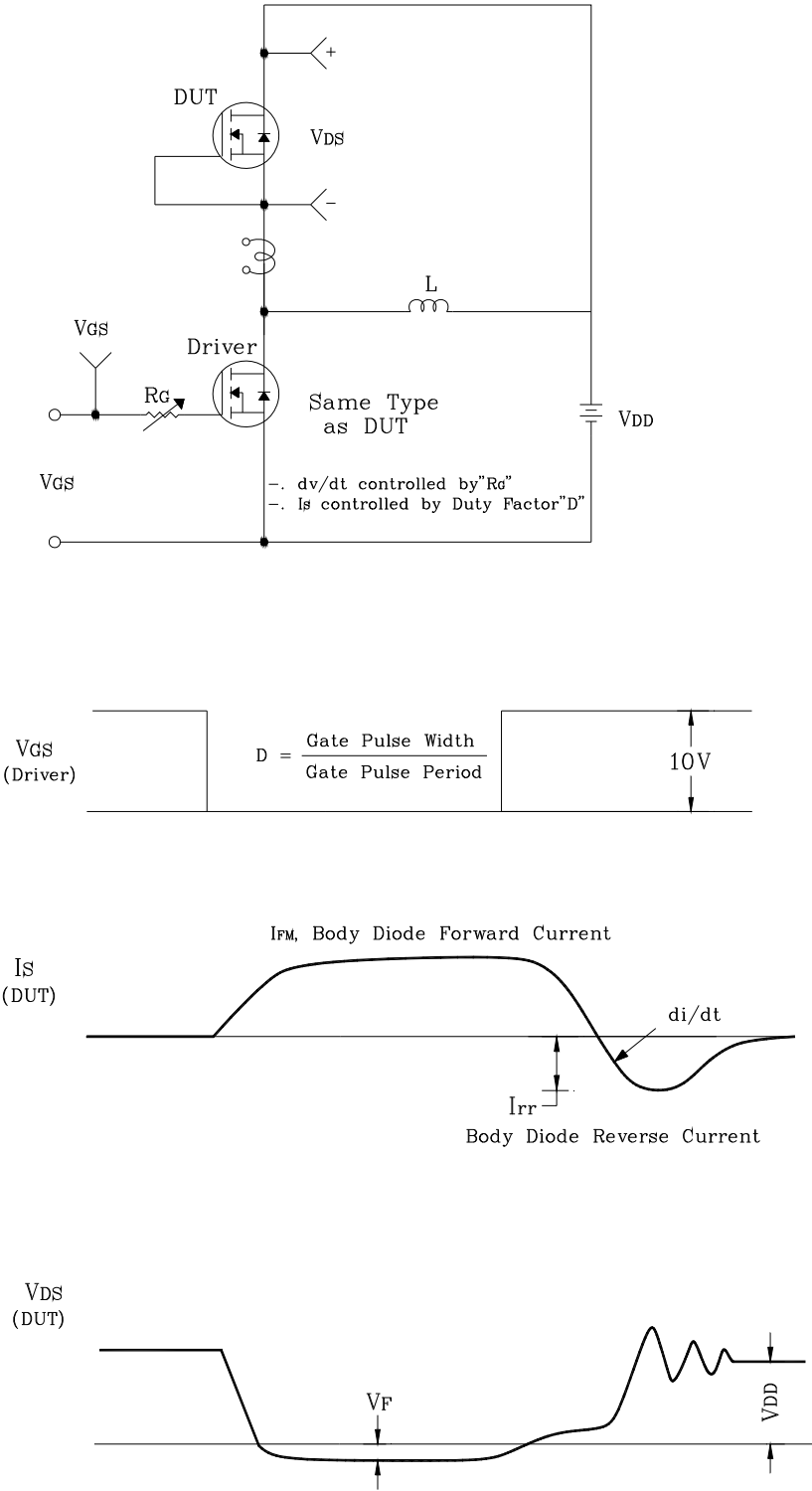
**Fig. 12 Resistive Switching Test Circuit & Waveform**



**Fig. 13 E<sub>AS</sub> Test Circuit & Waveform**

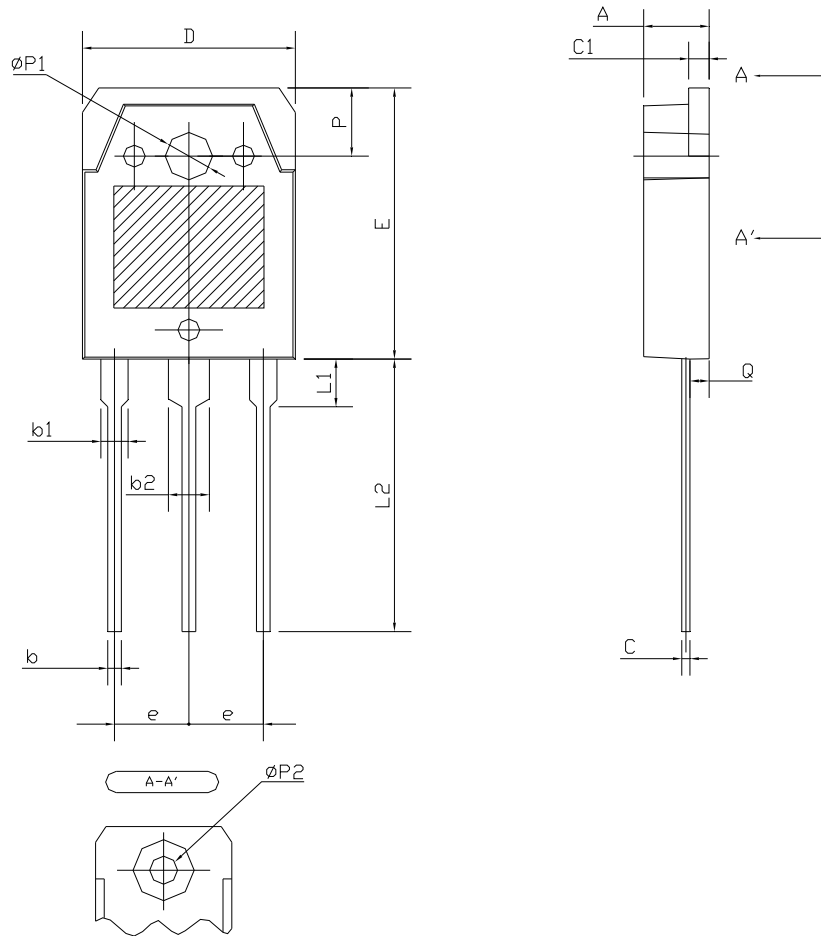


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform



## Outline Dimension

unit: mm



SYMBOL	MIN	NOM	MAX
A	4.60	4.80	5.00
b	0.80	1.00	1.20
b1	1.80	2.00	2.20
b2	2.80	3.00	3.20
C	0.55	0.60	0.75
C1	1.45	1.50	1.65
D	15.40	15.60	15.80
E	19.70	19.90	20.10
e	5.15	5.45	5.75
L1	3.30	3.50	3.70
L2	19.80	20.00	20.20
P	4.80	5.00	5.20
$\phi P1$	3.30	3.40	3.50
$\phi P2$	(3.20)		
Q	1.20	1.40	1.60

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