74LVC16244A; 74LVCH16244A

16-bit buffer/line driver; 5 V input/output tolerant; 3-state

Rev. 11 — 27 October 2011 Product data sheet

1. General description

The 74LVC16244A; 74LVCH16244A are 16-bit non-inverting buffer/line drivers with 3-state bus compatible outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. It features four output enable inputs, ($1\overline{OE}$ to $4\overline{OE}$) each controlling four of the 3-state outputs. A HIGH on $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

The 74LVCH16244A bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features and benefits

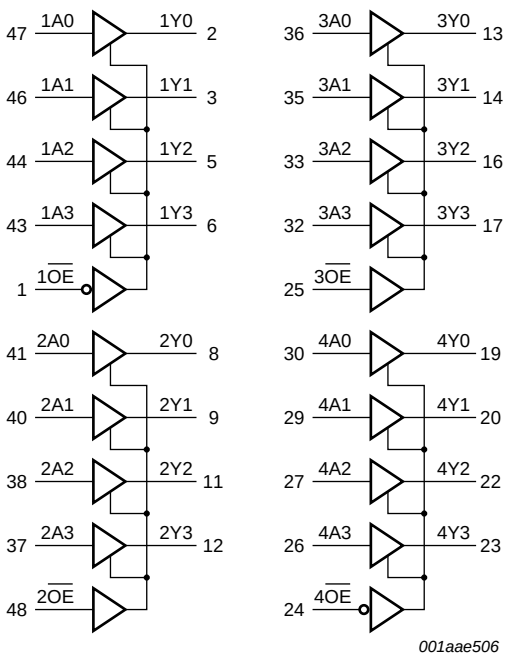
- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- High-impedance when V_{CC} = 0 V
- All data inputs have bus hold. (74LVCH16244A only)
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

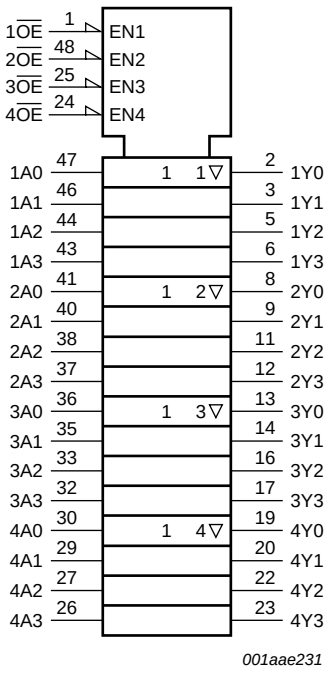
Type number	Temperature range	Package		
		Name	Description	Version
74LVC16244ADL	−40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVCH16244ADL				
74LVC16244ADGG	−40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVCH16244ADGG				
74LVC16244AEV	−40 °C to +125 °C	VFBGA56	plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 × 7 × 0.65 mm	SOT702-1
74LVCH16244AEV				
74LVC16244ABX	−40 °C to +125 °C	HXQFN60U	plastic thermal enhanced extremely thin quad flat package; no leads; 60 terminals; UTLP based; body 4 × 6 × 0.5 mm	SOT1134-1
74LVCH16244ABX				

4. Functional diagram



Pin numbers are shown for SSOP48 and TSSOP48 packages only.

Fig 1. Logic symbol



Pin numbers are shown for SSOP48 and TSSOP48 packages only.

Fig 2. IEC logic symbol

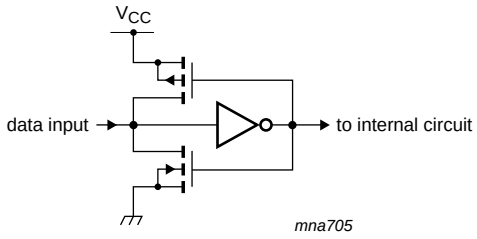


Fig 3. Bus hold circuit

5. Pinning information

5.1 Pinning

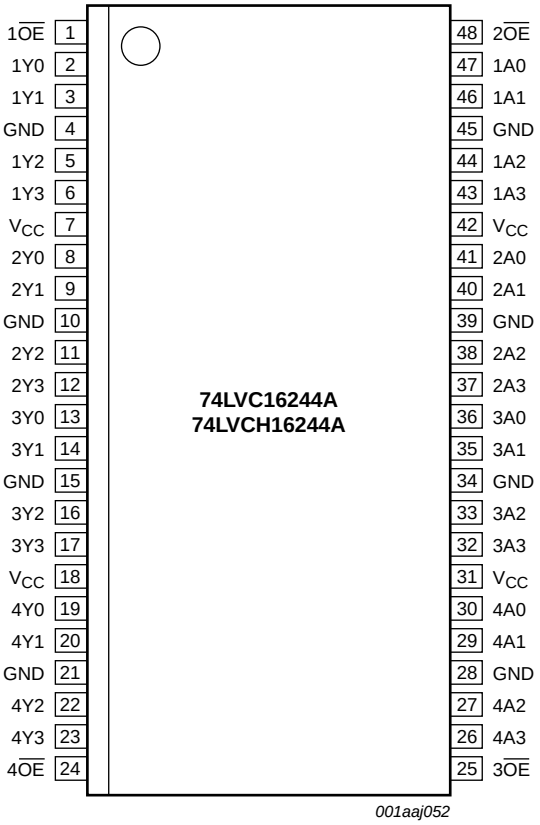
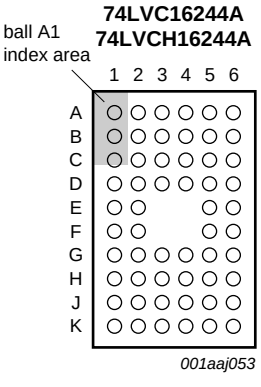
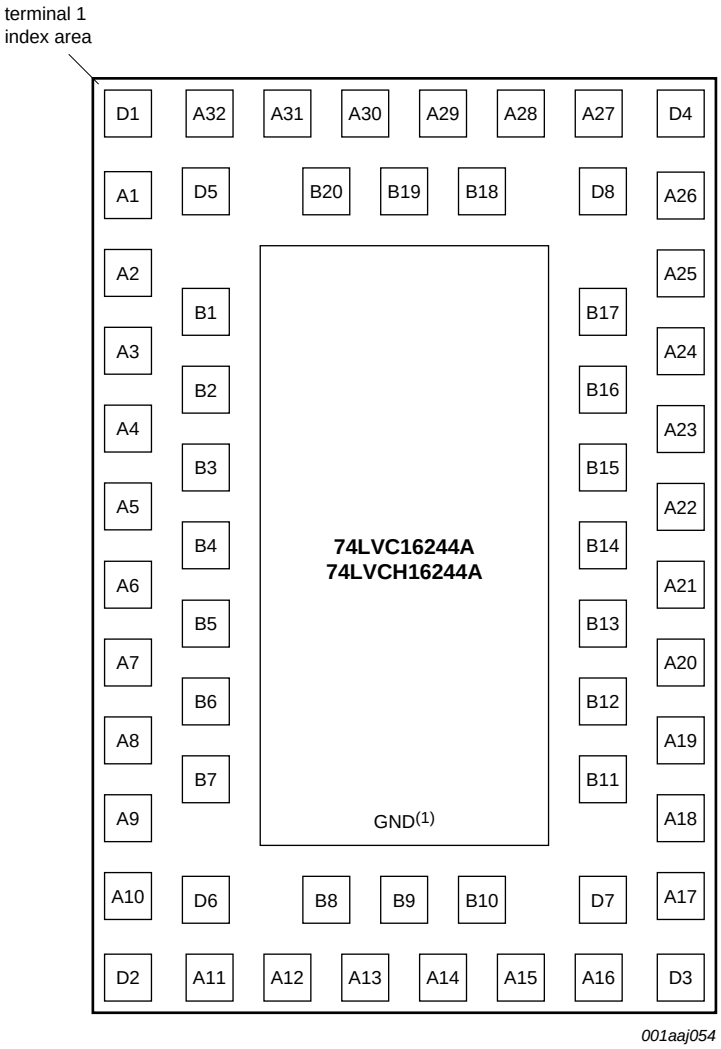


Fig 4. Pin configuration SOT370-1 (SSOP48) and SOT362-1 (TSSOP48)



Transparent top view

Fig 5. Pin configuration SOT702-1 (VFBGA56)



Transparent top view

(1) This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad however if it is soldered the solder land should remain floating or be connected to GND.

Fig 6. Pin configuration SOT1134-1 (HXQFN60U)

5.2 Pin description

Table 2. Pin description

Symbol	Pin			Description
	SOT370-1 and SOT362-1	SOT702-1	SOT1134-1	
1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$	1, 48, 25, 24	A1, A6, K6, K1	A30, A29, A14, A13	output enable input (active LOW)
1Y0 to 1Y3	2, 3, 5, 6	B2, B1, C2, C1	B20, A31, D5, D1	data output
2Y0 to 2Y3	8, 9, 11, 12	D2, D1, E2, E1	A2, B2, B3, A5	data output
3Y0 to 3Y3	13, 14, 16, 17	F1, F2, G1, G2	A6, B5, B6, A9	data output
4Y0 to 4Y3	19, 20, 22, 23	H1, H2, J1, J2	D2, D6, A12, B8	data output
GND	4, 10, 15, 21, 28, 34, 39, 45	B3, B4, D3, D4, G3, G4, J3, J4	A32, A3, A8, A11, A16, A19, A24, A27	ground (0 V)
V_{CC}	7, 18, 31, 42	C3, C4, H3, H4	A1, A10, A17, A26	supply voltage
1A0 to 1A3	47, 46, 44, 43	B5, B6, C5, C6	B18, A28, D8, D4	data input
2A0 to 2A3	41, 40, 38, 37	D5, D6, E5, E6	A25, B16, B15, A22	data input
3A0 to 3A3	36, 35, 33, 32	F6, F5, G6, G5	A21, B13, B12, A18	data input
4A0 to 4A3	30, 29, 27, 26	H6, H5, J6, J5	D3, D7, A15, B10	data input
n.c.	-	A2, A3, A4, A5, K2, K3, K4, K5	A4, A7, A20, A23, B1, B4, B7, B9, B11, B14, B17, B19	not connected

6. Functional description

Table 3. Function table[1]

Control	Input	Output
n$\overline{OE}$	**nAn**	**nYn**
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW	[2]	–0.5	V_{CC} + 0.5	V
		output 3-state	[2]	–0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C;				
		(T)SSOP48 package	[3]	-	500	mW
		VFBGA56 package	[4]	-	1000	mW
		HXQFN60U package	[4]	-	1000	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

[4] Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
		functional	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.2 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	0.65 × V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = –100 μA; V_{CC} = 1.65 V to 3.6 V	V_{CC} – 0.2	-	-	V_{CC} – 0.3	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 μA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I_{OZ}	OFF-state output current [2]	V_I = V_{IH} or V_{IL}; V_{CC} = 3.6 V; V_O = 5.5 V or GND;	-	±0.1	±5	-	±20	μA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	±0.1	±10	-	±20	μA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.1	20	-	80	μA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V; I_O = 0 A	-	5	500	-	5000	μA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	5.0	-	-	-	pF
I_{BHL}	bus hold LOW current [3][4]	V_{CC} = 1.65; V_I = 0.58 V	10	-	-	10	-	μA
		V_{CC} = 2.3; V_I = 0.7 V	30	-	-	25	-	μA
		V_{CC} = 3.0; V_I = 0.8 V	75	-	-	60	-	μA

Table 6. Static characteristics *...continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{BHH}	bus hold HIGH current [3][4]	V_{CC} = 1.65; V_I = 1.07 V	–10	-	-	–10	-	µA
		V_{CC} = 2.3; V_I = 1.7 V	–30	-	-	–25	-	µA
		V_{CC} = 3.0; V_I = 2.0 V	–75	-	-	–60	-	µA
I_{BHLO}	bus hold LOW overdrive current [3][5]	V_{CC} = 1.95 V	200	-	-	200	-	µA
		V_{CC} = 2.7 V	300	-	-	300	-	µA
		V_{CC} = 3.6 V	500	-	-	500	-	µA
I_{BHHO}	bus hold HIGH overdrive current [3][5]	V_{CC} = 1.95 V	–200	-	-	–200	-	µA
		V_{CC} = 2.7 V	–300	-	-	–300	-	µA
		V_{CC} = 3.6 V	–500	-	-	–500	-	µA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] The bus hold circuit is switched off when $V_I > V_{CC}$ allowing 5.5 V on the input terminal.

[3] Valid for data inputs only. Control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data input holds the input below the specified V_I level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 9.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	
t_{pd}	propagation delay	nAn to nYn; see Figure 7	[1]						
		V_{CC} = 1.2 V		-	11.0	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		1.5	4.8	10.7	1.5	11.3	ns
		V_{CC} = 2.3 V to 2.7 V		1.0	2.6	5.3	1.0	5.9	ns
		V_{CC} = 2.7 V		1.0	2.6	4.7	1.0	6.0	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.1	2.2	4.1	1.1	5.5	ns
t_{en}	enable time	$n\overline{OE}$ to nYn; see Figure 8	[1]						
		V_{CC} = 1.2 V		-	15.0	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		1.5	6.2	12.1	1.5	12.7	ns
		V_{CC} = 2.3 V to 2.7 V		1.0	3.5	6.4	1.0	7.1	ns
		V_{CC} = 2.7 V		1.0	3.3	5.8	1.0	7.5	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	2.8	4.6	1.0	6.0	ns
t_{dis}	disable time	$n\overline{OE}$ to nYn; see Figure 8	[1]						
		V_{CC} = 1.2 V		-	10.0	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		2.5	4.4	8.7	2.5	9.4	ns
		V_{CC} = 2.3 V to 2.7 V		1.0	2.4	4.9	1.0	5.3	ns
		V_{CC} = 2.7 V		1.0	3.2	6.2	1.0	8.0	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.8	3.1	5.2	1.8	6.5	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 9.

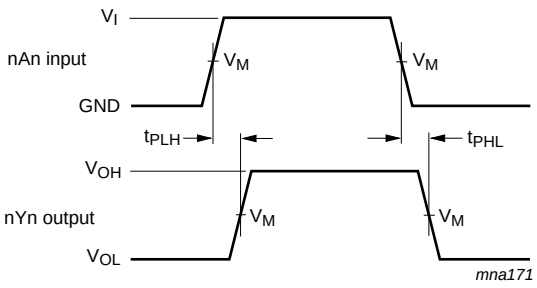
Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
C_{PD}	power dissipation capacitance	per input; V_I = GND to V_{CC} [3]						
		V_{CC} = 1.65 V to 1.95 V	-	4.8	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	8.3	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	11.4	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

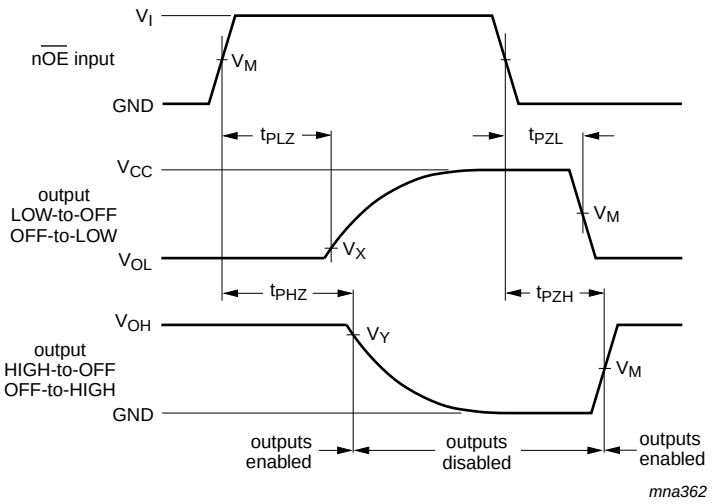
11. Waveforms



Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The input (nAn) to output (nYn) propagation delays



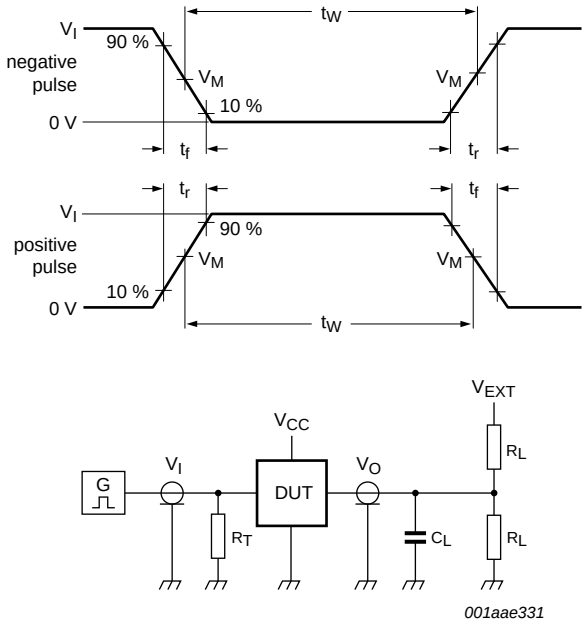
Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. 3-state enable and disable times.

Table 8. Measurement points

Supply voltage	V_M	Input			
V_{CC}		V_I	$t_r = t_f$	V_X	V_Y
1.2 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns	V_{OL} + 0.15 V	V_{OH} − 0.15 V
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.7 V	1.5 V	2.7 V	≤ 2.5 ns	V_{OL} + 0.3 V	V_{OH} − 0.3 V
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

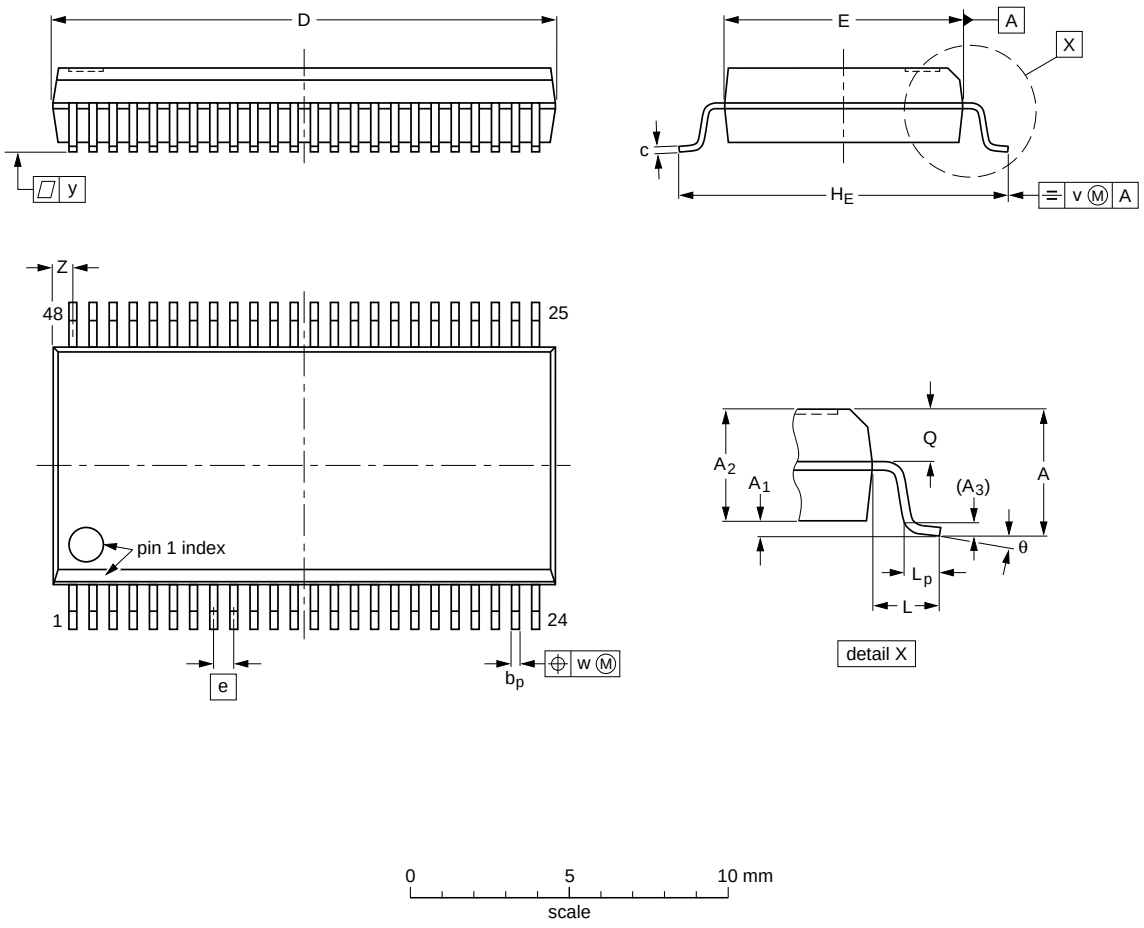
Fig 9. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

12. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

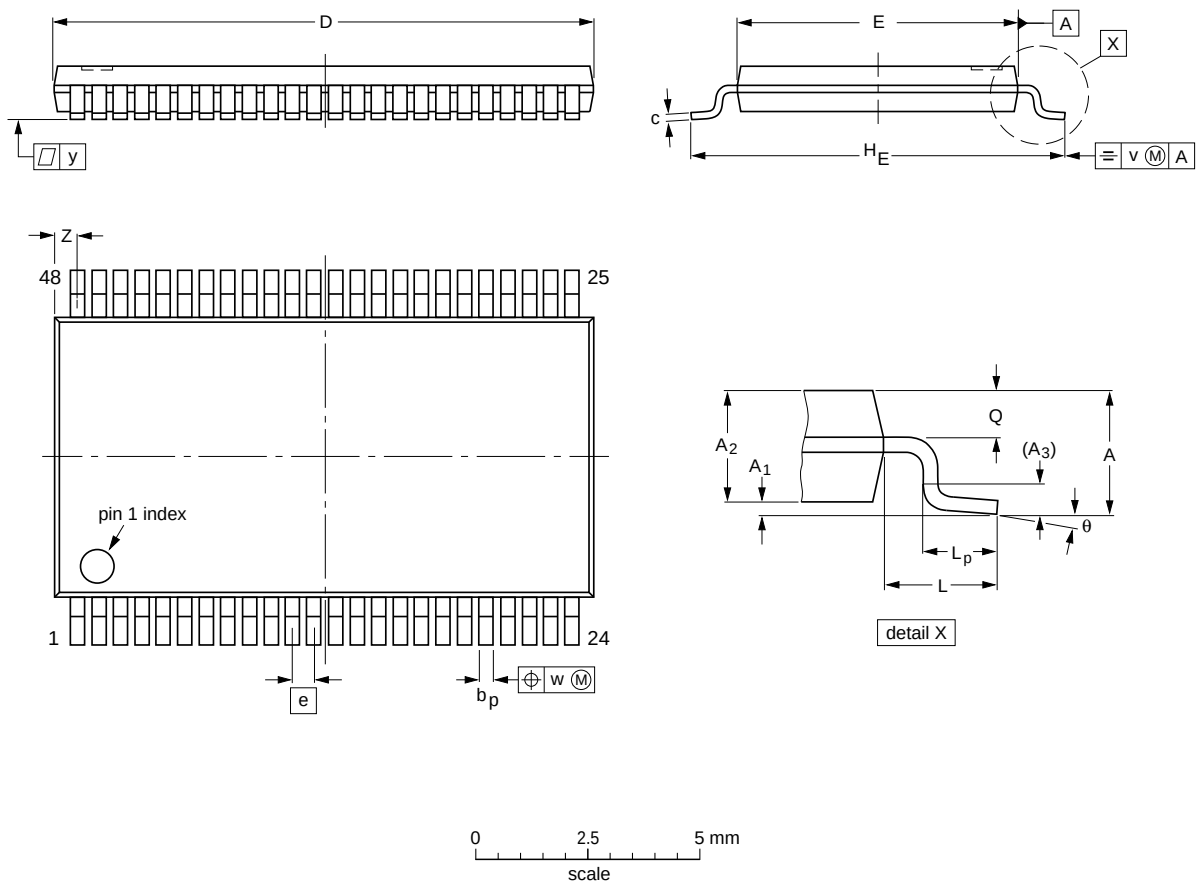
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

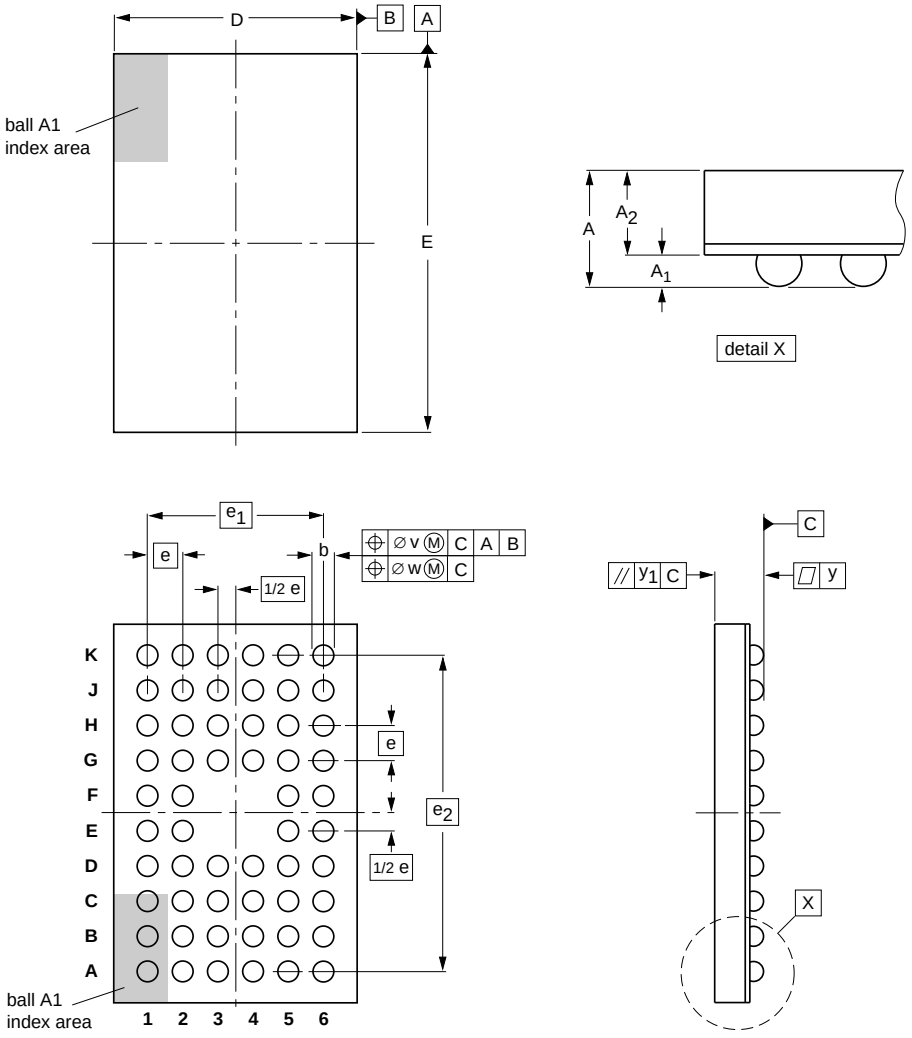
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

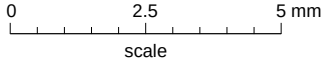
Fig 11. Package outline SOT362-1 (TSSOP48)

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm **SOT702-1**



DIMENSIONS (mm are the original dimensions)

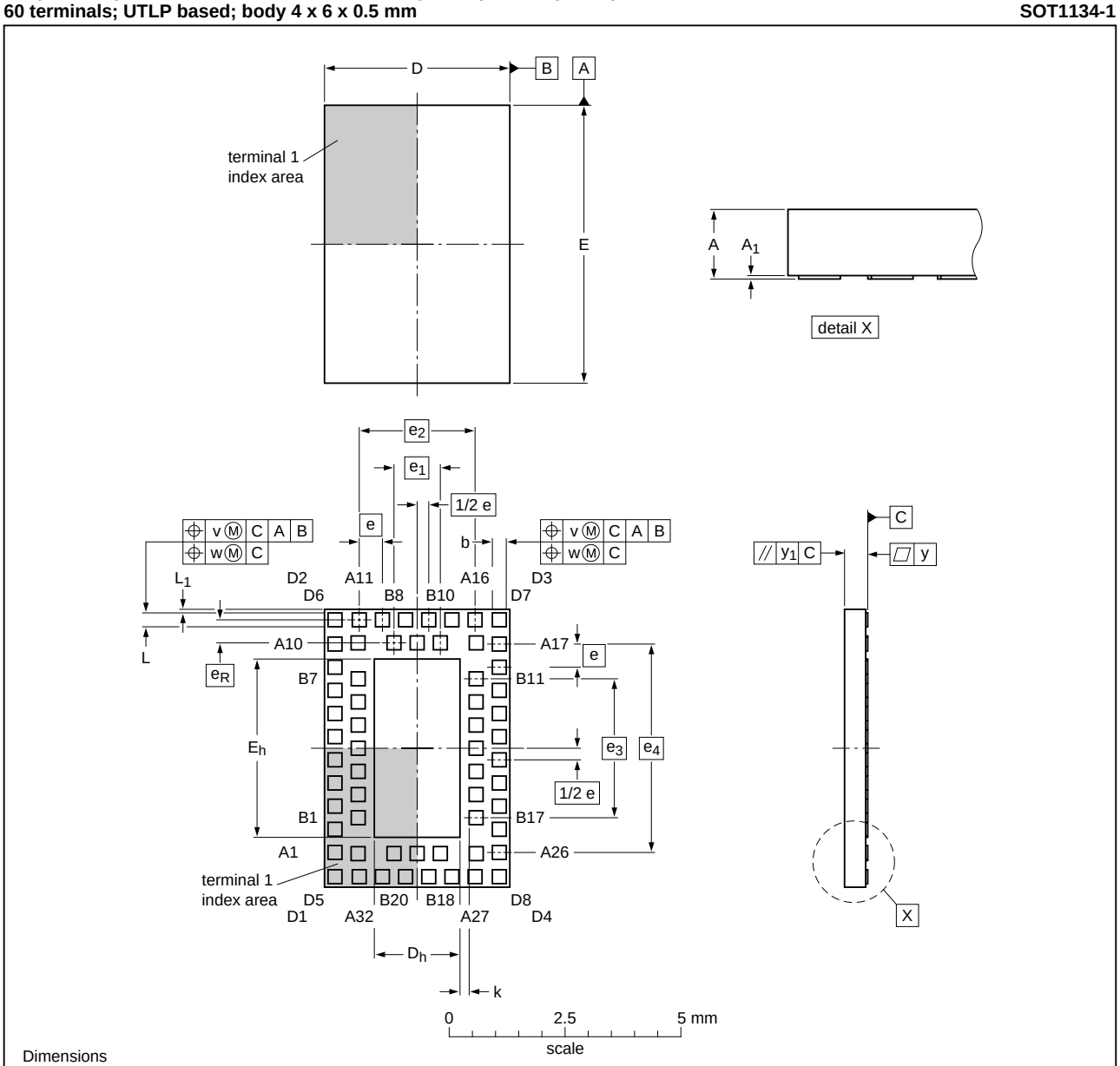
UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1	0.3 0.2	0.7 0.6	0.45 0.35	4.6 4.4	7.1 6.9	0.65	3.25	5.85	0.15	0.08	0.08	0.1



OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT702-1		MO-225				~~02-08-08~~ 03-07-01

Fig 12. Package outline SOT702-1 (VFBGA56)

HXQFN60U: plastic thermal enhanced extremely thin quad flat package; no leads; 60 terminals; UTLP based; body 4 x 6 x 0.5 mm **SOT1134-1**



Dimensions

Unit		A	A_1	b	D	D_h	E	E_h	e	e_1	e_2	e_3	e_4	eR	k	L	L_1	v	w	y	y_1
mm	max	0.50	0.05	0.35	4.1	1.90	6.1	3.90							0.25	0.35	0.125				
	nom	0.48	0.02	0.30	4.0	1.85	6.0	3.85	0.5	1	2.5	3	4.5	0.5	0.20	0.30	0.075	0.07	0.05	0.08	0.1
	min	0.46	0.00	0.25	3.9	1.80	5.9	3.80							0.15	0.25	0.025				

sot1134-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1134-1	- - -	- - -	- - -			~~08-12-17~~ 09-01-22

Fig 13. Package outline SOT1134-1 (HXQFN60U)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH16244A v.11	20111027	Product data sheet	-	74LVC_LVCH16244A v.10
Modifications:	• Table 4, Table 5, Table 6, Table 7, and Table 9: values added for lower voltage ranges.			
74LVC_LVCH16244A v.10	20110429	Product data sheet	-	74LVC_LVCH16244A v.9
Modifications:	• type numbers 74LVC16244ABQ and 74LVCH16244ABQ changed to 74LVC16244ABX and 74LVCH16244ABX. • Figure 6: figure note 1 changed.			
74LVC_LVCH16244A v.9	20100318	Product data sheet	-	74LVC_LVCH16244A v.8
74LVC_LVCH16244A v.8	20081117	Product data sheet	-	74LVC_LVCH16244A v.7
74LVC_LVCH16244A v.7	20031208	Product specification	-	74LVC_LVCH16244A v.6
74LVC_LVCH16244A v.6	20030130	Product specification	-	74LVC_LVCH16244A v.5
74LVC_LVCH16244A v.5	20021030	Product specification	-	74LVC_H16244A v.4
74LVC_H16244A v.4	19971028	Product specification	-	74LVC16244A_ 74LVCH16244A v.3
74LVC16244A_ 74LVCH16244A v.3	19971028	Product specification	-	74LVC16244A v.2
74LVC16244A v.2	19970630	Product specification	-	74LVC16244A v.1
74LVC16244A v.1	-	-	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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