Complete 12-Bit A/D Converters with Programmable Gain

AD368/AD369

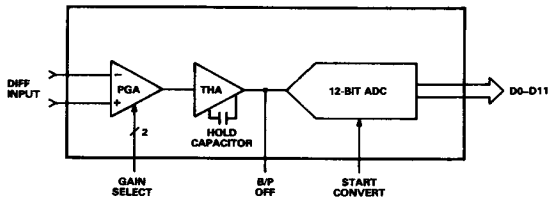
FEATURES

- **Low Cost Data Acquisition Systems Including:**
  - **Programmable Gain Instrumentation Amplifier**
  - **Track-and-Hold Amplifier**
  - **12-Bit A/D Converter**
- **Digitally Controlled Gains:**
  - **AD368 Gains = 1, 8, 64, 512**
  - **AD369 Gains = 1, 10, 100, 500**
- **50kHz Throughput Rate**
- **Small Size: 28-Pin Hermetic Double DIP**
- **Guaranteed No Missing Codes Over Specified Temperature**
- **True 12-Bit Linear; Error ≤1/2LSB (B-Grade)**
- **Unipolar or Bipolar Operation**
- **MIL-STD-883B Screening Available**

APPLICATIONS

- **Microprocessor Based Data Acquisition**
- **Wide Dynamic Range Measurement Systems**
- **Analytic and Medical Instruments**
- **Multichannel Systems With High/Low Level Signals**

AD368/AD369 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD368/AD369 are low cost, wide dynamic range data acquisition systems which condition and subsequently convert an analog signal into a 12-bit digital word. They include a programmable gain amplifier, a track-and-hold amplifier, and a 12-bit analog-to-digital converter – all in a 28-pin dual in-line package.

The digitally programmable-gain amplifier (PGA) of the AD368 enables the user to select binary-based gains of 1, 8, 64, and 512. These gain steps are especially useful in extending system dynamic range in DSP applications. The PGA of the AD369, with gains of 1, 10, 100, and 500, allows the user to choose full-scale input voltage ranges of 10V, 1V, 100mV, and 20mV, respectively. In addition, the precision differential input of the PGA provides the AD368/AD369 with excellent common-mode rejection.

The track-and-hold amplifier (T/H) features excellent linearity, low noise, and an internal hold capacitor.

The successive approximation analog-to-digital converter (ADC) features true 12-bit operation, with 0.012% max nonlinearity (B-grade). The user can select bipolar or unipolar operation to digitize both ac and dc input signals.

The AD368/AD369 provide a completely specified (industrial and military temperature ranges) and tested function in a space saving 28-pin hermetic package for system designers with cost, space, and time constraints.

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ORDERING GUIDE

Model	Monotonic Temperature Range 10 Bits	Monotonic Temperature Range 12 Bits	Offset Temperature Drift	Units
AD368AD		−25°C to +85°C	25 + 0.2 × G	mV
AD368BD		−25°C to +85°C	10 + 0.1 × G	mV
AD368SD	−55°C to +125°C	−55°C to +85°C	25 + 0.2 × G	mV
AD369AD		−25°C to +85°C	25 + 0.2 × G	mV
AD369BD		−25°C to +85°C	10 + 0.1 × G	mV
AD369SD	−55°C to +125°C	−55°C to +125°C	25 + 0.2 × G	mV

SPECIFICATIONS (typical @ +25°C, V_S = ±15V, +5V, R_{SPAN} = 63Ω and R(B/P) = 31Ω unless otherwise noted)

Parameter	AD368AD/SD AD369AD/SD Min	Typ	Max	AD368BD AD369BD Min	Typ	Max	Units
ANALOG INPUT							
Voltage Range, Unipolar (G = 1)	0		+10	*		*	V
Voltage Range, Bipolar (G = 1)	−5		+5	*		*	V
Common-Mode Voltage		12 − (V_{DIFF} × G/2)			*		V
Resistance		10^9			*		Ω
Capacitance		5			*		pF
Bias Current (I_B)		10	50		*	25	nA
I_B vs. Temperature		50			*		pA/°C
Input Offset Current (I_{OS})		2	20		*	10	nA
I_{OS} vs. Temperature		20			*		pA/°C
Noise Current (0.1 to 10Hz)		60			*		pA p-p
Output Offset Voltage (V_{OS})[1]		5 + 0.02 × G	25 + 0.2 × G		*	10 + 0.1 × G	mV
V_{OS} vs. Temperature		70 + 0.2 × G	300 + 2.0 × G		*	*	μV/°C
V_{OS} vs. Common-Mode Voltage[2]		60 + 0.5 × G	320 + 3.2 × G		*	150 + 1.5 × G	μV/V
V_{OS} vs. Supply Voltage[3]		100 + 1.0 × G	2300 + 10 × G		*	1000 + 4 × G	μV/V
Output Noise Voltage (rms)							
G = 1		250			*		μV
G = 8, 10		260			*		μV
G = 64, 100		340			*		μV
G = 512, 500		600			*		μV
DIGITAL INPUTS[4]							
V_{IH}	3.0		V_{CC}	*		*	V
V_{IL}	0.0		0.8	*		*	V
I_{IH}, I_{IL}		0.01	1.0		*	*	μA
C/S Pulse Width	50			*			ns
DIGITAL OUTPUTS, 12-BIT PARALLEL							
V_{OH} @ I_{OH} = −40μA	3.6	5.0		*	*		V
V_{OL} @ I_{OL} = 1.6mA		0.2	0.4		*	*	V
SIGNAL DYNAMICS							
Conversion Time (t_C)		12	15		*	*	μs
t_C vs. Temperature		−10			*		ns/°C
System Throughput Rate[5]							
G = 1, 8, 10			50			*	kHz
G = 64, 100			50			*	kHz
G = 512, 500			20			*	kHz
Gain Switching Time		1.5	2.0		*	*	μs
PGA Settling Time (to 1/2LSB)							
G = 1, 8, 10		8	10		*	*	μs
G = 64, 100		12	15		*	*	μs
G = 512, 500		40	50		*	*	μs
Amplifier − 3dB Bandwidth							
G = 1		1000			*		kHz
G = 8, 10		400			*		kHz
G = 64, 100		150			*		kHz
G = 512, 500		40			*		kHz
T/$\overline{H}$ Acquisition Time (t_{ACQ} to 1/2LSB)			3			*	μs
T/$\overline{H}$ Aperture Delay Time (t_{AP})		140	250		*	*	ns
t_{AP} vs. Temperature		−0.3			*		ns/°C
Aperture Jitter		1			*		ns
ACCURACY							
Integral Nonlinearity		0.30	0.75		*	0.5	LSB
Differential Nonlinearity (DNL)[6]		0.30	0.90		*	0.5	LSB
Gain Error @ G = 1		0.05	0.5		*	0.2	%
@ Other Gains Referred to G = 1[7]		0.01	0.1		*	0.05	%
Gain vs. Temperature @ G = 1		3	30		*	*	ppm/°C
@ Other Gains Referred to G = 1		3	10		*	*	ppm/°C
Gain vs. Supply Voltage							
V_P ± 10%		10	30		*	*	ppm/%
V_N ± 10%		5	30		*	*	ppm/%
V_{CC} ± 10%		5	15		*	*	ppm/%

Parameter	AD368AD/SD AD369AD/SD Min	Typ	Max	AD368BD AD369BD Min	Typ	Max	Units
MONOTONIC TEMPERATURE RANGE							
12 Bits	−25		+85	−25		+85	°C
	−55 (S Grade)		+85 (S Grade)				°C
10 Bits	−55 (S Grade)		+125 (S Grade)				°C
REFERENCE							
Voltage (V_{REF})	6.28	6.30	6.32	*	*	*	V
V_{REF} vs. Temperature			20			*	ppm/°C
Internal Resistance		2			*		Ω
External Load			0.5			*	mA
POWER REQUIREMENTS							
Positive Supply Range	+13.5	15	16.5	*	*	*	V
Negative Supply Range	−13.5	−15	−16.5	*	*	*	V
Logic Supply Range	4.5	5.0	5.5	*	*	*	V
Supply Current, V_{IN} = 10V, f_C = 50kHz							
+15V		15	20		*	*	mA
−15V		30	40	*	*		mA
+5V		20	35		*	*	mA
Power Consumption		775			*		mW
THERMAL RESISTANCE (J-A)		25			*		°C/W
PACKAGE OPTION[8]							
DH-28A		AD368AD/SD AD369AD/SD			AD368BD AD369BD		

NOTES
*Same specifications as A Grade.
[1]Offset voltage applies to both bipolar and unipolar operating modes.
[2]V_{CM} = ±10V.
[3]V_S = ±10%.
[4]For digital inputs, pull-up resistors needed (typ 5kΩ) when interfacing with TTL/DTL logic.
[5]Assumes pipelining, i.e., signal is inputted to I.A. when T/H goes into hold mode, allowing voltage to settle concurrently with A/D conversion (see timing diagram).
[6]Includes T/H droop rate.
[7]This is gain error (% FS) after error at G = 1 is cancelled by adjustment. Without adjustment, total error becomes: E(Total) = E(G = 1) + E(G = 8/10, 64/100, or 512/500).
[8]See Section 14 for package outline information.
Specifications subject to change without notice.

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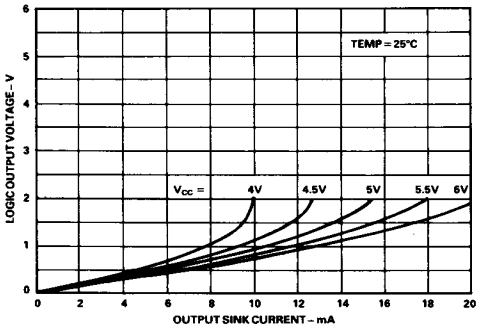
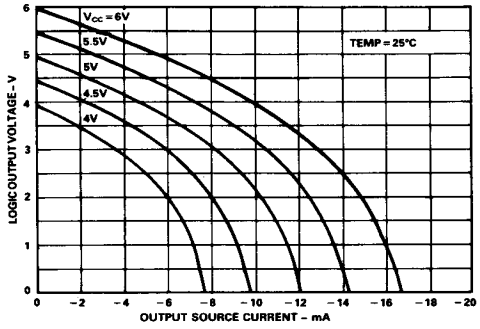
ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Positive Supply, V_P	−0.3	+17	V
Negative Supply, V_N	+0.3	−17	V
Digital-to-Analog Ground	−1	+1	V
Logic Supply	−0.3	+7	V
Analog Input (Either)	V_N	V_P	V
Analog Input Current	−10	+10	mA
Lead Soldering, 10 sec		+300	°C
Storage Temperature	−65	+150	°C

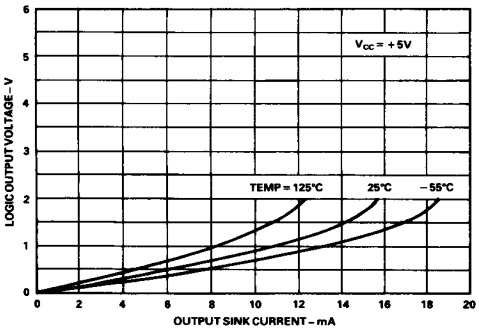
LOGIC OUTPUTS TYPICAL PERFORMANCE GRAPHS



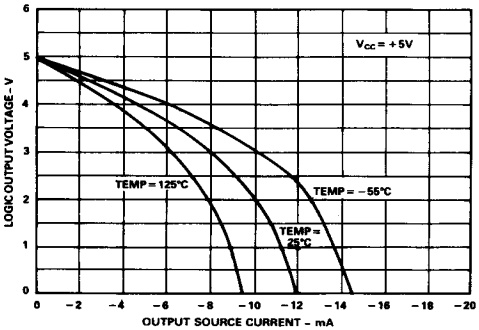
Logic Low Level Output Voltage vs. Sink Current



Logic High Level Output Voltage vs. Source Current

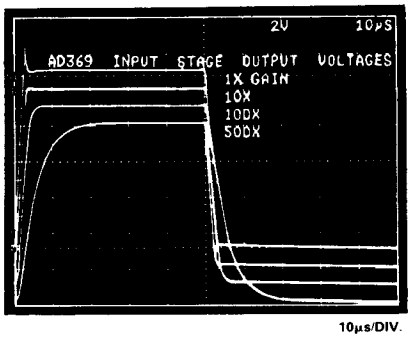


Logic Low Level Output Voltage vs. Sink Current

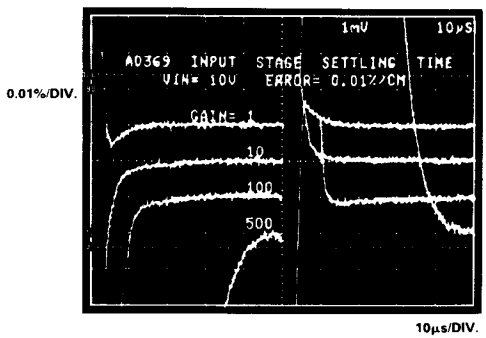


Logic High Level Output Voltage vs. Source Current

AMPLIFIER LARGE SIGNAL RESPONSE



AD369 Input Stage Output Voltage



AD369 Input Stage Settling Time

ANALOG INPUT

An analog multiplexer and resistor network form the gain switching circuit of the PGA. As shown in Table I, the user selects a gain according to the state of binary address inputs G0 and G1.

Also shown in the table is the input range data. The full-scale range of the DAS is 10V, and an LSB value is 4.8μV/4.9μV in the gain 512/500 mode; therefore, the dynamic range of the AD368/AD369 is 126dB.

The PGA uses a monolithic instrumentation amplifier, which is based on the classic three-op-amp approach. The differential analog input is amplified, according to gain selection, by two input op amps. The third amplifier, a unity gain subtractor, removes any common-mode signal and yields a single-ended output.

DATA CONVERSION

The track-and-hold amplifier is a monolithic device with an internal hold capacitor. It has an acquisition time of ≤3μs.

Input signals are digitized using a successive-approximation A/D converter. The rising (L to H) edge of the Convert Start pulse resets the internal flip-flops of the SAR. The falling (H to L) edge of the pulse initiates the conversion. After an aperture delay of 230ns, the track and hold amplifier goes into the hold mode, and the Status output goes High, indicating a conversion is in progress. Conversion time from the falling edge of the CS pulse is 15μs, maximum. A low output on the Status line indicates that the conversion is complete. The data at the output is valid at least 15ns before the Status goes low (see timing diagram). This gives sufficient setup time so that data may be latched to an external register on the falling edge of the Status pulse. The T/H amplifier returns to the tracking mode when the Status line goes low. Data is valid at the output until the next falling edge of a C/S pulse. After a maximum of 3μs acquisition time, a new C/S pulse may be issued to begin a new conversion. Timing diagrams are shown in Figure 1.

Figure 1a shows timing when a conversion sequence has first begun. All functions are being performed in series. This is the timing for the first data conversion, assuming a new gain must be selected.

The timing in Figure 1b assumes conversions are progressing continuously. After a conversion has been initiated by the falling edge of the C/S pulse, a new analog signal may be inputted to the DAS or a new gain may be selected. The figure shows that if a new gain is selected, no more than 2μs later, the new voltage begins settling at the PGA output. In the G = 512/500 mode, the determining factor for conversion speed is the amplifier settling time and, if necessary, the gain switching time. If the PGA gain is not switched, the conversion time for G = 512/500 becomes 50μs, maximum, and a minimum throughput rate of 20kHz can be achieved.

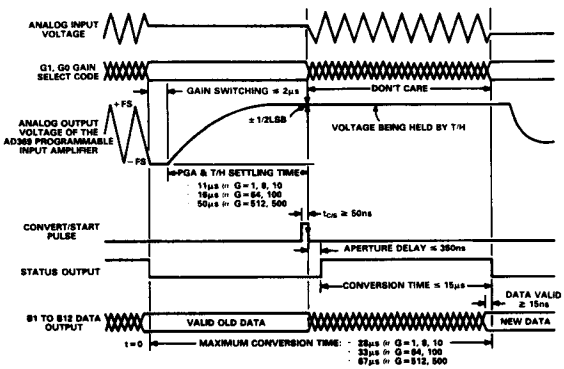


Figure 1a. AD368/AD369 Timing Diagram Without Pipelining

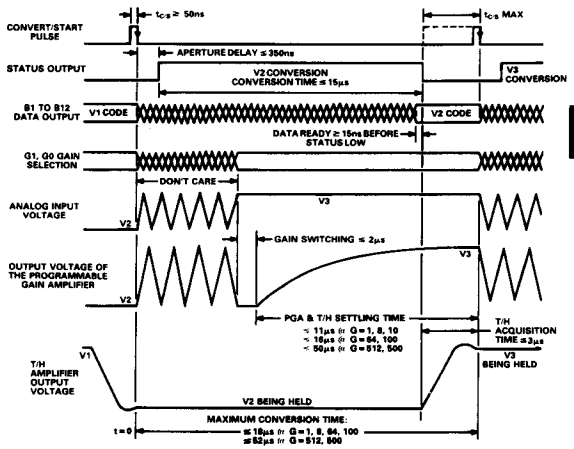


Figure 1b. AD368/AD369 Timing Diagram With Pipelining

Gain Code G1	Gain Code G0	Programmable Gain Amplifier Gain	Analog Input Voltage Range	Unipolar	Bipolar		One Least Significant Bit (LSB) Value
0	0	1	0	+10V	−5V	+5V	2.44mV
0	1	8, 10	0	+1.25V, +1V	−0.625V, −0.5V	+0.625V, +0.5V	0.31mV, 0.24mV
1	0	64, 100	0	+156mV, +100mV	−78mV, −50mV	+78mV, +50mV	38μV, 24μV
1	1	512, 500	0	+19.5mV, +20mV	−9.75mV, −10mV	+9.75mV, +10mV	4.8μV, 4.9μV

Table I. Input Voltage Range Selection

CALIBRATING THE AD368/AD369 WITH TRIMPOTS

This is a calibration procedure which is implemented with potentiometers, resistors, and LEDs. The hardware can be incorporated on the board which utilizes the AD368/AD369 for convenient field calibration.

The ideal transfer function of the AD368/AD369 in Figure 2 shows that the output code steps up from all ones to all zeros as the analog input voltage increases from the minus full scale limit to the plus full scale limit. The purpose of the calibration is to put the first and last bit transitions where they belong; 1LSB above −FS and 1LSB below +FS respectively.

The transfer function shows that for each output code there is an associated quantization uncertainty of 1LSB. For a given code, there is an LSB wide range of possible analog input voltages. Only at the transition point between two adjacent codes is there a precise correlation between input voltage and digital output. This circumstance must be utilized in the calibration or the accuracy may be off by ±1/2LSB.

In reality, due to noise on the analog input, the transitions do not occur as sharply as illustrated in the figure. When changing codes, the output will toggle constantly while moving from one value to the next. The desired transition point is obtained when 50% of the time the output is above this point and 50% of the time the output is below it. This transition point may be observed on an oscilloscope. Another way to measure this 50% duty cycle is by using a light emitting diode (LED) as shown in Figure 3. The duty cycle is approximately 50% when the LED is about halfway between minimum and maximum brightness.

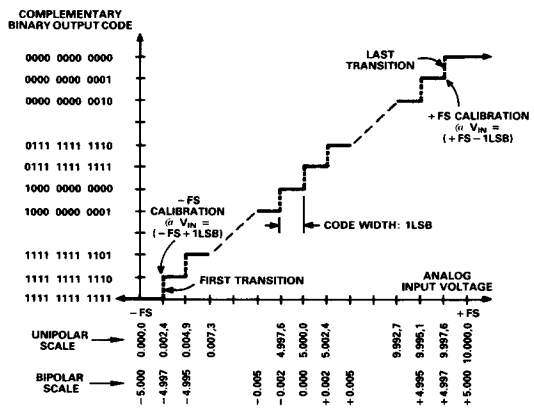


Figure 2. AD368/AD369 Transfer Function

UNIPOLAR MODE CALIBRATION

Figure 3 shows the AD368/AD369 in the unipolar mode of operation, with calibration hardware connected. The calibration begins with cancellation of the input stage offset by applying 0V to the input and manipulating R_{RTI} and R_{RTO} until the first transition occurs exactly at 0V, regardless of the amplifier gain. The next step in the calibration is to cancel the output stage offset by adjusting R_{RTO} to put the first transition at the proper input voltage of +1LSB. Finally, R_{SPAN} is adjusted and the last bit transition is put 1LSB below +FS.

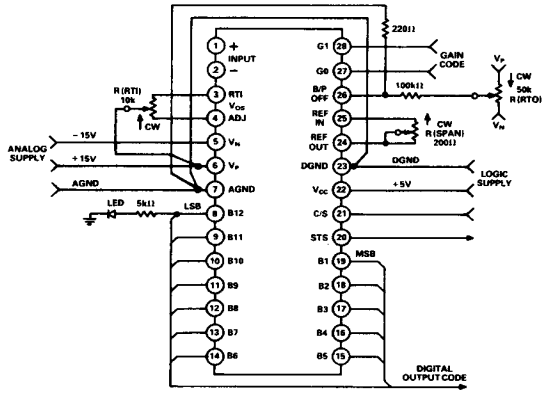


Figure 3. AD368/AD369 in the Unipolar Mode with RTI V_{OS}, RTO V_{OS} and Span Trimpots

Calibration steps for input stage offset voltage (V_{OS}) cancellation:

1. Connect the inputs to analog ground.
2. Set G=512/500 and turn R_{RTI} all the way clockwise (CW). This shifts the transfer function to the right, causing the output code to be all ones. The LED will light up.
3. Now turn R_{RTI} counterclockwise (CCW) until the LED dims to half brightness. The first transition is now positioned at the $V_{IN}=0$ line.
4. Switch to G=1 and turn R_{RTO} all the way CW. This will cause the output code to be all ones again.
5. Turn R_{RTO} CCW until the LED dims; the first transition is at 0V again.
6. Switch the gain to G=512/500, turn R_{RTI} CW just enough to assure an all ones code, then turn it CCW until the LED dims to half brightness.
7. Switch the gain back to one, turn R_{RTO} CW enough to assure an all ones code, then turn it CCW until the LED dims.
8. Repeat steps 5 and 6 until the LED brightness does not change when switching between G=1 and G=512/500. The input stage offset voltage is now zero.

Calibration steps for the output stage offset voltage (V_{OS}) cancellation:

1. Connect the inputs to a 2.44mV supply, as in Figure 4.
2. Set G=1, turn R_{RTO} all the way CW, assuring an all ones output and lighting the LED.
3. Turn R_{RTO} CCW until the LED dims to half brightness. The first transition is now 1LSB above 0V.

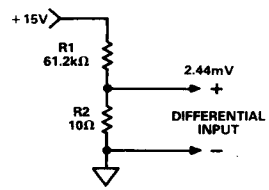


Figure 4. Input Connection for the R_{RTO} Calibration

Calibration steps for Gain Error (SPAN) cancellation:

1. Apply a precise 10V–2.44mV across the input of the AD368/AD369. A voltage divider as shown in Figure 5 can be employed; in conjunction with a precision voltmeter to verify an input of 9.997,56V.
2. Set G = 1, turn R_{SPAN} all the way CCW, assuring an output of all zeros.
3. Turn R_{SPAN} CW until the LED begins to light up (about half-brightness). At this point the last transition will be at +FS −1LSB.

The calibration in the unipolar mode is now complete.

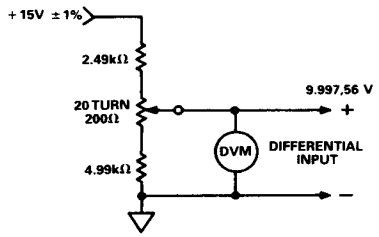


Figure 5. Input Connection for the R_{SPAN} Calibration

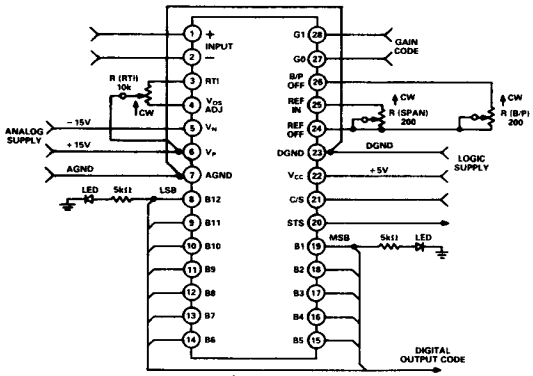


Figure 6. AD368/AD369 in the Bipolar Mode with Offset and Gain Trimpots

BIPOLAR MODE CALIBRATION

The AD368/AD369, with calibration hardware, are shown in Figure 6 for operation in the bipolar mode. The adjustments begin, as in the unipolar case, with the input stage V_{OS} cancellation. In this case however, the calibration is different because the 0V point is now at mid-scale; the MSB is used instead of the LSB. Next in the calibration is to adjust R_{RTO} and put the first LSB transition at an input voltage of −5V +1LSB. Last is the R_{SPAN} adjust to put the last bit transition 1LSB below +5V.

Input stage V_{OS} cancellation steps:

1. Connect the inputs to analog ground.
2. Select G = 512/500 and turn R_{RTI} until the MSB LED is at half-brightness.
3. Switch to G = 1 and adjust R_{RTO} until the LED is again at half-brightness.
4. Repeat steps 2. and 3. until the LED brightness does not change when gains are switched. This indicates that the input stage V_{OS} = 0V.

Output stage V_{OS} cancellation steps:

1. Set G = 1.
2. Connect the plus input to ground and the minus input to 4.997,56 volts using a voltage divider such as in Figure 7.
3. Turn R_{RTO} completely CW to assure an output code of all ones.
4. Now turn R_{RTO} CCW until the LSB LED dims to half-brightness. The first transition is now 1LSB above −FS.

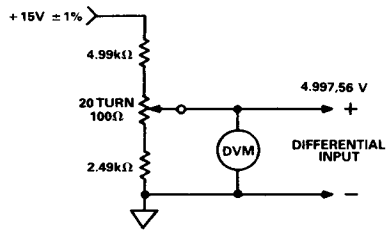


Figure 7. Voltage Divider to Derive RTO V_{OS} and Span Calibration Voltage

Gain Error cancellation steps:

1. Set G = 1.
2. Now connect the plus input to 4.997,56 Volts and the minus input to analog ground.
3. Turn R_{SPAN} completely CCW to assure an output code of all zeros.
4. Now turn R_{SPAN} CW until the LSB LED begins to light up. At this point the last bit transition will be at +FS −1LSB.

Calibration in the bipolar mode is now complete.

CALIBRATING THE AD368/AD369 WITHOUT TRIMPOTS

Figure 8 shows the AD368/AD369 in the unipolar mode with calibration hardware consisting of a Quad 8-Bit D/A Converter (AD7226) circuit instead of the previous trimpot configuration. The calibration procedure is basically the same as before except that instead of adjusting the potentiometers, three DACs are used to correct for offsets and gain error. Bipolar calibration may be accomplished by referring to Figure 6.

This calibration routine has some excellent benefits in addition to the elimination of potentiometers. Dipswitches may be used initially to set the 8-bit word values needed for each connection; however, after the word values are determined, this data may be stored into a memory (i.e., RAM) for auto-calibration in the field. The entire calibration may be accomplished under microprocessor control. Temperature offsets may be cancelled by using a temperature sensor in conjunction with a microprocessor.

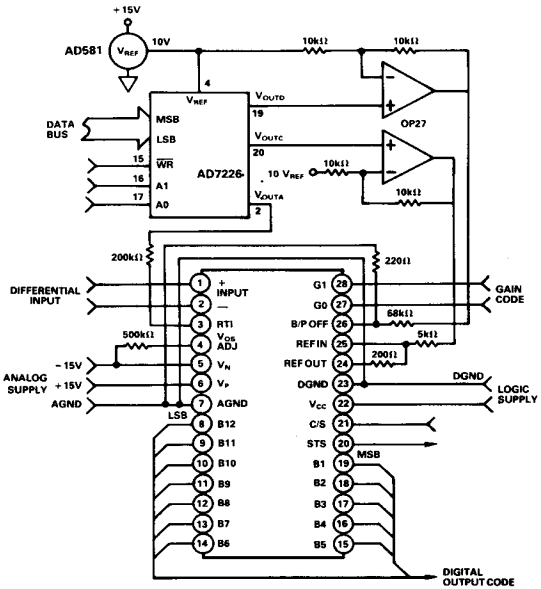


Figure 8. AD368/AD369 in the Unipolar Mode with D/A Circuit Replacing Trimpots

INPUT PROTECTION

There are two considerations when applying input protection for the PGA: 1) that maximum input current must be limited to less than 20mA and 2) that input voltages must not exceed the supplies. Outside the linear operating range, the input impedance of the AD368/AD369 becomes low and nonlinear due to the input transistors going into saturation. The graph in Figure 9 illustrates the input current vs. differential input voltage relationship without input protection.

Resistors of 1kΩ in series with each input would keep the currents within safe limits for input voltages in the range of $V_P = +15V$ to $V_N = -15V$. Figure 10 shows the external components necessary to protect the AD368/AD369 under all overload conditions at any gain. The diodes to the supplies are necessary if input voltages outside of the range of the supplies are encountered.

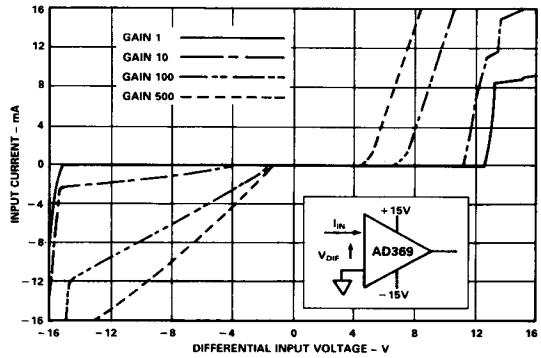


Figure 9. Input Current vs. Differential Input Voltage Without Input Protection

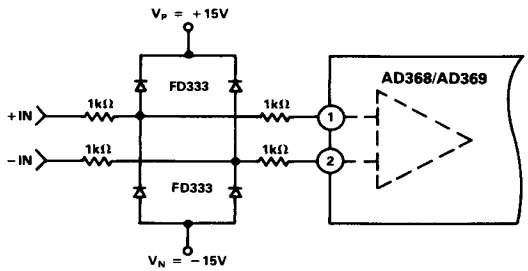


Figure 10. Input Protection Circuit for AD368/AD369

The equivalent noise resistance of the AD368/AD369 input stage is only 1kΩ. Input protection resistors, however, will quickly degrade this excellent noise performance. To reduce the noise encountered with added resistors, FETs may be used to limit the input current. FETs, such as the 2N4416, with low I_{DSS} and low on-resistance should be used. Figure 11 shows the protection circuit and Figure 12 shows the input current vs. the differential input voltage with the FET protection circuit. The 20kΩ resistor is put in series with the gate to limit the "reverse" I_{DSS} current and does not add to the noise.

The above input protection circuits also protect the AD368/AD369 in case there is a voltage applied to the input while the supplies are shut off.

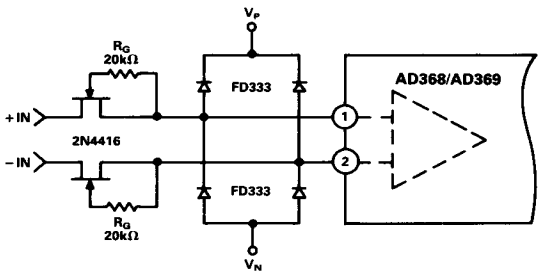


Figure 11. Low Noise Input Protection Circuit for AD368/AD369

If using multiplexers, proper device selection can provide AD368/AD369 input protection. Some MUXes limit the maximum current as well as the maximum output voltage to safe levels. Keep in mind that the on resistance of the MUX will add to the input stage noise.

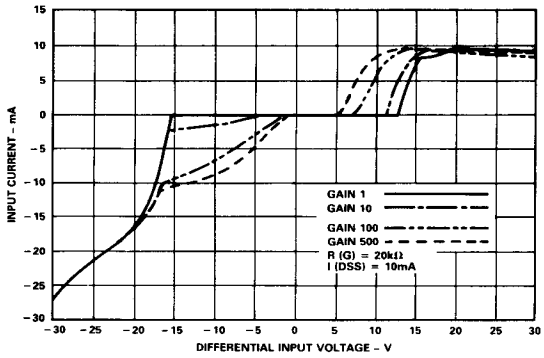


Figure 12. AD625 Input Protection with 2N4416 FETs and FD333 Clamping Diodes

GROUND RETURNS FOR INPUT BIAS CURRENTS

There must be a direct return path for the input bias currents of the PGA input transistors; otherwise, they will charge external capacitances, causing the output to drift uncontrollably or saturate. Therefore, when amplifying floating input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 13.

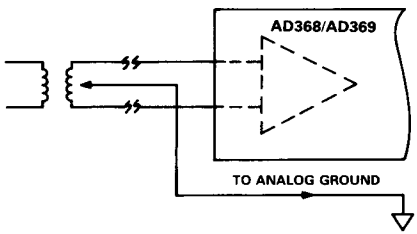


Figure 13a. Ground Returns for Bias Currents with Transformer Coupled Input

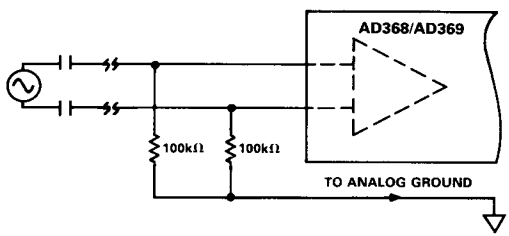


Figure 13b. Ground Returns for Bias Currents with ac Coupled Inputs

GROUND CONNECTIONS

The digital and analog ground pins of the AD368/AD369 should be tied together as close to the package as possible to avoid noise coupling from the digital ground to the analog circuit. When an application calls for separate grounding entirely, a 0.1μF capacitor should be connected between the AGND and DGND pins to filter out any noise.

POWER SUPPLY DECOUPLING

Each of the AD368/AD369 supply terminals should be capacitively decoupled as close to the IC as possible. A 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are decoupled to the analog ground pin and the Logic supply is decoupled to the digital ground pin.

TRACK-AND-HOLD ERRORS

The aperture delay time is the time required for the track-and-hold amplifier to switch from track to hold. Since this is effectively a constant, it may be tuned out by advancing the track-to-hold command with respect to the input signal.

Unlike the aperture delay time, aperture jitter is a true error source and must be considered. Aperture jitter is a result of noise within the switching network. It causes variations in the value of the analog input being held. The aperture error which results from this jitter is directly related to the dV/dT of the analog input and may limit the signal bandwidth. The aperture jitter of the T/H in the AD368/AD369, however, is small enough that the instrumentation amplifier will limit the signal frequency well below the frequency at which the jitter error would be of concern.

Droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major contributors are switch leakage current and bias current. This dV_{OUT}/dT is equal to the ratio of the total leakage current, I_l to the hold capacitance, C_H. The droop rate of the T/H in the AD368/AD369 is included in the differential nonlinearity specification.

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change. Care should be taken to assure that both input lines are balanced with regard to parasitic capacitances and source resistances; otherwise, the excellent common-mode rejection of the AD368/AD369 will be degraded.

ERRORS DUE TO BANDWIDTH LIMITATIONS OF THE AD368/AD369

When using the AD368/AD369 to digitize sine-wave signals, it is important to know the frequency at which the system response roll-off will cause an error of 1/2LSB.

The ratio of output to input voltage for the instrumentation amplifier of the AD368/AD369 is:

$$|V_O/V_I| = G/|(1+jf/f_a)| = G/[1+(f/f_a)^2]^{0.5}$$

where f_a equals the −3dB bandwidth and a single-pole roll-off is assumed.

It can be shown that the V_O/V_I ratio will have an error of 1/2LSB for a 12-bit A/D converter when:

$$f(1/2LSB) = f_a/\sqrt{2^{12}} = f_a/64.$$

The instrumentation amplifier will have reached the limit of 12-bit precision for signal frequencies of $f_s/64$. The frequency can be doubled at the expense of two bits of accuracy.

The frequency at which the amplitude of a 10V p-p sine wave is reduced by one half of an LSB is typically 10kHz, 3.5kHz, 1.7kHz, and 0.5kHz at gains of 1, 10, 100, and 500 respectively.

NOISE CONSIDERATIONS

Assuming normally distributed or white noise, the rms noise voltage E_n of a system is a function of its noise bandwidth BW_N. The correlation between −3dB bandwidth (BW) and BW_N is dependant upon the frequency response of the system under consideration.[1] For a 6dB/octave filter, the ratio is $\pi/2 = 1.57$. For a "brick wall" filter it is one. The noise correlation is simply: $E_N = e_N\sqrt{BW_N}$, where e_N is the noise density ($nV/\sqrt{Hz}$).

The noise of the input signal must also be added to the noise of the DAS. Again, in calculating the rms noise contribution of the signal, the BW_N of the source must be considered. If not filter limited before the AD368/AD369 input, the BW_N of the PGA, as stated above, must be used, which is about $\pi/2$ times its −3dB bandwidth.

Input protection resistors will also contribute to the total system noise. The rms noise voltage of a 1kΩ resistor over a noise bandwidth of 1Hz is 4nV. So, the noise voltage of a resistor, R(kΩ) and a noise bandwidth, BW_N(Hz) is: $E_N(R) = 4nV\sqrt{R \times BW_N}$.

The total system rms noise is given by the equation:

$$E_N(\text{system}) = \sqrt{E_N(AD369)^2 + [G \times E_N(R_{IN})]^2 + [G \times E_N(sig)]^2}$$

Once the system rms noise value is known, the probability of the peak-to-peak value of the noise exceeding an LSB is given in Table II.

LSB/E_N	Probability of Noise Exceeding 1LSB
1.0	62.0%
2.0	32.0%
3.0	13.0%
4.0	4.6%
5.0	1.2%
5.15	1.0%
6.0	0.27%
6.6	0.10%

Table II.

[1]See "Low Noise Electronic Design," by C. D. Motchenbacher, F. C. Fitchen.

OTHER CONSIDERATIONS

One of the more overlooked problems in designing ultra-low-drift dc amplifiers is thermocouple induced offset. In a circuit comprised of two dissimilar conductors (i.e., copper, kovar), a voltage known as the "Seebeck" or thermocouple emf is generated when the two junctions are at different temperatures. Standard IC lead material (kovar) and copper form a thermocouple with a high thermoelectric potential (about 35μV/°C). This means that care must be taken to insure that all connections in the input circuit of the AD368/AD369 remain isothermal. In addition, the user should also avoid air currents over the circuitry since slowly fluctuating thermocouple voltages will appear as "flicker" noise.

The base emitter junction of an input transistor can rectify out-of-band signals (i.e., RF interference). These rectified voltages act as small dc offset errors. In the case of a resistive transducer, a small capacitor (e.g. 150pF) across the input working against the internal resistance of the transducer may suffice to provide an RC filter without affecting system bandwidth. Again, every effort should be made to match the capacitance at Pins 1 and 2, to preserve CMR.