μP-Compatible 10-Bit High-Speed A/D Converter

ADC-910

FEATURES

- **Includes Clock, Reference, 3-State Buffered Outputs**
- **Fast Conversion Time 6μs**
- **Four Input Ranges . . +/−2.5V, +/−5.0V, +5.0V and +10.0V**
- **1/2 LSB INL**
- **No Missing Codes Over Temperature**
- **Low ESD Sensitivity Due to Rugged Bipolar Processing**
- **Software Programmable Unipolar/Bipolar**
- **Easily Interfaced to 8 and 16-Bit μP Bus**
- **Available in Die Form**

ORDERING INFORMATION†

PMI MODEL NO.	TEMPERATURE RANGE
ADC910AT*	−55°C/+125°C
ADC910BT*	
ADC910ET	−25°C/+85°C
ADC910FT	
ADC910GT	0°C/+70°C
ADC910HT	

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

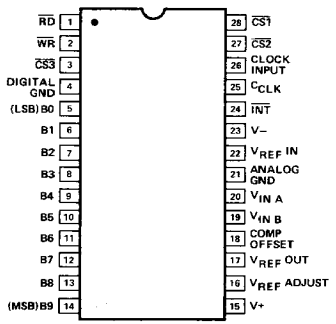
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The ADC-910 is a 10-bit A/D converter designed specifically for interfacing with microprocessors. 3-state data outputs allow direct connection to an 8-bit data bus in an MSB byte of 8 bits and an LSB byte of 2 bits. A command register with read/write inputs and 3 Chip Select inputs to control the 10 data lines is included. Interrupt enable, start conversion and bipolar/unipolar mode selection are controlled by the data bus. The use of high-speed Linear Differential Logic results in fast (6μs) conversion time and low power dissipation.

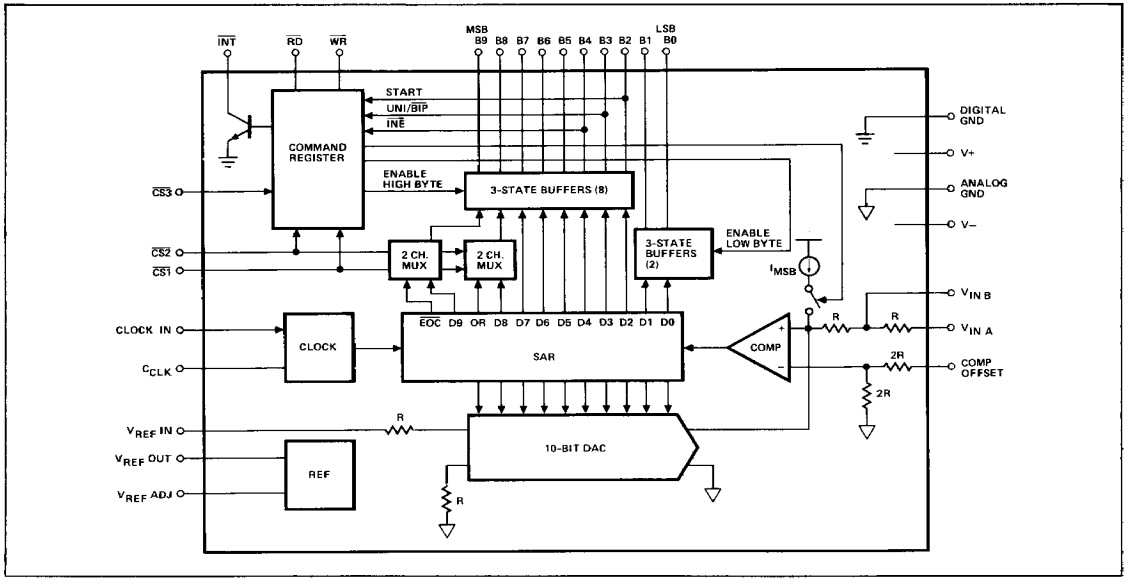
2

PIN CONNECTIONS



28-PIN HERMETIC DIP
(T-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range
- ADC-910AT/BT ..... −55°C to +125°C
- ADC-910ET/FT ..... −25°C to +85°C
- ADC-910GT/HT ..... 0°C to +70°C

Maximum Junction Temperature (T_j) ..... 175°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Supply Voltage (V+) 6V
Supply Voltage (V−) 6V
V+ to V− 12V
Logic Inputs ..... +6V, −0.3V
Logic Outputs (in 3-state) ..... +6V, −0.3V
$V_{IN\,A}$ 15V
$V_{IN\,B}$ 7.5V
Reference Inputs 3.0V
Digital Ground to Analog Ground Voltage 0.5V

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
28-Pin Hermetic DIP (T)	50	7	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP package.

ELECTRICAL CHARACTERISTICS at V+ = 5V, V− = −5V, V_{REF} = 2.5V, f_{CLK} = 0.5MHz; T_A = −55°C to +125°C apply for ADC-910AT/BT, unless otherwise noted.

			ADC-910AT			ADC-910BT			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Integral Nonlinearity (Note 3)	INL	T_A = 25°C	—	—	1/2	—	—	1	LSB
		T_A = Full Temp. Range	—	—	3/4	—	—	1	
Gain Drift (Note 1)	TCG_{FS}	External Reference	—	—	25	—	—	30	ppm FS/°C
		Internal Reference	—	—	40	—	—	50	
Reference Line Regulation		4.75V < V+ < 5.25V	—	—	500	—	—	600	µV/V
Positive Supply Current	I+		—	30	40	—	30	40	mA
Negative Supply Current	I−		—	50	60	—	50	60	mA

ELECTRICAL CHARACTERISTICS at V+ = 5V, V− = −5V, V_{REF} = 2.5V, f_{CLK} = 0.5MHz; T_A = −25°C to +85°C apply for ADC-910ET/FT, unless otherwise noted.

			ADC-910ET			ADC-910FT			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Integral Nonlinearity (Note 3)	INL	T_A = 25°C	—	—	1/2	—	—	1	LSB
		T_A = Full Temp. Range	—	—	1/2	—	—	1	
Gain Drift (Note 1)	TCG_{FS}	External Reference	—	—	20	—	—	25	ppm FS/°C
		Internal Reference	—	—	35	—	—	45	
Reference Line Regulation		4.75V < V+ < 5.25V	—	—	500	—	—	600	µV/V
Positive Supply Current	I+		—	30	40	—	30	40	mA
Negative Supply Current	I−		—	50	60	—	50	60	mA

ELECTRICAL CHARACTERISTICS at V+ = 5V, V− = −5V, V_{REF} = 2.5V, f_{CLK} = 0.5MHz; T_A = 0°C to +70°C apply for ADC-910GT/HT, unless otherwise noted.

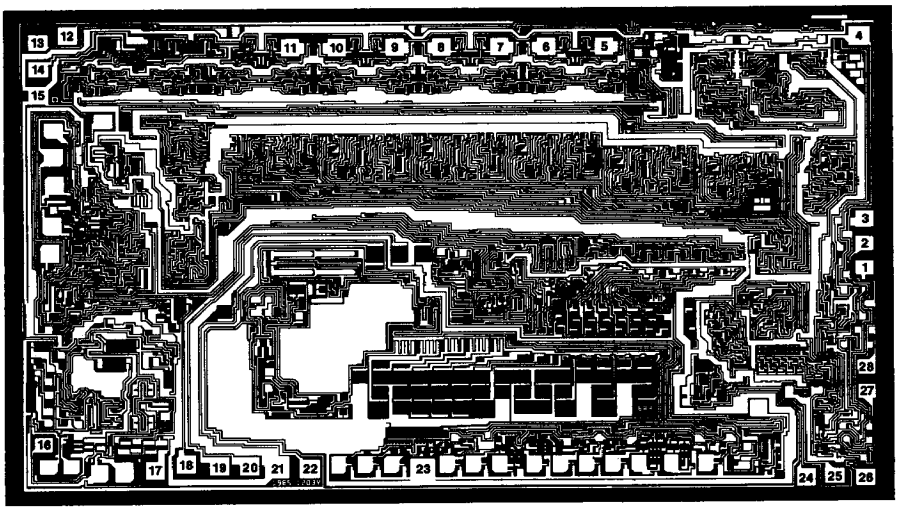
			ADC-910GT			ADC-910HT			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Integral Nonlinearity (Note 3)	INL	T_A = 25°C	—	—	1/2	—	—	1	LSB
		T_A = Full Temp. Range	—	—	3/4	—	—	1	
Gain Drift (Note 1)	TCG_{FS}	External Reference	—	10	—	—	10	—	ppm FS/°C
		Internal Reference	—	25	—	—	25	—	
Reference Line Regulation		4.75V < V+ < 5.25V	—	300	—	—	300	—	µV/V
Positive Supply Current	I+		—	30	—	—	30	—	mA
Negative Supply Current	I−		—	50	—	—	50	—	mA

ELECTRICAL CHARACTERISTICS at V+ = 5V, V− = −5V, V_{REF} = 2.5V, f_{CLK} = 0.5MHz; T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-910AT/ET/GT MIN	TYP	MAX	ADC-910BT/FT/HT MIN	TYP	MAX	UNITS
Resolution	N	T_A = Full Temp. Range	10	—	—	10	—	—	Bits
Resolution for which No Missing Codes Guaranteed		T_A = Full Temp. Range (Notes 2, 3)	10	—	—	10	—	—	Bits
Gain Error	G_{FSE}	V_{REF} = 2.500V (Notes 2, 3)	—	—	4	—	—	6	LSB
Unipolar Mode Offset Error	V_{ZSE}	T_A = Full Temp. Range	—	—	1/2	—	—	1	LSB
Bipolar Mode Offset Error	V_{OSE}		—	—	1	—	—	1.5	LSB
Bipolar Mode Zero-Scale Offset Drift	TCV_{ZS}	T_A = Full Temp. Range (Note 1)	—	—	1	—	—	1.5	LSB
Analog Input Impedance	$R_{IN\,A}$	Pin 20	3.5	5	8	3.5	5	8	kΩ
Analog Input Impedance	$R_{IN\,B}$	Pin 19	1.75	2.5	4	1.75	2.5	4	kΩ
Reference Input Resistance	R_{REF}	Pin 22	1.75	2.5	3.5	1.75	2.5	3.5	kΩ
Reference Voltage Output	$V_{REF}OUT$	Pin 17, Untrimmed	2.45	2.50	2.55	2.45	2.50	2.55	V
Reference Voltage Trim Range		R_T = 10kΩ	±40	—	—	±40	—	—	mV
Reference Output Load Regulation		1mA < I < 5mA, T_A = Full Temp. Range	—	—	1.5	—	—	1.5	mV/mA
Positive Power Supply Sensitivity	$+P_{SS}$	4.75V to 5.25V	—	—	1/2	—	—	1/2	LSB
Negative Power Supply Sensitivity	$-P_{SS}$	−4.75V to −5.25V	—	—	1/2	—	—	1/2	LSB
Conversion Time	T_C	f_{CLK} = 1MHz (Note 4)	—	—	6	—	6	—	μs
Conversion Time	T_C	f_{CLK} = 0.5MHz (Note 5)	—	—	12	—	12	—	μs
Digital Input High	V_{INH}	T_A = Full Temp. Range	2.0	—	—	2.0	—	—	V
Digital Input Low	V_{INL}	T_A = Full Temp. Range	—	—	0.8	—	—	0.8	V
Digital Input Current	I_{INH}	T_A = Full Temp. Range	—	0.4	1	—	0.4	1	μA
Digital Input Current	I_{INL}	T_A = Full Temp. Range	—	10	20	—	10	20	μA
Digital Output High	V_{OH}	I_{OH} = −400μA, T_A = Full Temp. Range	2.4	3.7	—	2.4	3.7	—	V
Digital Output Low	V_{OL}	I_{OL} = 1.6mA, T_A = Full Temp. Range	—	0.1	0.4	—	0.1	0.4	V
Digital Output Current	I_{OH}	V_{OH} = 2.4V	−400	—	—	−400	—	—	μA
Digital Output Current	I_{OL}	V_{OL} = 0.4V	—	—	1.6	—	—	1.6	mA
Three-State Output Leakage	I_{OZ}	T_A = Full Temp. Range	—	5	10	—	5	10	μA

NOTES:
1. Change in 25°C value from 25°C to T_{Min} or T_{Max}.
2. Tested in the 5V unipolar mode at 6μs conversion time.
3. Tested in the ±5V bipolar mode at 12μs conversion time.
4. Applies to 5V input unipolar operation; see Figure 1 for connections.
5. Applies to 10V input unipolar operation, and ±5V/±10V input bipolar operation; see Figure 1 for connections.

DICE CHARACTERISTICS



DIE SIZE 0.131 × 0.221 inch, 28,951 sq. mils
(3.33 × 5.61 mm, 18.68 sq. mm)

1. $\overline{RD}$
2. $\overline{WR}$
3. $\overline{CS3}$
4. DIGITAL GND
5. B0 (LSB)
6. B1
7. B2
8. B3
9. B4
10. B5
11. B6
12. B7
13. B8
14. B9 (MSB)
15. V+
16. V_{REF} ADJUST
17. V_{REF} OUT
18. COMP OFFSET
19. $V_{IN\ B}$
20. $V_{IN\ A}$
21. ANALOG GND
22. V_{REF} IN
23. V−
24. $\overline{INT}$
25. C_{CLK}
26. CLOCK INPUT
27. $\overline{CS2}$
28. $\overline{CS1}$

WAFER TEST LIMITS at V+ = 5V, V− = −5V, V_{REF} = 2.5V, and T_A = 25°C.

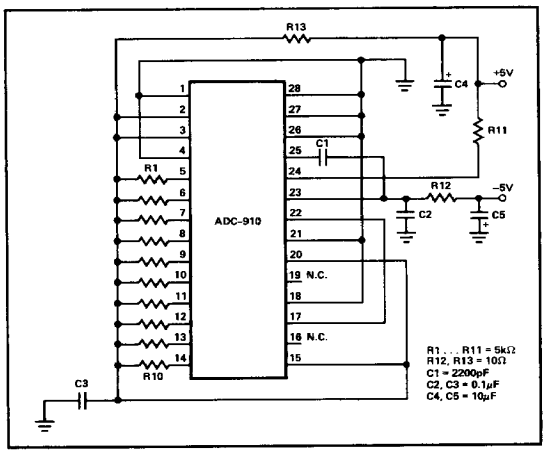
PARAMETER	SYMBOL	CONDITIONS	ADC-910G LIMIT	UNITS
Integral Nonlinearity	INL		1	LSB MAX
Differential Nonlinearity	DNL		1	LSB MAX
Gain Error	G_{FSE}	V_{REF} = 2.500V	6	LSB MAX
Unipolar Mode Offset Error	V_{ZSE}		1	LSB MAX
Analog Input Impedance	$R_{IN\ A}$	Pin 20	3.5/8	kΩ MIN/MAX
Reference Input Resistance	R_{REF}	Pin 22	1.75/4	kΩ MIN/MAX
Reference Voltage Output	V_{REF}OUT	Pin 17, Untrimmed	2.45/2.55	V MIN/MAX
Positive Power Supply Sensitivity	$+P_{SS}$	4.5V to 5.5V	1/2	LSB MAX
Negative Power Supply Sensitivity	$-P_{SS}$	−4.5V to −5.5V	1/2	LSB MAX
Digital Input High	V_{INH}		2.0	V MIN
Digital Input Low	V_{INL}		0.8	V MAX
Digital Input Current	I_{INH} I_{INL}		1 20	μA MAX
Digital Output High	V_{OH}	I_{OH} = −400μA	2.4	V MIN
Digital Output Low	V_{OL}	I_{OL} = 1.6mA	0.4	V MAX
Digital Output Current	I_{OH} I_{OL}	V_{OH} = 2.4V V_{OL} = 0.4V	−400 1.6	μA MIN mA MAX
Three-State Output Leakage	I_{OZ}		10	μA MAX
Positive Supply Current	I+		40	mA MAX
Negative Supply Current	I−		60	mA MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 5V, V− = −5V, V_{REF} = 2.5V, and T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS	ADC-910G TYPICAL	UNITS
Conversion Time	T_C	f_{CLK} = 1MHz, 5V Unipolar Mode f_{CLK} = 0.5MHz ±5V Bipolar Mode	6 12	μs

BURN-IN CIRCUIT



APPLICATIONS INFORMATION

CIRCUIT OPERATION (Refer to the Simplified Schematic)
The ADC-910 uses a successive approximation type A/D conversion routine. When a start command is received by the command register, the SAR, DAC and comparator begin a bit-by-bit trial against the analog input voltage. When all ten bits have been tried, the ten data outputs of the SAR will contain a 10-bit digital representation of the analog input voltage.

When the conversion is complete, a read command and a chip selection will output the data through the 3-state output buffers. Selecting CS1 will output the eight MSBs (the high byte) and selecting CS2 will output the two LSBs (the low byte). Selecting both CS1 and the CS2 will cause all ten data bits to be output through the 3-state output buffers.

When the conversion is complete, the SAR sends an end of conversion (EOC) signal to the command register, which turns on the interrupt output open-collector NPN transistor ($\overline{INT}$), providing the interrupt disable bit ($\overline{INE}$) is set to "0". The EOC signal is also multiplexed into the input of the 3-state buffer for bit 9 (B9). Also, at this time, the overrange signal appears at the SAR output and is multiplexed into the input of the 3-state buffer for bit 8 (B8). These two bits of information comprise the status register, which is multiplexed to the data bus with a read command and a selection of $\overline{CS3}$.

Unipolar/bipolar mode selection and the enabling/disabling of the interrupt output is done when the start of conversion command is entered. In the unipolar mode, the I_{MSB} current source is turned off. For bipolar mode operation, the I_{MSB} current source is applied to the summing mode of the comparator. This provides the proper offset of I_{MSB} to do a bipolar conversion.

BASIC CONNECTIONS (Refer to Figure 1)
Power Supply Connections: The ADC-910 is operated on ±5 volt power supplies. +5 volts is applied to pin 15 and −5 volts is applied to pin 23. These lines should be bypassed near the device with a 0.1μF capacitor in parallel with a large value capacitor such as 10μF.

Analog and Digital Ground: Separate analog and digital grounds are provided to maintain optimum noise rejection. Care should be maintained to insure that digital switching noise is not introduced into the analog ground line. This can be accomplished by making the final ground point as close (physically and electrically) as possible to the analog ground pin of the ADC-910.

Analog Inputs: There are two analog voltage inputs to the ADC-910. $V_{IN\,A}$ (pin 20) accepts input signals between 0 volts and +10 volts in the unipolar mode and between −5 volts and +5 volts in the bipolar mode. $V_{IN\,B}$ (pin 19) accepts input signal levels between 0 volts and +5 volts in the unipolar mode and between −2.5 volts and +2.5 volts in the bipolar mode. The input resistance is nominally 5kΩ for $V_{IN\,A}$ and 2.5kΩ for $V_{IN\,B}$. The comparator offset pin (pin 18) is left open when using $V_{IN\,A}$, and is tied to analog ground when using $V_{IN\,B}$.

FIGURE 1: Basic Connections

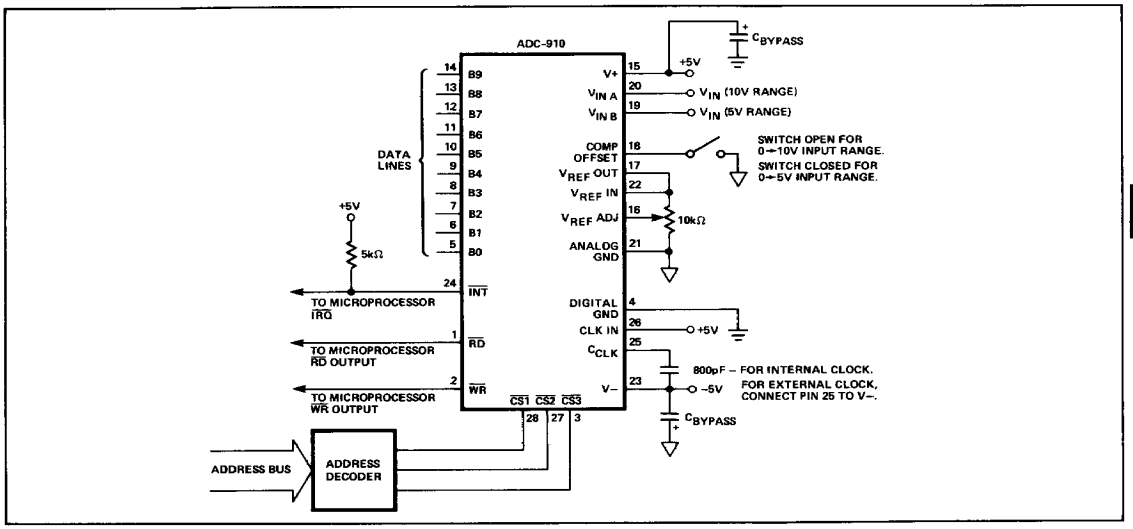


FIGURE 2: Start Conversion and Operating Mode Selection
(Write Mode $\overline{WR}$ = "Low", CS3 = "Low")

MSB B9	B8	B7	B6	B5	B4 (Interrupt Disable/ Enable)	B3 (Unipolar/ Bipolar Select)	B2 (Start Bit)	B1	LSB B0	
X	X	X	X	X	0	0	1	X	X	**Start Conversion, Bipolar Mode, Interrupt Enabled.**
X	X	X	X	X	1	1	1	X	X	**Start Conversion, Unipolar Mode, Interrupt Disabled.**

X = "Don't Care"

FIGURE 3: Reading Data and Status
(Read Mode $\overline{RD}$ = "Low")

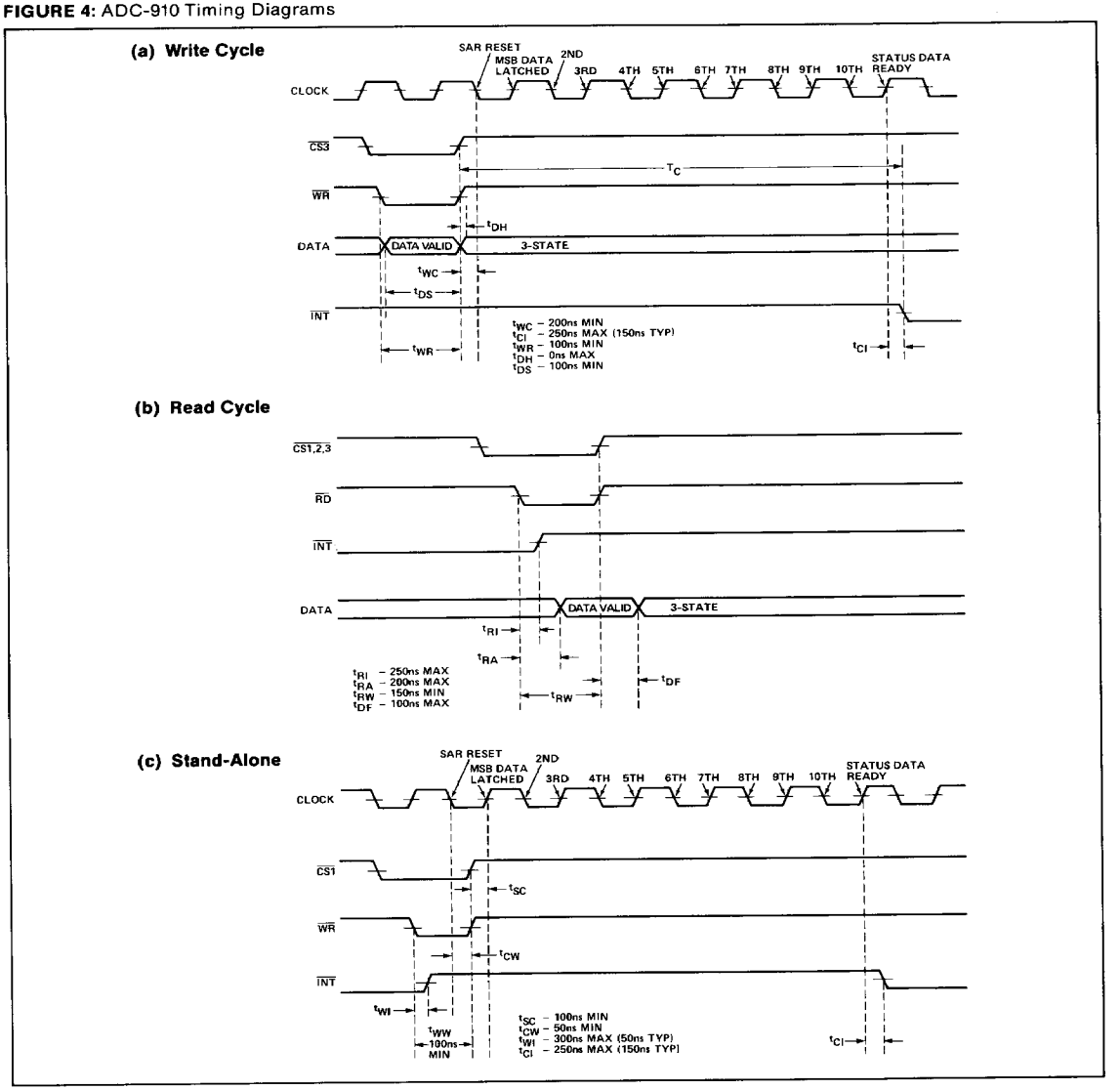
MSB B9	B8	B7	B6	B5	B4	B3	B2	B1	LSB B0	
B9 Data	B8 Data	B7 Data	B6 Data	B5 Data	B4 Data	B3 Data	B2 Data	3-State	3-State	$\overline{CS1}$ = "Low" Read High Byte
3-State	3-State	3-State	3-State	3-State	3-State	3-State	3-State	B1 Data	B0 Data	$\overline{CS2}$ = "Low" Read Low Byte
Busy Bit	Overrange Bit	X	X	X	X	X	X	3-State	3-State	$\overline{CS3}$ = "Low" Read Status

High Byte — Low Byte

Overrange Bit: 1 = Overrange, 0 = Within Range

Busy Bit: 1 = Busy, 0 = Conversion Complete

FIGURE 4: ADC-910 Timing Diagrams



Voltage Reference: The voltage reference for the ADC-910 is nominally +2.5 volts. To use this internal reference, the reference output pin (pin 17) should be tied to the reference input pin (pin 22). Adjustment of the reference voltage may be done by applying a 10kΩ trimmer between the reference output and analog ground with the center tap wiper tied to the reference adjust pin (pin 16).

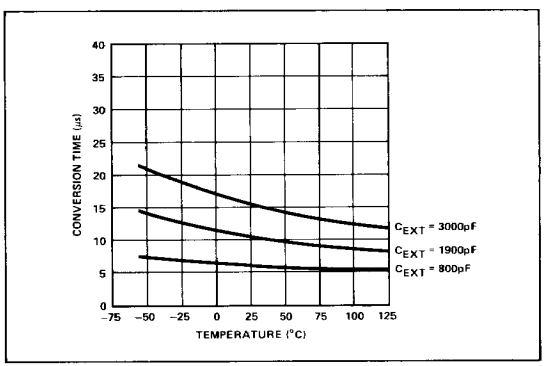
To use an external reference with the ADC-910, simply apply it to the V_{REF} input pin (pin 22). This voltage should be bypassed to analog ground with a 0.01μF capacitor.

Clock: For internal clock operation, the external capacitor (C_{CLK}) sets the conversion rate. The conversion rate graph provides the relationship of C_{CLK} and temperature to conversion rate. The C_{CLK} capacitor is connected between C_{CLK} (pin 25) and the V– supply (pin 23), see Figure 1. The clock input (pin 26) is connected to the V+ supply (pin 15). Internal clock operation exhibits a conversion time variation from device to device for a given C_{CLK}, due to capacitor and internal resistor tolerances of the basic R-C oscillator. For operation at the upper frequencies of 0.5 and 1MHz, an external clock input is recommended.

For external clock operation, no clock capacitor is required. The C_{CLK} pin (pin 25) should be tied to the –5 volt supply and the external clock is applied to the clock input (pin 26). 1.0MHz clock maximum may be used. This will result in a 6μs conversion time. Slower clock rates will result in slower conversion speeds.

$$\text{Conversion time} \approx 6 \times \frac{1}{f_{CLK}}$$

Conversion time (T_C) also depends on user supplied timing relationship between positive $\overline{WR}$ edge and negative clock edge used to reset the SAR. See Figure 4(a) t_{WC} parameter.



CHIP SELECT, READ AND WRITE INPUTS
(Refer to Figure 2)
Start Commands: To start a conversion the $\overline{WR}$ input (pin 2) must be held "low" while $\overline{CS3}$ (pin 3) is held "low" and a logic "high" is applied to bit 2 (pin 7). Another way to start a conversion is to hold $\overline{CS1}$ (pin 28) and $\overline{WR}$ (pin 2) "low" for a complete clock cycle.

Operating mode selection is done when the start command is applied. As with the start command, $\overline{WR}$ and $\overline{CS3}$ are held "low". A logic "high" applied to bit 4 (pin 9) disables the interrupt and a logic "low" enables the interrupt. A logic "high" applied to bit 3 (pin 8) selects unipolar mode and a logic "low" selects bipolar-mode operation.

READING DATA AND CONVERSION STATUS
(Refer to Figure 3)
Data can be read in two ways: a single 10-bit word or in a 8-bit "high byte" with a 2-bit "low byte". When interfacing to a 16-bit bus, single 10-bit word reading is possible. When using an 8-bit data bus, the "high byte" and "low byte" can be multiplexed onto a single 8-bit bus as indicated in Figure 5.

To read all 10 bits at once, the RD (pin 1), CS1 (pin 28) and CS2 (pin 27) are all held "low". This turns on 3-state output buffers and all data bits can be read.

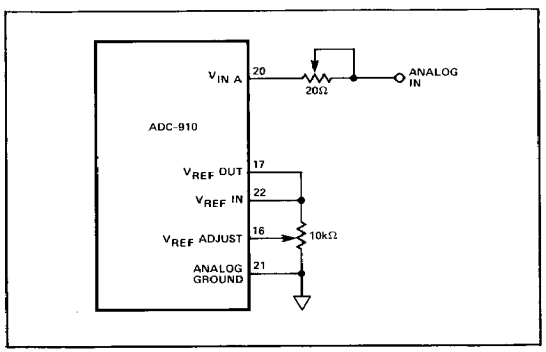
To read the 8-bit "high byte", the RD (pin 1) and CS1 (pin 28) lines are held "low".

To read the 2-bit "low byte", the RD and CS2 lines are held "low".

Included on the ADC-910 is a 2-bit status register which is multiplexed onto the data bus on lines B9 and B8.

To read the status register, RD (pin 1) and CS3 are held "low". End of conversion (EOC) is indicated by a "low" bit 9 (pin 14) and overrange (OR) is indicated by a "high" in bit 8 (pin 13).

FIGURE 5: Calibration Circuit



CALIBRATION (Refer to Figure 5)
Unipolar Mode: To adjust out gain error, a trimmer may be inserted in series with the analog input voltage input. Assuming a 2.500 volt reference is applied at the reference input, gain error trimming is accomplished by adjusting the input trimmer so that the final digital output code transition occurs for an input voltage of V_A = 9.985 volts (this is the transition from 1111 1111 10 to 1111 1111 11). When using the internal reference or an adjustable external reference, gain error trimming may be accomplished by adjusting the reference voltage until the final digital output code transition occurs at V_A = 9.985 volts.

Bipolar Mode: To trim out offset error, set series trimmer (if used) to 0Ω and tie $V_{IN\ A}$ to analog ground. Adjust V_{REF} to just beyond the major carry transition (that point where the digital output code changes from 0111 1111 11 to 1000 0000 00).

To trim out gain error, tie $V_{IN\ A}$ to voltage source. Adjust the series trimmer so that the final digital output code transition (from 1111 1111 10 to 1111 1111 11) occurs at an input voltage of +4.9902V.

DRIVING THE ANALOG INPUT

To insure 10-bit accuracy the input to the ADC-910 must be driven by a source which has an output impedance of less than 0.5 ohms at 1MHz.

INTERFACING THE ADC-910 TO THE MC68000

(Refer to Figure 6)

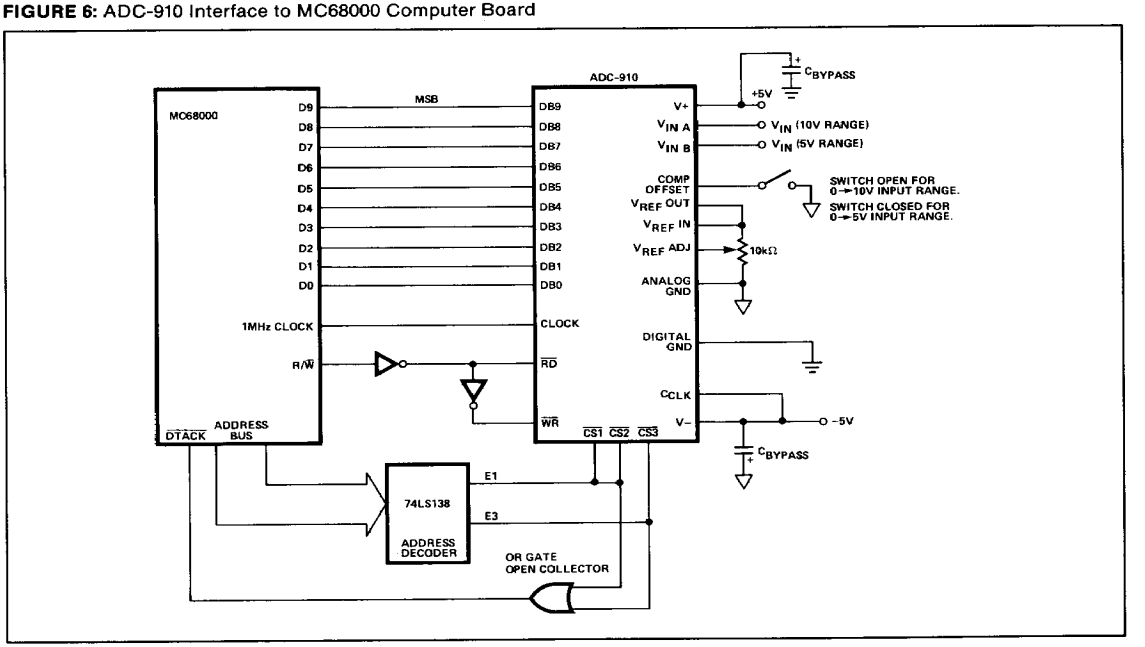
An example of a direct connection to a 16-bit data bus is shown in Figure 6. The 10-bit output of the ADC-910 is connected directly to the 10 least significant bits of the MC68000 data bus. In this example, a Motorola MC68000 Computer Board supports the 68000μP. A flow chart and assembly language program is shown below for a simplified 10-bit wide conversion.

INTERFACING THE ADC-910 TO THE 6502μP

(Refer to Figure 7)

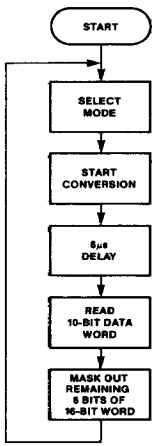
An example of direct connection to an 8-bit data bus is shown in Figure 7. Notice that the two least significant bits are connected to data bits B3 and B4. This allows a 10-bit data transfer over an 8-bit bus. In this example, a Synertek Systems SYM-1 Educational Computer Board supports the 6502μP. The flow charts and op codes for a variety of conversion exercises are shown below.

FIGURE 6: ADC-910 Interface to MC68000 Computer Board



ADC-910 INTERFACE SOFTWARE AND FLOW CHART FOR 16-BIT μP (MC68000 COMPUTER BOARD)

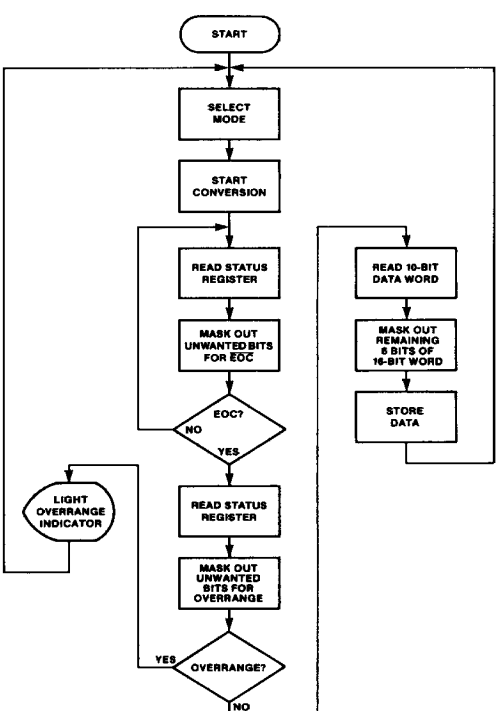
(a) Minimum Software Using Fixed Delay



PC	MNEMONIC	COMMENT
1000	MOVEQ #12, D0	Select Mode*
1002	MOVE D0, $50000	Start Conversion
1008	NOP	
100A	NOP	Delay
100C	NOP	
100E	MOVE $20000, D1	Read Data
1014	ANDI #1023, D1	Mask out B15–B10 leaving B9–B0
1018	JMP $1000	Jump to 1000

* Loading a decimal 12 into D0 will apply the following binary word to the command register at the start of the conversion:
B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
0 0 0 0 0 0 1 1 0 0
This results in unipolar mode selection with the interrupt disabled.

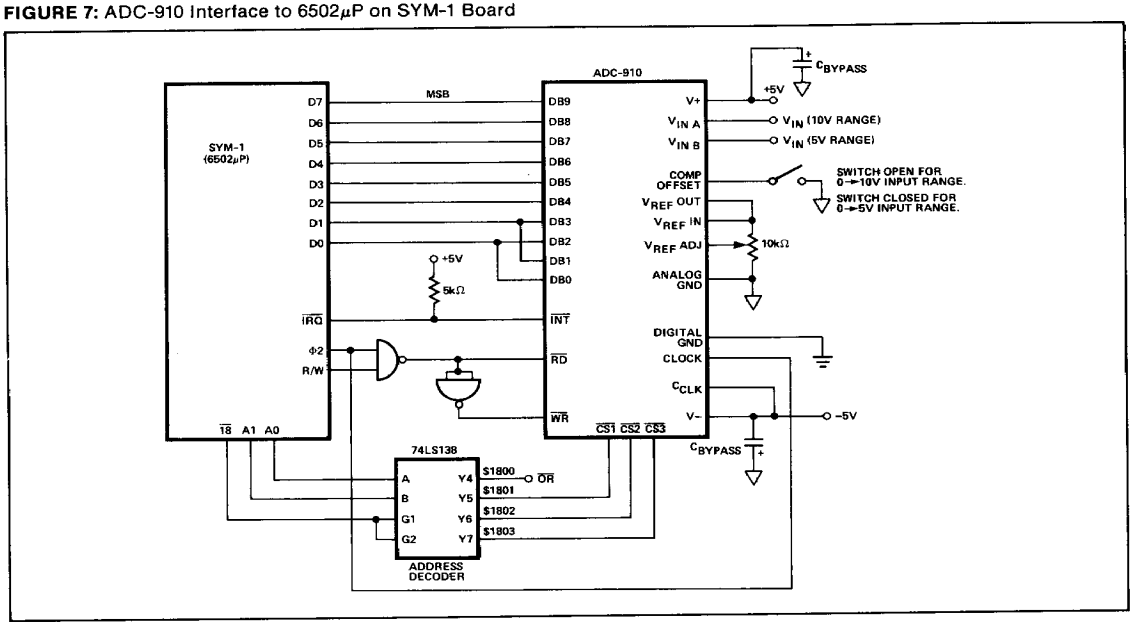
(b) Polling Status Register for End of Conversion and Overrange



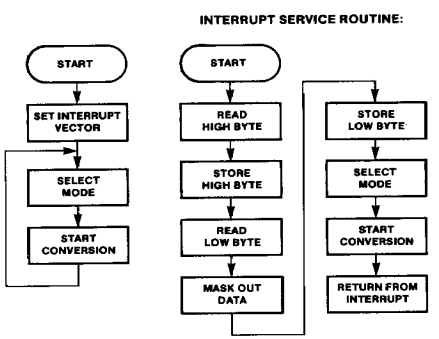
PC	MNEMONIC	COMMENT
1000	MOVEQ #X,D0	Select Mode*
1002	MOVE D0, $50000	Start Conversion
1008	MOVE $50000,D1	Read Status Register into D1
100E	AND #512,D1	Mask for EOC Bit (1000000000 = 512 Decimal)
1012	BNE.L $1008	Loop Until EOC
1016	MOVE $50000,D2	Read Status Register
101C	AND #256,D2	Mask for OR Bit (0100000000 = 256 Decimal)
1020	BEQ.L $102E	Branch to $102E Unless OR
1024	MOVE D3,$40000	Light OR Indicator
102A	JMP $1000	Start Over
102E	MOVE $20000,D4	Read and Store 10-Bit Data
1032	AND #1023,D4	Mask Unwanted 6 LSBs
1036	JMP $1000	Start Over

*For Bipolar Mode with Interrupt Enabled: X = 4 Decimal
For Unipolar Mode with Interrupt Enabled: X = 12 Decimal
For Bipolar Mode, Interrupt Disabled: X = 20 Decimal
For Unipolar Mode, Interrupt Disabled: X = 28 Decimal

FIGURE 7: ADC-910 Interface to 6502μP on SYM-1 Board



ADC-910 INTERFACE SOFTWARE AND FLOW CHART FOR 6502μP (SYM-1)
Interrupt-Driven Conversion



PC	MNEMONIC	OP CODE	COMMENT
0200	LDA#$02	A9 02	Set Interrupt Vector
0202	STA$A679	8D 79 A6	
0205	LDA#$12	A9 12	
0207	STA$A678	8D 78 A6	
020A	LDA#$03	A9 03	Select Mode (Unipolar, Interrupt Enabled)
020C	STA$1803	8D 03 18	Start Conversion
020F	JMP$20A	4C 0A 02	Jump to 20A (Loop Until Interrupt)
	Interrupt Service Routine		
0212	LDA$1801	AD 01 18	Read High Byte
0215	STA$024E	8D 4E 02	Store High Byte at 024E
0218	LDA$1802	AD 02 18	Read Low Byte
021B	AND#$03	29 03	Mask Out Bits 9–4
021D	STA$024F	8D 4F 02	Store Low Byte at 024F
0220	LDA#$03	A9 03	Select Mode
0222	STA$1803	8D 03 18	Start Conversion
0225	RTI	40	Return from Interrupt