APPLICATION NOTE

APN1001: Circuit Models for Plastic Packaged Microwave Diodes

Abstract

This paper reports on the measurement and establishment of circuit models for SOT-23 and SOD-323 packaged diodes. Results indicate that the 1.5 nH estimate for the SOT-23 is a useful result, as is 1.2 nH for SOD-323 single packaged diodes. It was also determined that the effective inductance of the SOT-23 may be reduced to approximately 0.4 nH by adding a second bond wire and modifying the microstrip line. Other lead configurations, including parallel bond wires and common cathode configurations, were also studied.

Introduction

Discrete, low-cost, surface mount semiconductor diodes are attractive choices for UHF and microwave applications where package parasitic may have a significant impact on performance. The most common package styles are the SOT-23 and the SOD-323 (Figure 1) which were neither designed nor intended for RF service. A primary limitation to their high-frequency performance, particularly in PIN diode shunt connected switches, is parasitic package inductance, which limits high-frequency isolation. The model information available from vendors of these devices has been generally limited to estimates of inductance, typically 1.5 nH, for single junction SOT-23 diodes. Establishing a better model will enable circuit designers to better predict performance and possibly give the manufacturer alternative designs to reduce package parasitic effects.

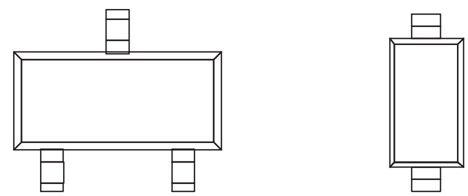


Figure 1. Diode Package Styles

Package Modeling

Network Analysis

To create a high-frequency device model S-parameter, measurements were taken over a wide frequency band so that resonance and other high order effects would be included in the measurements. This procedure utilizes an HP 8510C vector network analyzer. The package under test was inserted into an Inter-Continental Microwave test fixture as a series connected element. This fixture uses a Thru-Reflect-Line calibration procedure to produce accurate calibration and assures a reference plane at the device under test.

Using this methodology, a circuit model was generated for each of the devices as shown in Figures 2 and 3. These models produce very good correlation between the measured and simulated performance as shown in Figure 4.

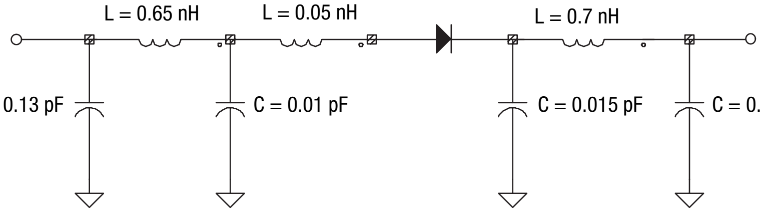


Figure 2. SOT-23 Circuit Model

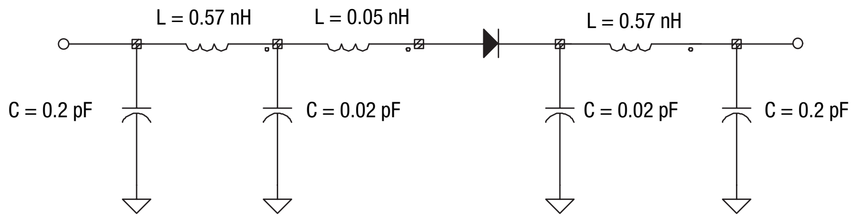


Figure 3. SOD-323 Circuit Model

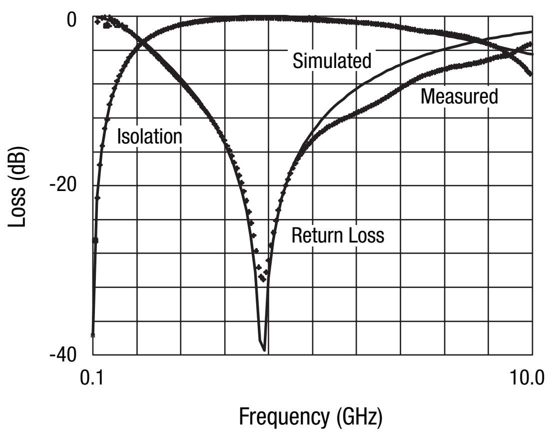


Figure 4. Measurement vs. Model Simulation of a SOT-23 Package

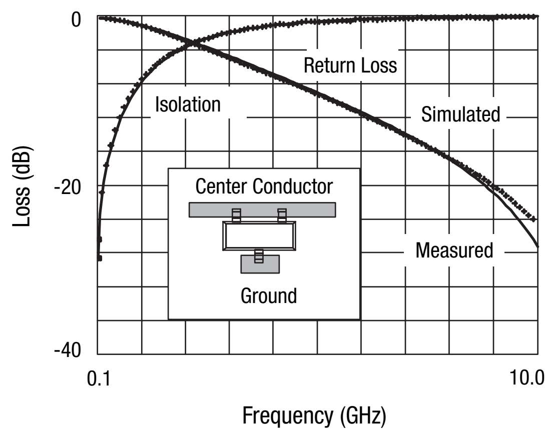


Figure 5. SOT-23 Validation: Simulation vs. Measurement

Impedance Measurements

The HP 4291A Impedance Analyzer, an instrument based on measuring the vector V/I with coverage from 1 MHz–1.8 GHz, was also utilized to characterize inductance of the packages under consideration. Measurements were taken on a group of PIN diodes that were forward biased to low values of forward resistance. The inductance values derived from these measurements are shown in Table 1 and compare well with the values derived from network analysis. The advantage of the direct impedance measurement is the capability of a quick measurement without the necessity of hard bonding the device to a substrate.

Validation of Simulated Model

Validation of the model was performed by placing the diode into a test circuit that simulates a shunt connected switch. The test circuit was constructed using a Duriod microstrip board and the device was placed as shown in Figure 5. This provided a different operating environment because not only was the diode connected differently, but the microstrip insulator had a different dielectric constant.

The measured performance of this circuit was imported into the circuit simulator and compared to a simulation using the circuit model. Figure 6 shows good validation of the network analyzer generated model.

Alternative SOT-23 Designs for Lower Inductance

To reduce the total inductance of the SOT-23 package, alternative wire bonding schemes were studied. Figure 6 shows four bonding wire designs considered in this study. The measured inductance of these bonding schemes are shown on Table 1.

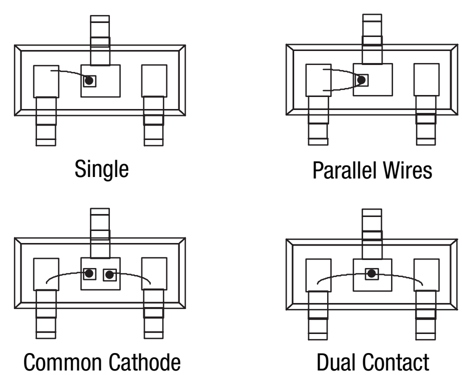
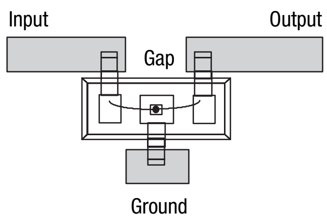


Figure 6. SOT-23 Configurations

The single wire SOT-23 diode with 1.5 nH inductance will perform with 10.1 dB isolation at 900 MHz as a shunt connected switch. The inductance is reduced to 1.2 nH if a parallel bond wire is attached to the diode contact. This will increase the isolation to 11.6 dB. A further reduction of inductance may be obtained by adding a second diode chip in a common cathode configuration. This reduces the inductance to 0.84 nH resulting in an increase in isolation to 14.6 dB.

Since two junctions are employed, in the common cathode alternative, the capacitance is doubled under reverse bias. The consequence may be an adverse effect on insertion loss. The inductance of the dual bond wire design is similar to the common cathode design resulting in similar performance. But, if the package is inserted in the microstrip circuit with a gap in the transmission line as shown in Figure 7, then the effective inductance is reduced to below 0.4 nH and the isolation is increased to 20 dB at 900 MHz. Figure 7 shows a plot of the measured isolation of the dual bond wire package versus frequency to 4 GHz. A plot of an inductance of 1.5 nH is shown as a reference.

Table 1 shows a summary of the effective package inductance values for the SOD-323 and SOT-23 packaged diodes with alternative wiring configurations using the measurement techniques described.



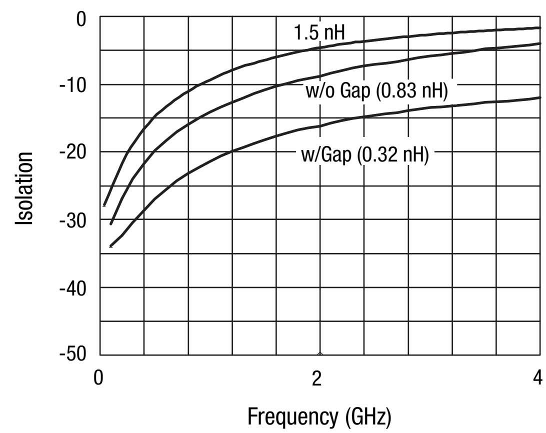


Figure 7. SOT-23 Dual Bond Wire With and Without a Gap

Package	Configuration	S-Parameter Model (nH @ 1 GHz)	S-Parameter Validation (nH @ 1 GHz)	HP 4291A Inductance (nH)
SOT-23	Single junction	1.45	1.5	1.5/1.7
SOT-23	Dual no gap	1.2	0.9	
SOT-23	Dual gap	0.5	0.4	
SOT-23	Parallel bonds			1.2
SOT-23	Common cathode			0.84
SOT-323	Single junction	1.1	1.19	1.2

Table 1. Summary of Package Inductance Values

Conclusion

As a result of this effort, accurate and concise microwave models are now available for commonly used, low-cost, surface mount, SOT-23 and SOD-323 packaged diodes. The measurement methodology utilized de-imbedding techniques valid at frequencies through 10 GHz. This material will assist design engineers to design and predict circuit performance using these popular devices.

In addition, it was demonstrated that the inductance of the SOT-23 may be significantly reduced by modifying both the internal package wiring and the microstrip transmission line. This further improves the frequency response of the package.

Reference

R.W. Waugh and D. Gustedt, “Low Cost Surface Mount Power Limiters,” Proceedings RF EXPO WEST, March 1992, pp. 19-40.