



3.3V CMOS 20-BIT D-TYPE FLIP-FLOP WITH 3-STATE OUT- PUTS, 5 VOLT TOLERANT I/O

IDT74LVC16821A

FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC16821A:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

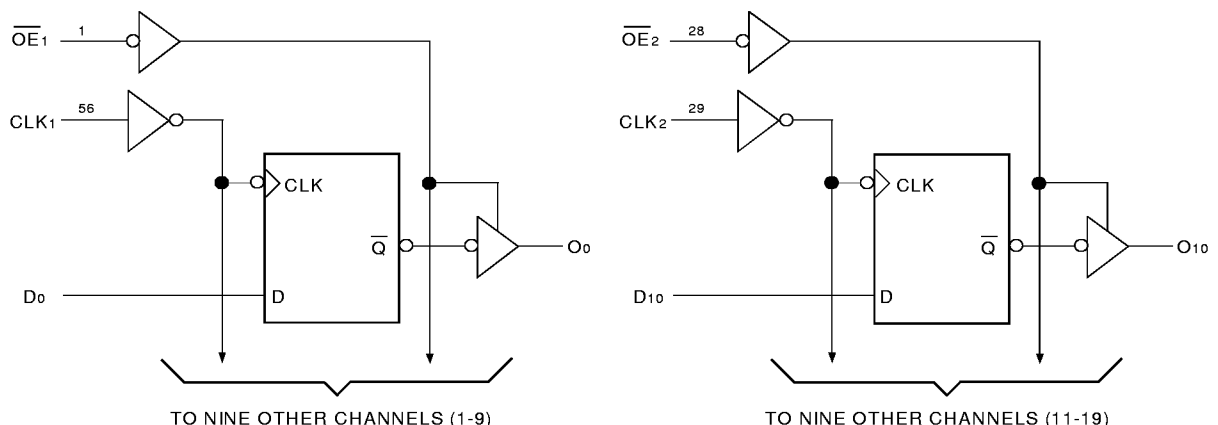
The LVC16821A 20-bit Flip-Flop is built using advanced dual metal CMOS technology. This device contains twenty non-inverting D-Type flip-flops with 3-State outputs. The device is byte controlled with each byte functioning identically, but independent of each other. Control pins can be shorted together to obtain full 20-bit operation.

The buffered output-enable ($\overline{OE}$) inputs place the 20 outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without the need for interface drive or pullup components. $\overline{OE}$ inputs do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

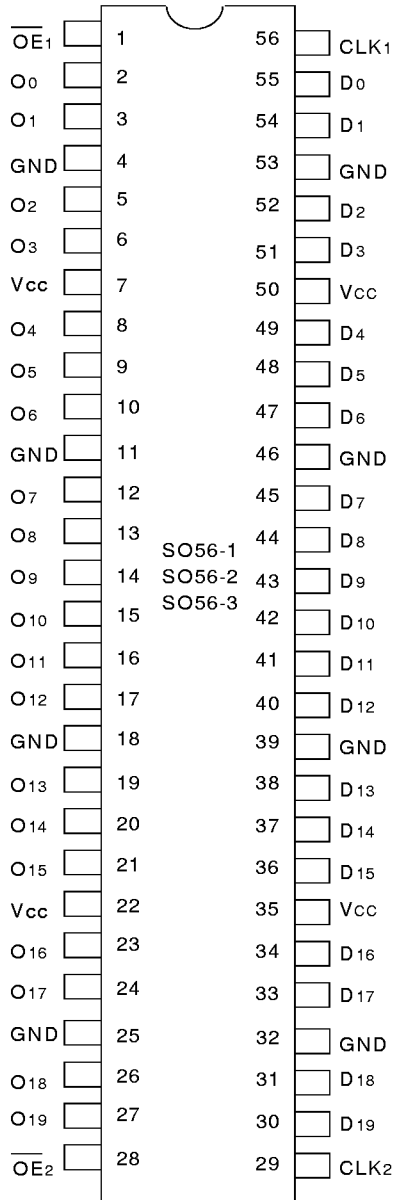
All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a Flip-Flop in a mixed 3.3V/5V supply system.

The LVC16821A has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
TSTG	Storage Temperature	– 65 to +150	°C
I _{OUT}	DC Output Current	– 50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	– 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

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NOTE:

- As applicable to the device type.

FUNCTION TABLE (1)

Inputs			Outputs
Dx	CLKx	$\overline{OE}x$	Ox
X	X	H	Z
L	↑	L	L
H	↑	L	H
X	H or L	L	O ₀ ⁽²⁾

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH transition
- O₀ = Output level before LOW-to-HIGH clock transition.

PIN DESCRIPTION

Pin Names	Description
Dx	Data Inputs
Ox	3-State Outputs
CLKx	Clock Input
$\overline{OE}x$	Output Enable Inputs (Active LOW)

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 5.5V	—	—	± 5	μA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to 5.5V	—	—	± 10	μA
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 5.5\text{V}$		—	—	± 50	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or V_{CC}	—	—	10	μA
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ other inputs at V_{CC} or GND		—	—	500	μA

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NOTES:

- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -6\text{mA}$	2	—	
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -12\text{mA}$	1.7	—	
		$V_{CC} = 2.7\text{V}$		2.2	—	
		$V_{CC} = 3.0\text{V}$		2.4	—	
		$V_{CC} = 3.0\text{V}$	$I_{OH} = -24\text{mA}$	2.2	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OL} = 0.1\text{mA}$	—	0.2	V
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 6\text{mA}$	—	0.4	
			$I_{OL} = 12\text{mA}$	—	0.7	
		$V_{CC} = 2.7\text{V}$	$I_{OL} = 12\text{mA}$	—	0.4	
		$V_{CC} = 3.0\text{V}$	$I_{OL} = 24\text{mA}$	—	0.55	

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NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance Outputs enabled	$C_L = 0pF$, $f = 10MHz$	—	pF
CPD	Power Dissipation Capacitance Outputs disabled		—	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min	Max	Min	Max	
t _{PHL}	Propagation Delay	1.5	6.5	1.5	6.2	ns
t _{PLH}	CLKx to Ox					
t _{PZL}	Output Enable Time	1.5	7	1.5	6.5	ns
t _{PZH}	$\overline{OE}x$ to Ox					
t _{PLZ}	Output Disable Time	1.5	7	1.5	6.5	ns
t _{PHZ}	$\overline{OE}x$ to Ox					
t _{SU}	Set-up Time HIGH or LOW Dx to CLK	2.5	—	2.5	—	ns
t _H	Hold Time HIGH or LOW Dx to CLK	1.5	—	1.5	—	ns
t _W	CLK Pulse Width	3.3	—	3.3	—	ns
t _{SK(o)}	Output Skew ⁽²⁾	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. $T_A = -40^\circ C$ to $+85^\circ C$.

2. Skew between any two outputs of the same package and switching in the same direction.

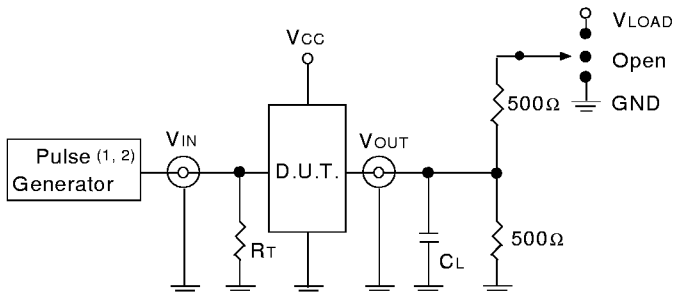
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1) = 3.3V ± 0.3V	V _{CC} (1) = 2.7V	V _{CC} (2) = 2.5V ± 0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance; includes jig and probe capacitance.
 R_T = Termination resistance; should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

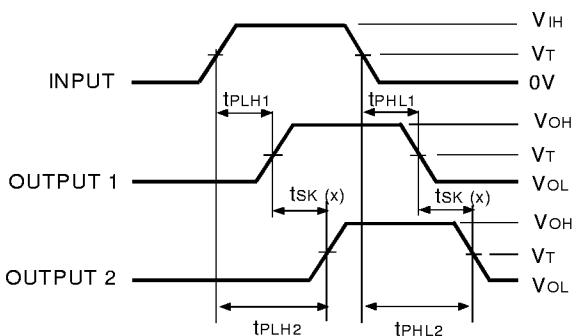
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK}(x)



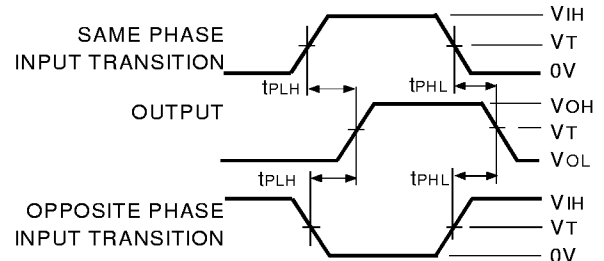
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

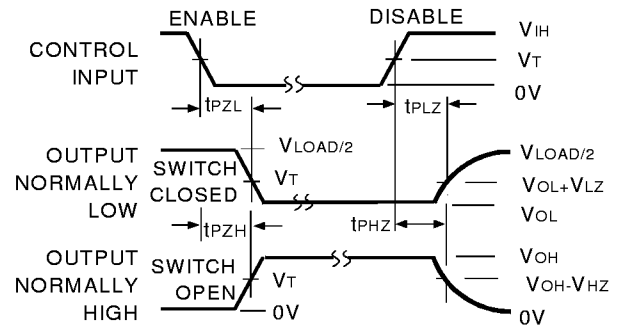
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

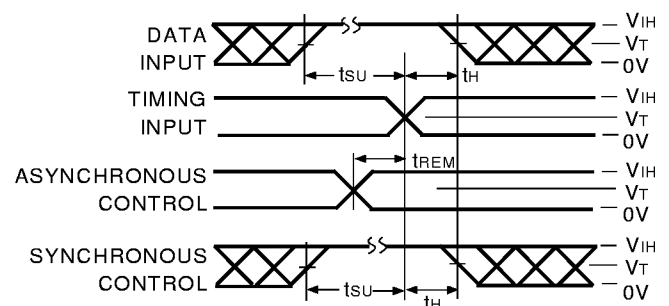


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NOTE:

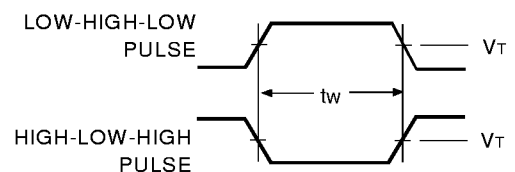
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	LVC	X	XX	XXXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					821A		20-Bit D-Type Flip-Flop with 3-State Outputs, 5V Tolerant I/O
					16		Double-Density with Resistors, $\pm 24\text{mA}$
						Blank	No Bus-hold
						74	-40°C to $+85^{\circ}\text{C}$



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