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SSI 32R510A/510AR
4, 6 Channel Read/Write Devices

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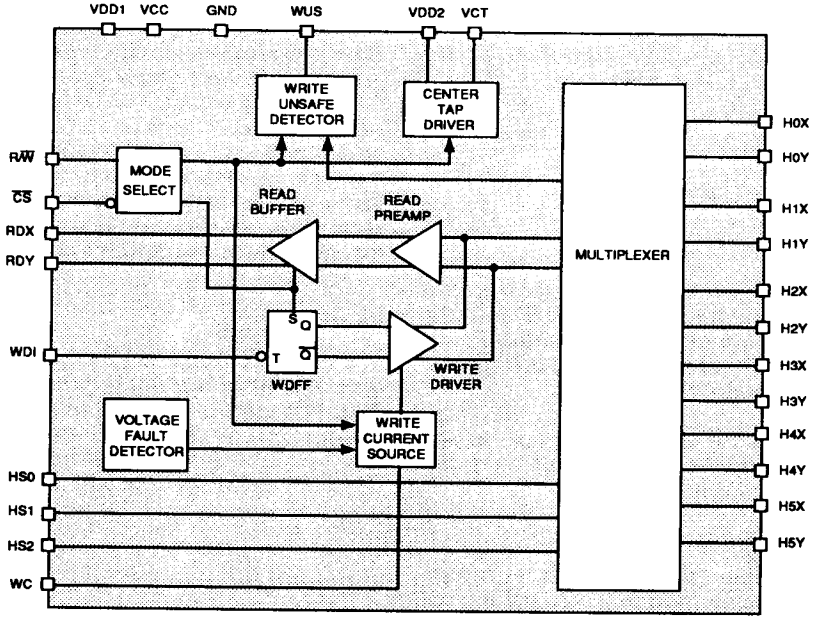
DESCRIPTION

The SSI 32R510A/510AR Read/Write devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read amplifier, write current control and data protection circuitry for as many as six channels. The R option provides internal 750Ω damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. They are available in a variety of package and channel configurations.

FEATURES

- **High performance:**
  - **Read mode gain = 100 V/V (32R510A)**
  - **Input noise = 1.5 nV/√Hz max.**
  - **Input capacitance = 20 pF max.**
  - **Write current range = 10 mA to 40 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Plug compatible to the SSI 32R117**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Write unsafe detection**
- **TTL compatible control signals**
- **+5V, +12V power supplies**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

These devices address up to six center-tapped ferrite heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$, and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$, will force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	None

0 = Low level 1 = High level X=Don't care

WRITE MODE

The write mode configures the device as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI).

The magnitude of the write current (0-pk) is programmed by an external resistor RWC, connected from pin WC to ground and is given by:

$$Iw = \frac{K}{RWC}$$

where K is the Write Current Constant. In multiple device applications, a single RWC resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in read mode
- No write current

To reduce internal power dissipation, an optional external resistor, RCT, given by RCT ≤ 130Ω x 40/Iw (Iw in mA), is connected between pins VDD1 and VDD2. Otherwise connect pin VDD1 to VDD2.

To initialize the Write Data Flip Flop (WDFF) to pass current through the X-side of the head, pin WDI must be low when the previous read mode was commanded.

READ MODE

The read mode configures the device as a low noise differential amplifier and deactivates the write current generator and write unsafe circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent pulse detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector, and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects Read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H5X H0Y-H5Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal output
WC	*	Write Current: used to set the magnitude of the write current
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center-tap voltage source
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VDD1	-0.3 to +14	VDC
DC Supply Voltage	VDD2	-0.3 to +14	VDC
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range	VIN	-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VDD1 + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +14	VDC
Write Current (0-pk)	Iw	60	mA
RDX, RDY Output Current	Io	-10	mA
VCT Output Current	IVCT	-60	mA
WUS Output Current	Iwus	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Lead Temperature PDIP, (10 sec Soldering)		260	°C
Package Temperature PLCC, SO (20 sec Reflow)		215	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VDD1	DC Supply Voltage		10.8	12.0	13.2	VDC
VCC	DC Supply Voltage		4.5	5.0	5.5	VDC
Lh	Head Inductance		5		15	µH
RD	Damping Resistor	32R510A	500		2000	Ω
RCT*	RCT Resistor	Iw = 40 mA	123	130	137	Ω
Iw	Write Current (0-pk)		10		40	mA
Tj	Junction Temperature Range		+25		+135	°C

*For Iw = 40 mA. At other Iw levels refer to Applications Information that follows this specification.

DC CHARACTERISTICS

(Recommended operating conditions apply unless otherwise specified.)

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current	Read/Idle Mode			35	mA
	Write Mode			30	mA
VDD Supply Current (sum of VDD1 and VDD2)	Idle Mode			20	mA
	Read Mode			35	mA
	Write Mode			20 + Iw	mA
Power Dissipation (Tj = +135°C)	Idle Mode			400	mW
	Read Mode			600	mW
	Write Mode, Iw = 40 mA, RCT = 0Ω			800	mW
	Write Mode, Iw = 40 mA, RCT = 130Ω			600	mW

DC CHARACTERISTICS (continued)

DIGITAL I/O

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VIL Input Low Voltage				0.8	VDC
VIH Input High Voltage		2.0			VDC
IIL Input Low Current	VIL = 0.8V	-0.4			mA
IIH Input High Current	VIH = 2.0V			100	µA
VOL WUS Output Low Voltage	IOL = 8 mA			0.5	VDC
IOH WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

VCT Center Tap Voltage	Write Mode 32R510A		6.0		VDC
Head Current (per side)	Write Mode, 0 ≤ VCC ≤ 3.7V, 0 ≤ VDD1 ≤ 8.7V	-200		200	µA
Write Current Range		10		40	mA
Write Current Constant "K"		2.375		2.625	
Iwc to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY = 6V Write/Idle Mode	-100		100	µA

READ MODE

VCT Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200		200	µA
Input Bias Current (per side)				45	µA
Output Offset Voltage	Read Mode 32R510A	-440		+440	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING

Iw = 35 mA, Lh = 10 µH, Rd = 750Ω; f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF. Recommended operating conditions apply unless otherwise specified.

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R510A	10K			Ω
	32R510AR	600		960	Ω
WDI Transition Frequency	WUS = low	250			KHz

READ MODE

Differential Voltage Gain 32R510A	Vin = 1 mVpp @ 300 kHz ZL(RDX), ZL(RDY) = 1 kΩ	85		115	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10% Vin = Vi + 0.5 mVpp @ 300 kHz	-2		+2	mV
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	$nV/\sqrt{Hz}$
Differential Input Capacitance	f = 5 MHz			20	pF
Differential Input Resistance	32R514, f = 5 MHz	3.2K			Ω
	32R514R, f = 5 MHz	500		1000	Ω
	32R510A, f = 5 MHz	2K			Ω
	32R510AR, f = 5 MHz	460		860	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Single Ended Output Resistance	f = 5 MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

DYNAMIC CHARACTERISTICS AND TIMING (continued)

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write Mode	Delay to 90% of Write Current			1.0	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current			1.0	µs
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope			1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			1.0	µs
HS0 - HS2 to any head	Delay to 90% of 100 mV 10 MHz Read Signal Envelope			1.0	µs
WUS, Safe to Unsafe - TD1	Iw = 35 mA, see Figure 1	1.6		8.0	µs
WUS, Unsafe to Safe - TD2	Iw = 35 mA, see Figure 1			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω, see Figure 1)					
Prop. Delay - TD3	From 50% Points			25	ns
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	ns
Rise/Fall Time	10% - 90% Points			20	ns

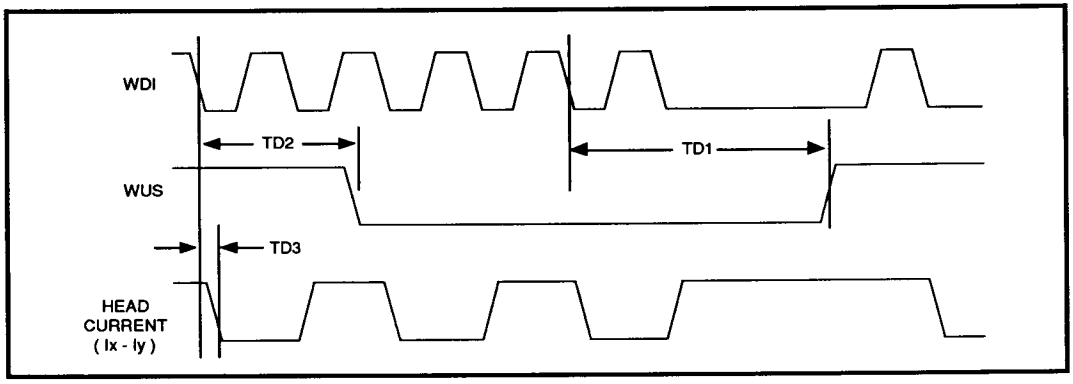


FIGURE 1: Write Mode Timing Diagram

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

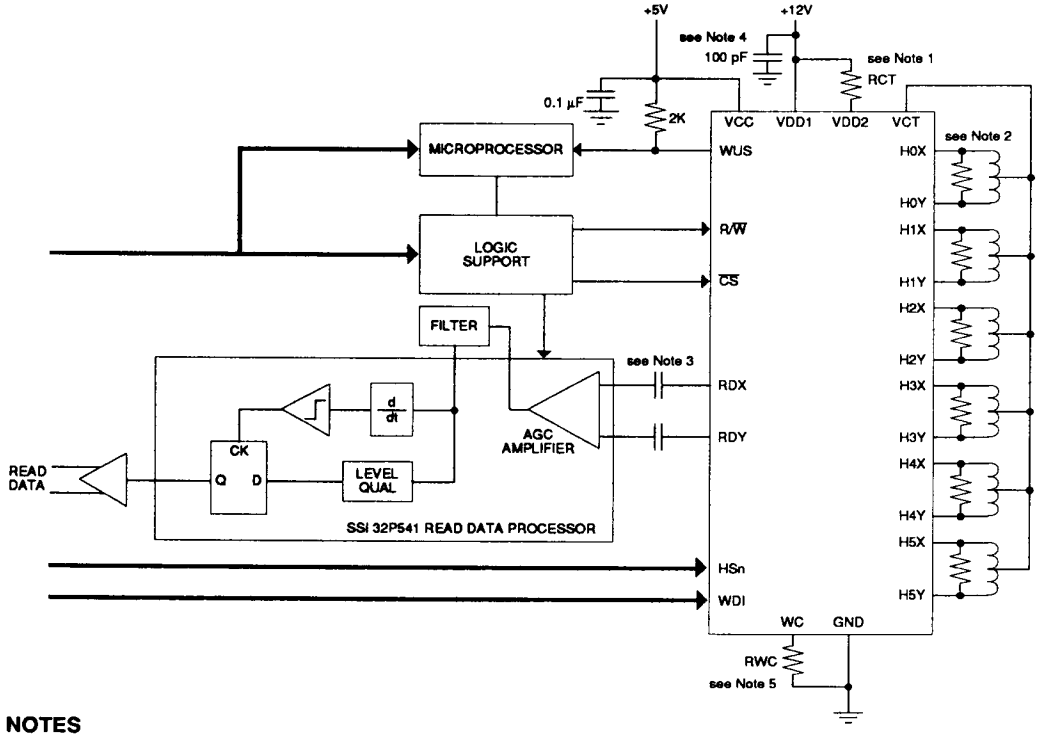
TABLE 3: Key Parameters Under Worst Case Input Noise Conditions

PARAMETER		Tj=25°C	Tj=135°C	UNITS
Inputs Noise Voltage (max.)		1.1	1.5	nV/√Hz
Differential Input Resistance (min.)	32R510AR	850	1000	Ω
	32R510A	15.4	29.4	KΩ
Differential Input Capacitance (max.)		11.6	10.8	pF

TABLE 4: Key Parameters Under Worst Case Input Impedance Conditions

PARAMETER		Tj=25°C	Tj=135°C	UNITS
Inputs Noise Voltage (max.)		0.92	1.2	nV/√Hz
Differential Input Resistance (min.)	32R510AR	500	620	Ω
	32R510A	3.2	6.1	KΩ
Differential Input Capacitance (max.)		10.1	10.3	pF

APPLICATIONS INFORMATION (continued)



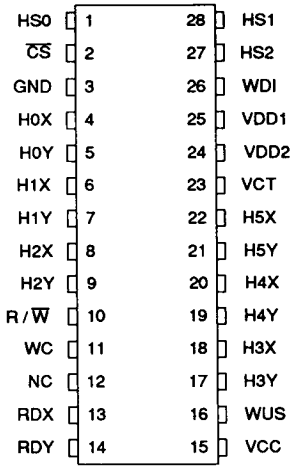
NOTES

1. An external resistor, RCT, given by; RCT ≤ 130 (40/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Damping resistors not required on R versions.
3. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire OR'ed.
4. The power bypassing capacitor must be located close to the device with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the device. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

FIGURE 2: Typical Application Diagram

SSI 32R510A/510AR
4, 6-Channel
Read/Write Devices

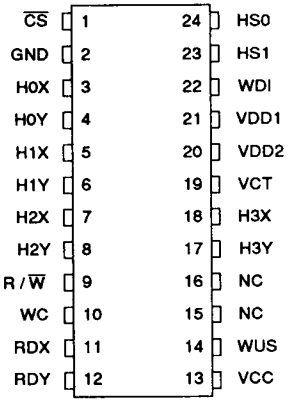
PACKAGE PIN DESIGNATIONS
(Top View)



6-CHANNEL
28-LEAD SOL

THERMAL CHARACTERISTICS

PACKAGE		θja
24-Lead	SOL	80°C/W
28-Lead	SOL	70°C/W



4-CHANNEL
24-LEAD SOL

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R510A		
4-Channel SOL	32R510A-4CL	32R510A-4CL
6-Channel SOL	32R510A-6CL	32R510A-6CL
SSI 32R510AR with Internal Damping Resistor		
4-Channel SOL	32R510AR-4CL	32R510AR-4CL
6-Channel SOL	32R510AR-6CL	32R510AR-6CL

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