Octal transceiver/register, non-inverting (3-State)

54ABT652

FEATURES

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 3-State outputs
- Output capability: +48mA/–24mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 54ABT652 high–performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 54ABT652 transceiver/register consists of bus transceiver circuits with 3-State outputs, D-type flip–flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

ORDERING INFORMATION

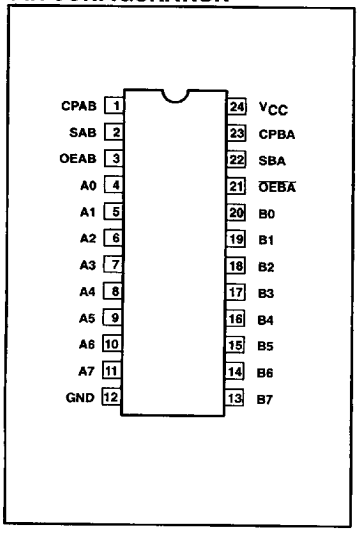
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24–pin Ceramic DIP	54ABT652/BLA	GDIP3-T24
28–pin Ceramic LLCC	54ABT652/B3A	CQCC2-N28

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

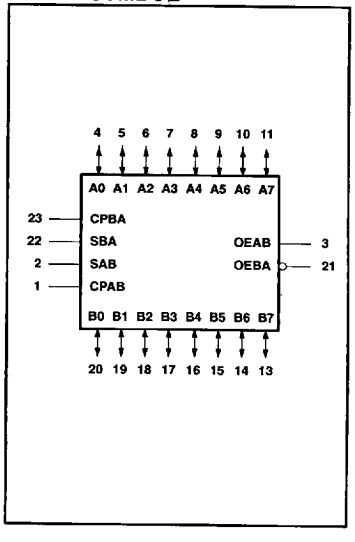
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3, 21	OEAB / $\overline{OEBA}$	A to B Output Enable input / B to A Output Enable input (active–Low)
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

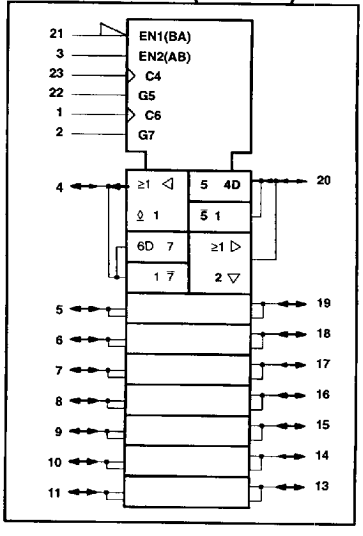
PIN CONFIGURATION



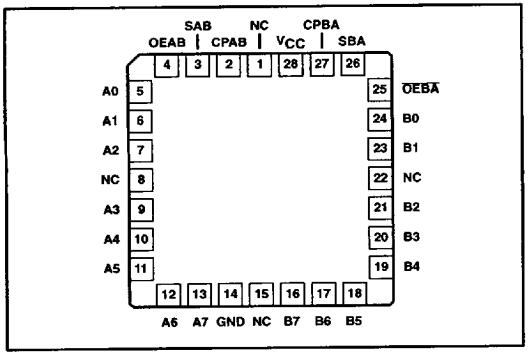
LOGIC SYMBOL



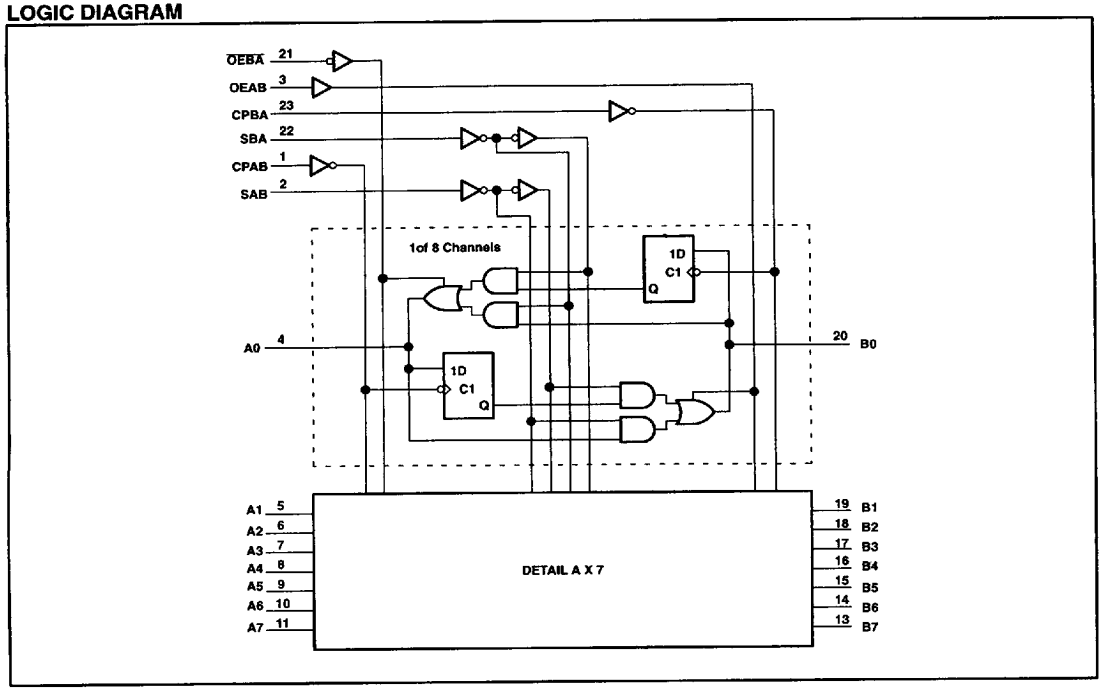
LOGIC SYMBOL (IEEE/IEC)



LLCC LEAD CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

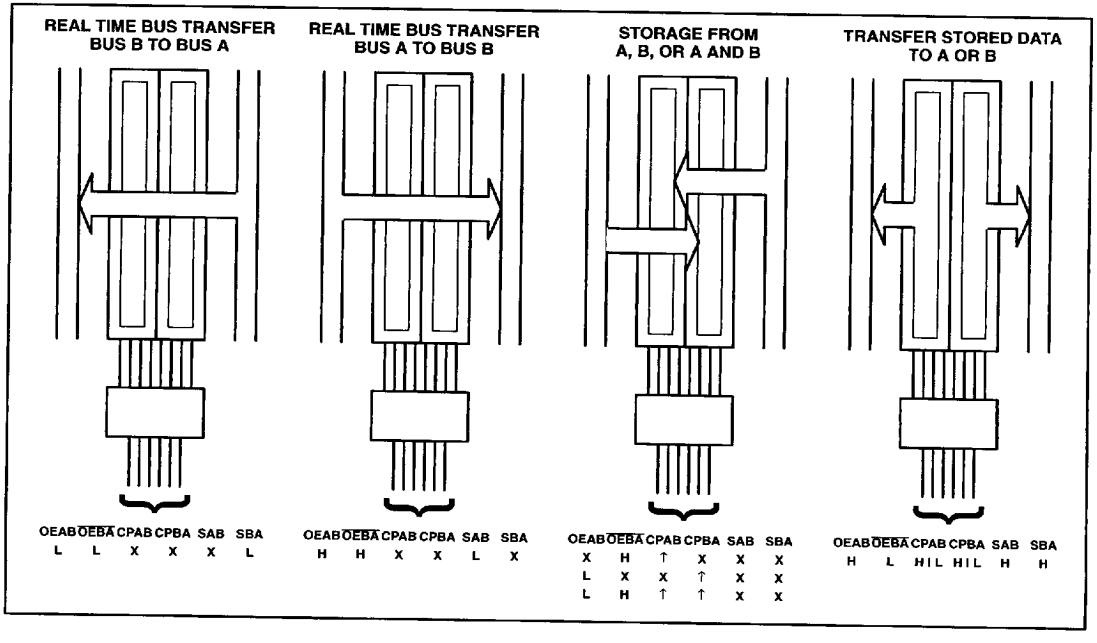
INPUTS						DATA I/O		OPERATING MODE
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low–to–High transition of the clock.
** If both Select controls (SAB and SBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 54ABT652.

The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	96	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High–level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High–level output current		–24	mA
I_{OL}	Low–level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free–air temperature range	–55	+125	°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted: V_{CC} = MAX, $V_I = V_{IL}$ or V_{IH}, $T_{amb} = -55$ to 125°C

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS V_{CC} = 5.0V±10% T_{amb} = −55 to +125°C			UNIT
				MIN	TYP	MAX	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2	V
V_{OH}	High–level output voltage		V_{CC} = 4.5V; I_{OH} = −3mA	2.5	3.5		V
			V_{CC} = 5.0V; I_{OH} = −3mA	3.0	4.0		V
			V_{CC} = 4.5V; I_{OH} = −24mA	2.0	2.8		V
V_{OL}	Low–level output voltage		V_{CC} = 4.5V; I_{OL} = 48mA		0.37	0.55	V
I_I	Input leakage current	Control pins	V_I = GND or 5.5V		±0.01	±1.0	µA
		Data pins[6]	V_I = GND or 5.5V		±5	±100	µA
$I_{IH} + I_{OZH}$	3–State output High current		V_O = 2.7V; $V_I = V_{IL}$ or 3.0V[7]		0.02	10	µA
$I_{IL} + I_{OZL}$	3–State output Low current		V_O = 0.5V; $V_I = V_{IL}$ or 3.0V[7]		−0.02	−10	µA
I_O	Output current[4]		V_O = 2.5V; V_I = GND or V_{CC}	−50	−80	−180	mA
I_{CCH}	Quiescent supply current		Outputs High, V_I = GND or V_{CC}		10	250	µA
I_{CCL}			Outputs Low, V_I = GND or V_{CC}		20	30	mA
I_{CCZ}			Outputs 3–State; V_I = GND or V_{CC}		10	250	µA
ΔI_{CC}	Additional supply current per input pin[5]		One input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5	mA
I_{OFF}	Power Off Leakage Current		V_{CC} = 0V; V_I or $V_O \leq$ 4 5V	−100	1.0	100	µA
I_{CEX}	Output High Leakage Current		V_{CC} = 5.5V; V_O = 5.5V		0.03	50	µA

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -55 to +125°C V_{CC} = +5.0V ±10%		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	17	125	200		125[10]		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	17	2.2 1.7	5.3 5.9	6.8 7.4	1.4 1.2	7.8 8.4	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	18	1.5 1.5	4.4 4.4	5.7 5 7	1.5 1.5	7.7 6.7	ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	19	1.5 1.5	4.6 5.4	5.9 6.7	1.2 1.2	7.4 7.7	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An	21 22	1.3 2.5	3.3 4.5	4.6 6.8	1.3 2.0	5 6 7.8	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An	21 22	1.5 1.5	6.2 5.0	7.7 6 3	1.5 1.5	8.2 7.3	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	21 22	1.8 2.9	3.8 4.9	6.1 6.5	1.7 2.2	7.7 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	21 22	1.5 1.5	4.5 4.1	5.7 5.3	1.0 1.5	6.9 6.3	ns

AC SETUP REQUIREMENTS[8, 9]

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

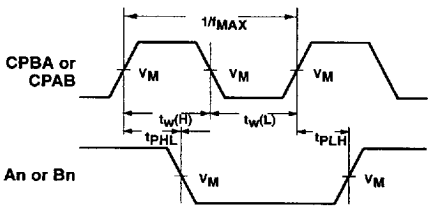
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -55 to +125°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time An to CPAB, Bn to CPBA	20	1.0 1.0	1.0 1.0		1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time An to CPAB, Bn to CPBA	20	0.0 0.0	0.0 0.0		0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	17	2.0 2.0	2.0 2.0		2.0 2.0		ns

NOTES:

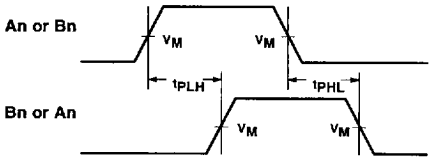
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. The performance capability of a high–performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
5. This is the increase in supply current for each input at 3.4V.
6. Input leakage on transceiver data pins also includes I_{OZH} or I_{OZL} current from the output circuitry.
7. To accommodate tester limitations, I_{OZ} tests are tested with V_{IH} = 3.0V, but 2.0V V_{IH} is guaranteed.
8. t_{set} and t_{hold} limits that are less than 3.0ns are guaranteed, but not tested to 3.0ns due to tester limitations.
9. t_w limits that are less than 6.0ns are guaranteed, but only tested to 6.0ns due to tester limitations.
10. Guaranteed by design, but not tested.

AC WAVEFORMS

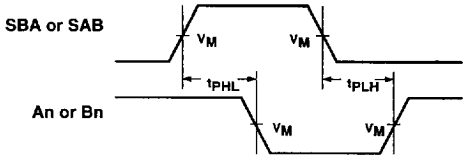
V_M = 1.5V, V_{IN} = GND to 3.0V



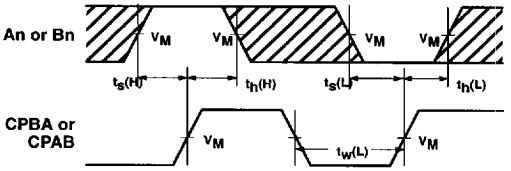
Waveform 17. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



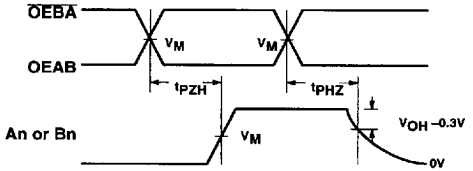
Waveform 18. Propagation Delay, An to Bn or Bn to An



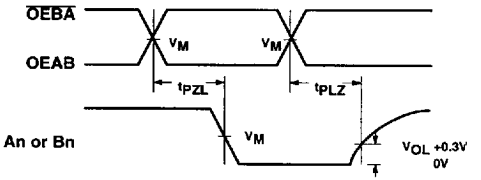
Waveform 19. Propagation Delay, SBA to An or SAB to Bn



Waveform 20. Data Setup and Hold Times



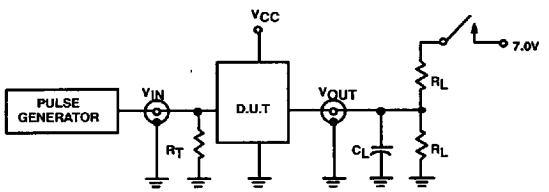
Waveform 21. 3–State Output Enable Time to High Level and Output Disable Time from High Level



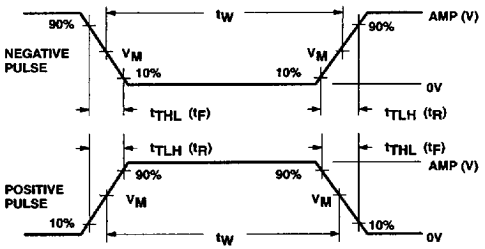
Waveform 22. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3–State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.