National Semiconductor

PRELIMINARY

Comlinear CLC952B
12-bit, 48MSPS Monolithic A/D Converter

General Description

The Comlinear CLC952B is a monolithic 12-bit, 48MSPS analog-to-digital converter subsystem. The device has been optimized for digital communications receivers and other applications where high resolution, high sampling rate, wide dynamic range, low power dissipation, and compact size are required. The chip includes a linear track-and-hold, a bandgap voltage reference and a proprietary 12-bit multi-stage quantizer.

The CLC952B is fabricated in a 0.8 micron BiCMOS process. The part features a 76dBc spurious-free dynamic range (SFDR) and 65dB signal-to-noise ratio (SNR). It is comprehensively tested at 40.96MSPS. Output registers and control functions are TTL compatible. The 28-pin SSOP package provides an extremely small footprint for applications where space is a critical consideration. The CLC952B operates from standard ±5V power supplies and features a >60dB PSRR for excellent noise isolation. The CLC952B operates over the industrial temperature range of -40 to +85°C. National Semiconductor thoroughly tests each part to verify full compliance with the guaranteed specifications.

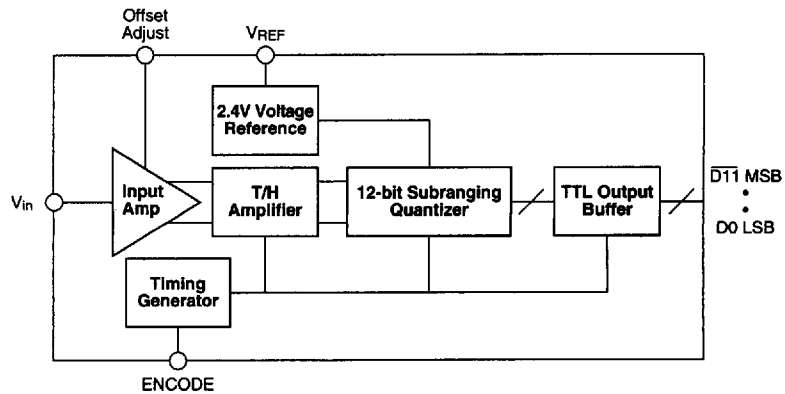
Features

- 48MSPS
- Wide dynamic range
  SFDR: 76dBc
  SNR: 65dB
- Low power dissipation: 625mW
- Ground centered, DC-coupled analog input
- Excellent PSRR: >60dB
- Very small package: 28-pin SSOP
- Low cost

Applications

- Cellular base-stations
- Digital communications
- Infrared/CCD imaging
- IF sampling
- Electro-optics
- Instrumentation
- Medical imaging
- High definition video

CLC952B Block Diagram



CLC952B Electrical Characteristics (V_{CC} = +5V, V_{EE} = -5V, 40.96MSPS; unless specified)

PARAMETERS	CONDITIONS	TEMP	RATINGS			UNITS	NOTES
			MIN	TYP	MAX		2
DYNAMIC PERFORMANCE							
small-signal bandwidth	V_{in} = 1/4FS	+25°C		250		MHz	
large-signal bandwidth	V_{in} = FS	+25°C		200		MHz	
slew rate		+25°C		200		V/µs	
overvoltage recovery time	V_{in} = 1.5FS (0.01%)	+25°C		18		ns	
effective aperture delay		+25°C		-0.25		ns	
aperture jitter		+25°C		1.0		ps(rms)	
NOISE AND DISTORTION (40.96MSPS)							
signal-to-noise ratio (w/o 10 harmonics)							
0.41MHz	FS	+25°C	63	65		dB	1
	FS	+85°C	62.5	64.5		dB	3
	FS	-40°C		63		dB	
9.67MHz	FS	+25°C	62.5	64		dB	1
	FS	+85°C	61.5	64		dB	3
	FS	-40°C		62.5		dB	
19.5MHz	FS	+25°C	62	63.5		dB	1
	FS	+85°C	61.5	63.5		dB	3
	FS	-40°C		61.5		dB	
spurious-free dynamic range							
0.41MHz	FS-1dB	+25°C		75.5		dBc	1
	FS-1dB	+85°C	71	73		dBc	3
	FS-1dB	-40°C		74.5		dBc	
9.67MHz	FS-1dB	+25°C	70	76		dBc	1
	FS-1dB	+85°C	70	75.5		dBc	3
	FS-1dB	-40°C		75		dBc	
19.5MHz	FS-1dB	+25°C	70	77		dBc	1
	FS-1dB	+85°C	73	78		dBc	3
	FS-1dB	-40°C		71.5		dBc	
NOISE AND DISTORTION (48MSPS)							
signal-to-noise ratio (w/o 10 harmonics)							
19.5MHz	FS	+25°C		60.5		dB	
spurious-free dynamic range							
19.5MHz	FS-1dB	+25°C		65.0		dBc	
DC ACCURACY AND PERFORMANCE							
differential non-linearity	DC; FS	+25°C		0.3		LSB	
integral non-linearity	DC; FS	+25°C		1.5		LSB	
bipolar offset error		+25°C		2.1		mV	
bipolar offset error		Full			20.0	mV	4
bipolar gain error		+25°C		1.5		%FS	
bipolar gain error		Full			10.0	%FS	4
ANALOG INPUT AND PERFORMANCE							
analog input resistance		+25°C		500		Ω	
analog input capacitance		+25°C		2		pF	
DIGITAL INPUTS							
input voltage	logic LOW	Full			0.8	V	1,4
	logic HIGH	Full	2.0			V	1,4
input current	logic LOW	Full		1	5	µA	1,4
	logic HIGH	Full		4.0	25	µA	1,4
output voltage	logic LOW	Full			0.4	V	1,4
	logic HIGH	Full	2.4			V	1,4
TIMING							
maximum conversion rate		Full			48	MSPS	1,4
minimum conversion rate		Full		0.3		MSPS	4
pulse width high		Full	12.2	12.2		ns	4
pulse width low		Full	10.5	12.2		ns	4
pipeline delay		Full			1.0	clk cycle	4
output propagation delay		+25°C		15		ns	

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PARAMETERS	CONDITIONS	TEMP	RATINGS			UNITS	NOTES
			MIN	TYP	MAX		2
POWER REQUIREMENTS							
+5V supply current	41MSPS	+25°C		55		mA	1
+5V supply current	41MSPS	Full			62.0	mA	4
-5V supply current	41MSPS	+25°C		79		mA	1
-5V supply current	41MSPS	Full			88.0	mA	4
nominal power dissipation	41MSPS	+25°C		670		mW	
V_{EE} power supply rejection ratio		+25°C		72		dB	
V_{CC} power supply rejection ratio		+25°C		60		dB	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes

1) These parameters are 100% tested at 25°C.
2) Typical specifications are the mean values of the distributions of deliverable converters tested to date.
3) Min/max data over temperature is based on the 5 sigma limit for deliverable converters tested to date.
4) Full temperature range is -40°C to +85°C

Absolute Maximum Ratings

positive supply voltage (V_{CC})	-0.5V to +6V
negative supply voltage (V_{EE})	+0.5V to -6V
differential voltage between any two grounds	<200mV
analog input voltage range	V_{EE} to V_{CC}
digital input voltage range	-0.5V to +V_{CC}
output short circuit duration (one-pin to ground)	infinite
junction temperature	175°C
storage temperature range	-65°C to 150°C
lead solder duration (+300°C)	10sec

Note: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceablity of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Recommended Operating Conditions

positive supply voltage (V_{CC})	+5V ±5%
negative supply voltage (V_{EE})	-5V ±5%
differential voltage between any two grounds	<10mV
analog input voltage range	±0.5V
operating temperature range	-40°C to +85°C

Package Thermal Resistance

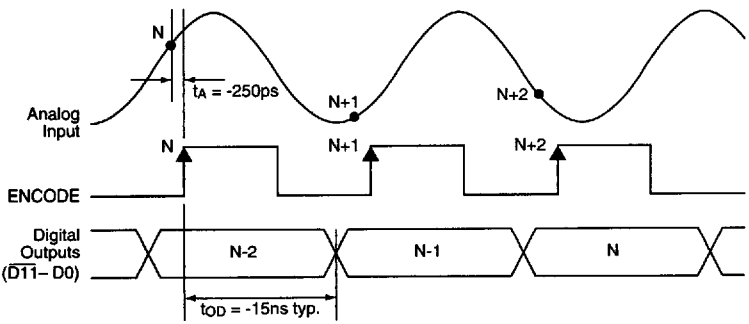
Package	θ_{JA}	θ_{JC}
28-pin SSOP	80°C/W	32°C/W

Reliability Information

Transistor count	3000

Ordering Information

Model	Temperature Range	Description
CLC952BAJMSA	-40°C to +85°C	28-pin SSOP
CLC952PCASM		Fully loaded evaluation board with CLC952B ... ready for test.

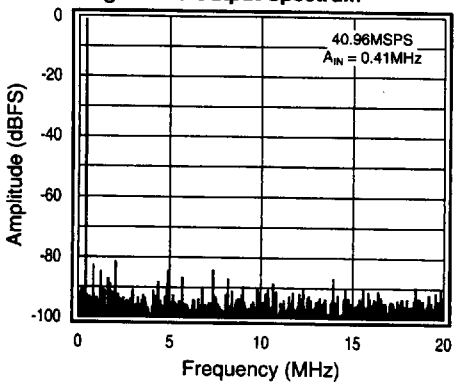


CLC952B Timing Diagram

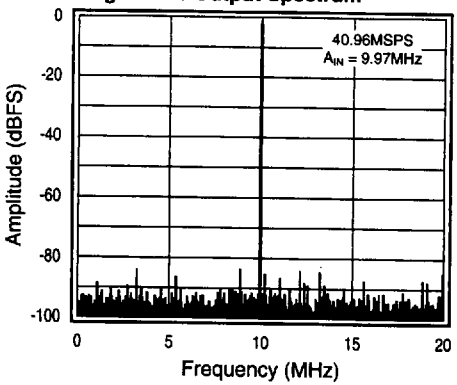
NOTE: At sample rates >45MSPS, it may be helpful to apply a >50% ($t_{PH} > t_{PL}$) duty cycle clock source to the ENCODE input to improve SNR and DNL. At sample rates <300kSPS, it is necessary to apply a <50% ($t_{PH} < t_{PL}$) duty cycle clock source to the ENCODE input to improve performance.

CLC952B Typical Performance Characteristics (V_{CC} = +5V, V_{EE} = -5V)

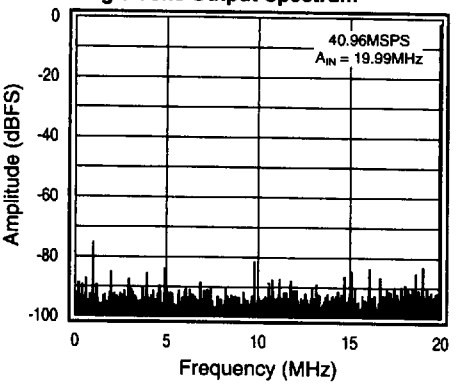
Single Tone Output Spectrum



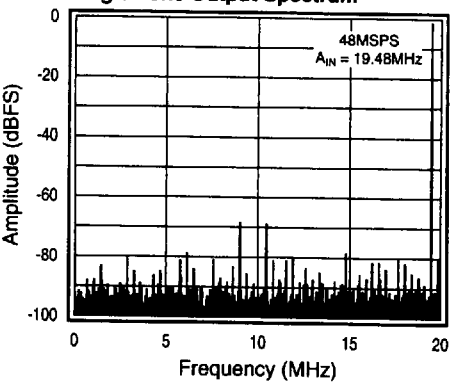
Single Tone Output Spectrum



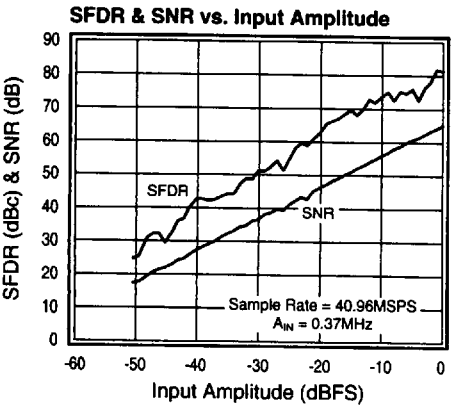
Single Tone Output Spectrum



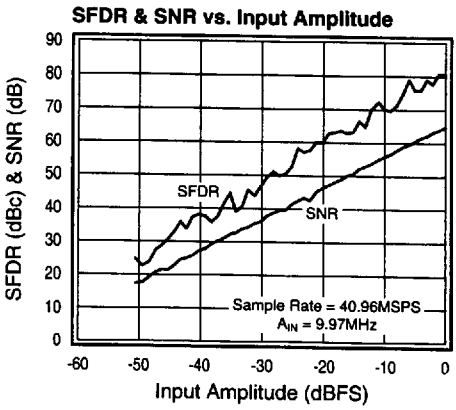
Single Tone Output Spectrum



SFDR & SNR vs. Input Amplitude

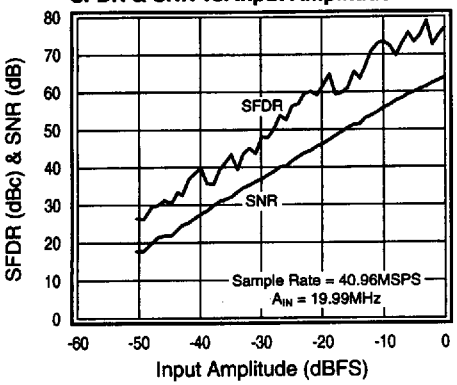


SFDR & SNR vs. Input Amplitude

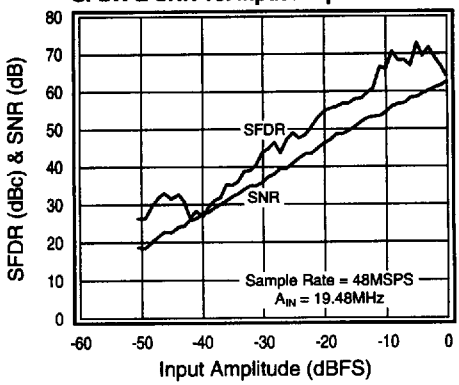


CLC952B Typical Performance Characteristics (V_{CC} = +5V, V_{EE} = -5V)

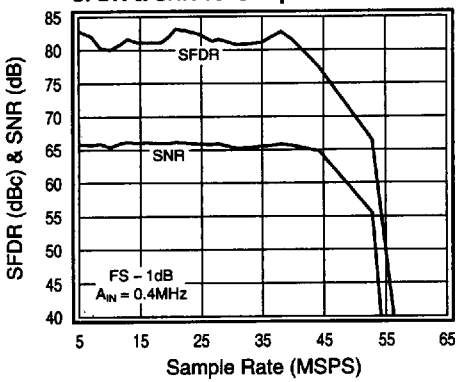
SFDR & SNR vs. Input Amplitude



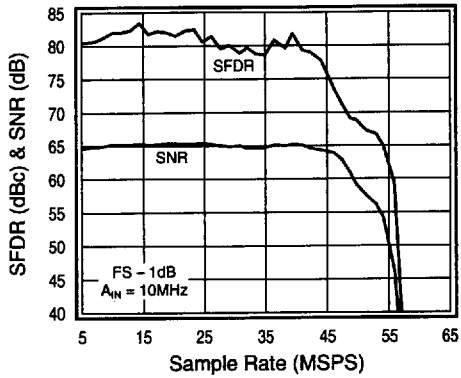
SFDR & SNR vs. Input Amplitude



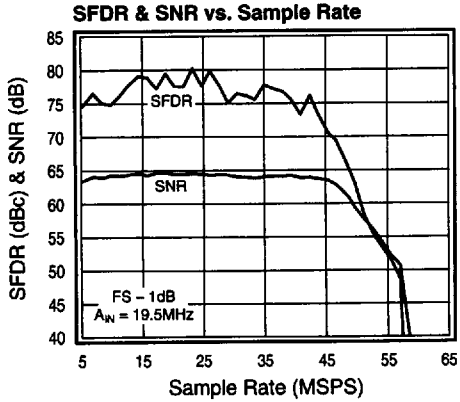
SFDR & SNR vs. Sample Rate



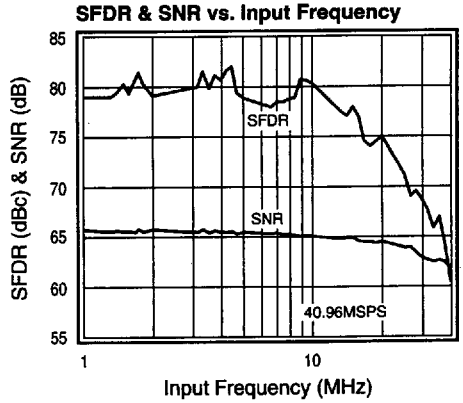
SFDR & SNR vs. Sample Rate



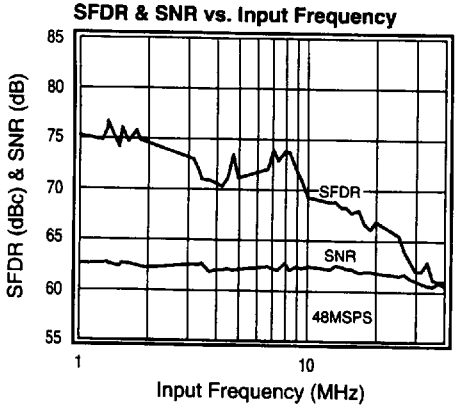
SFDR & SNR vs. Sample Rate

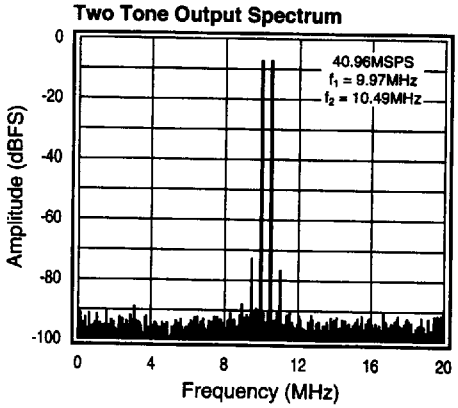


SFDR & SNR vs. Input Frequency

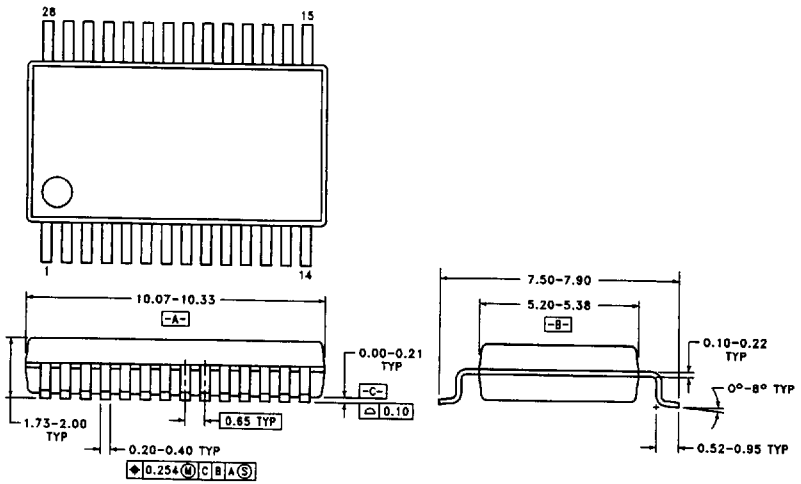


CLC952B Typical Performance Characteristics (V_{CC} = +5V, V_{EE} = -5V)





CLC952B Packaging Dimensions



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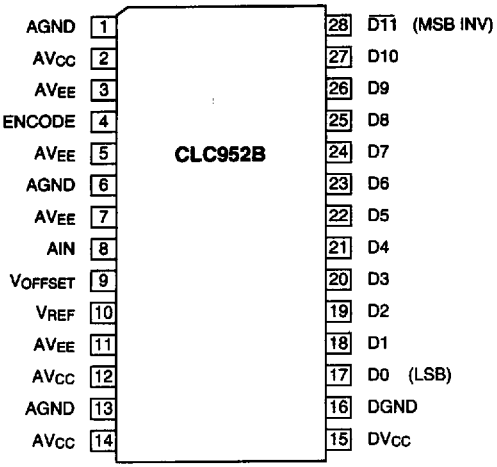
CLC952B Pin Definitions



AGND (Pins 1, 6, 13) Analog circuit ground.

AV_{CC} (Pins 2, 12, 14) +5V power supply for the analog section. Bypass to analog ground with a 0.1µF capacitor.

AV_{EE} (Pins 3, 5, 7,11) -5V power supply for the analog section. Bypass to analog ground with a 0.1µF capacitor.

ENCODE (Pin 4) ENCODE initiates a new data conversion cycle on each rising edge. Logic for this input is standard TTL. 50% duty cycle is recommended for full compliance with the guaranteed specifications.

AIN (Pin 8) Ground-centered, DC-coupled analog input with a $1V_{pp}$ maximum input range from -0.5V to +0.5V. Analog input impedance is approximately 500Ω.

V_{OFFSET} (Pin 9) Voltage offset control. Sets the midpoint of the analog input range. Normally left floating. Ratio of applied voltage to effective offset is 200:1. (1V applied to V_{OFFSET} produces 5mV midpoint offset.)

V_{REF} (Pin 10) Internal voltage reference. Nominally +2.4V. V_{REF} can be pulled up or down with a voltage source to program gain and input range.

DV_{CC} (Pin 15) +5V power supply for the digital section. Bypass to digital ground with a 0.1µF capacitor.

DGND (Pin 16) Digital ground.

D0-D11 (Pins 17-28) Digital data outputs are CMOS and TTL compatible. D0 is the LSB and D11 is the MSB. MSB is inverted. Output coding is two's complement.