

AM / FM - PLL

Description

The U4284BM is an integrated circuit in BICMOS technology for frequency synthesizer. It performs all the functions of a PLL radio tuning system and is controlled by

I²C bus. The device is designed for all frequency synthesizer applications of radio receivers, as well as RDS (Radio Data System) applications.

Features

- Reference oscillator up to 15 MHz
- Two programmable 16 bit dividers adjustable from 2 to 65535
- Fine tuning steps:
AM ≥ 1 kHz
FM ≥ 2 kHz
- 4 programmable switching outputs (open drain up to 20 V)
- Few external component requirements due to integrated loop-push-pull stage for AM/FM
- High signal/noise ratio

Block diagram

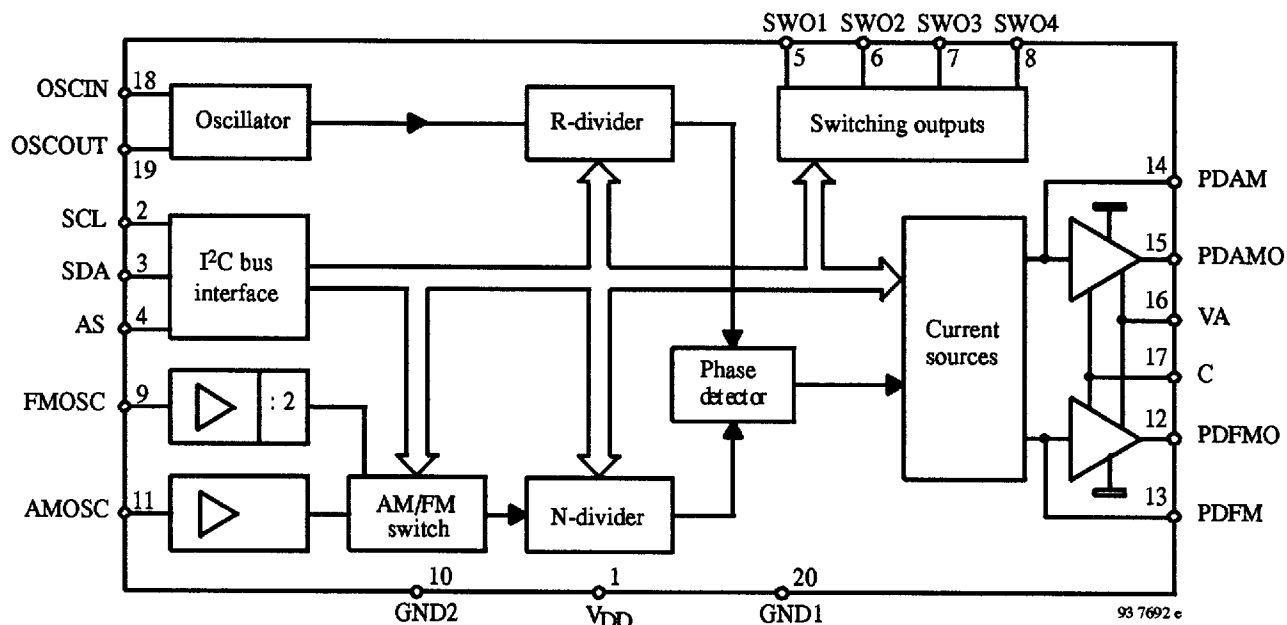
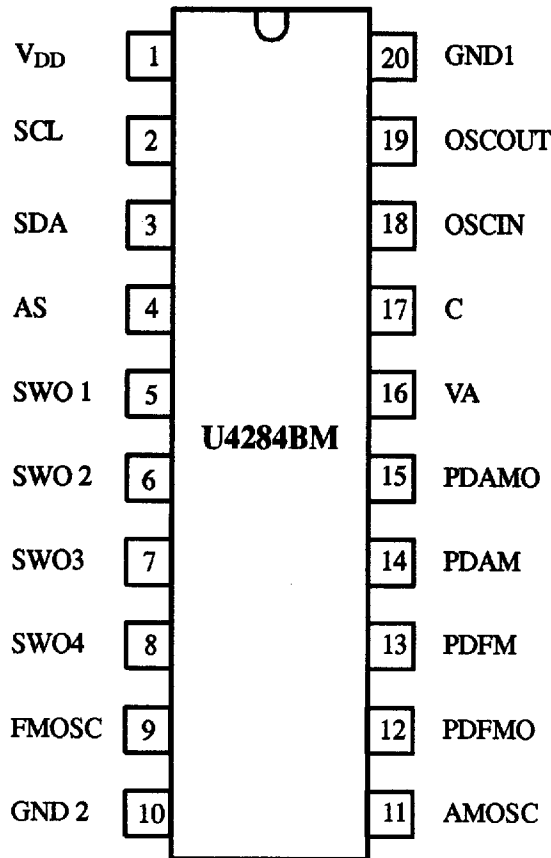


Figure 1

Pin description



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Pin	Symbol	Function
1	V _{DD}	Supply voltage
2	SCL	I ² C bus clock
3	SDA	I ² C bus data
4	AS	Address selection
5	SWO 1	Switching output 1
6	SWO 2	Switching output 2
7	SWO 3	Switching output 3
8	SWO 4	Switching output 4
9	FMOSC	FM oscillator input
10	GND 2	Ground 2 (analogue)
11	AMOSC	AM oscillator input
12	PDFMO	FM analogue output
13	PDFM	FM current output
14	PDAM	AM current output
15	PDAMO	AM analogue output
16	VA	Analogue supply voltage
17	C	Capacitor
18	OSCIN	Oscillator input
19	OSCOUT	Oscillator output
20	GND1	Ground 1 (digital)

Functional description

The U4284BM is controlled via the 2-wire I²C bus. For programming there are one module address byte, two subaddress bytes and five data bytes.

The module address contains a programmable address bit A 1 which with address select input AS (pin 4) makes it possible to operate two U4284BM in one system. If bit A 1 is identical with the status of the address select input AS, the chip is selected.

The subaddress determines which one of the data bytes is transmitted first. If subaddress of R-divider is transmitted, the sequence of the next data bytes is DB 0 (Status), DB 1 and DB 2.

If subaddress of N-divider is transmitted, the sequence of the next data bytes is DB 3 and DB 4. The bit organisation of the module address, subaddress and 5 data bytes are shown in figure 2.

Each transmission on the I²C bus begins with the "START"- condition and has to be ended by the "STOP"-condition (see figure 3).

The integrated Circuit U4284BM has two separate inputs for AM and FM oscillator. Pre-amplified AM signal is directed to the 16 bit N-divider via AM/FM switch, whereas (pre-amplified) FM signal is first divided by a fixed prescaler (:2). AM/FM switch is controlled by software. Tuning steps can be selected by 16 bit R-divider. Further there is a digital memory phase detector. There are two separate current sources for AM and FM amplifier (charge pump) as given in electrical characteristics. It allows independent adjustment of gain, whereby providing high current for high speed tuning and low current for stable tuning.

Bit organisation

	MSB							LSB
Module address	1	1	0	0	1	0	0/1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Subaddress (R-divider)	X	X	X	X	0	1	X	X
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Subaddress (N-divider)	X	X	X	X	1	1	X	X
------------------------	---	---	---	---	---	---	---	---

	MSB							LSB
Data byte 0 (Status)	SWO1	SWO2	SWO3	SWO4	AM/ FM	PD ANA	PD POL	PD CUR
	D7	D6	D5	D4	D3	D2	D1	D0

Data byte 1	2^{15}	R-divider						2^8
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Data byte 2	2^7	R-divider						2^0
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Data byte 3	2^{15}	N-divider						2^8
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Data byte 4	2^7	N-divider						2^0
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	LOW	HIGH
AM/FM	FM-operation	AM-operation
PD - ANA	PD analogue	TEST
PD - POL	Negative polarity	Positive polarity
PD - CUR	Output current 2	Output current 1

Figure 2

Transmission protocol

	MSB	LSB									
S	Address		A	Subaddress	A	Data 0	A	Data 1	A	Data 2	A P
	A7	A0		R-divider							

	MSB	LSB							
S	Address		A	Subaddress	A	Data 3	A	Data 4	A P
	A7	A0		N-divider				A	

S = Start P = Stop A = Acknowledge

Figure 3

Absolute maximum ratings

Parameters	Symbol	Value	Unit
Supply voltage Pin 1	V_{DD}	-0.3 to +6	V
Input voltage Pin 2, 3, 4, 9, 11, 18, 19	V_I	-0.3 to $V_{DD} + 0.3$	V
Output current Pin 3, 5, 6, 7, 8	I_O	-1 to +5	mA
Output drain voltage Pin 5, 6, 7, 8	V_{OD}	20	V
Analogue supply voltage Pin 16	V_A	8 to 16	V
With 220 Ω seriell resistance 2 minutes ²	V_A	24	V
Output current Pin 12, 15	I_{AO}	-1 to +20	mA
Ambient temperature range	T_{amb}	-25 to +85	°C
Storage temperature range	T_{stg}	-40 to +125	°C
Junction temperature	T_j	125	°C
Electrostatic handling (MIL Standard 883C) except Pins 12, 15 and 17	$\pm V_{ESD}$	2000	V

² corresponding our application circuit (page 7)

Thermal resistance

Parameters	Symbol	Maximum	Unit
Junction ambient	R_{thJA}	160	K/W

Electrical characteristics

$V_{DD} = 5\text{ V}$, $V_A = 12\text{ V}$, $T_{amb} = 25^\circ\text{C}$, unless otherwise specified

Parameters	Test conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 1	V_{DD}	4.5	5.0	5.5	V
Quiescent supply current	AM-mode FM-mode	Pin 1 I_{DD}		4.0 8.5	7.0 15.0	mA
FM Input sensitivity, $R_G = 50\ \Omega$ FMOSC						
$f_i = 70$ to 120 MHz	Pin 9	V_{SFM}	25			mV
$f_i = 120$ to 160 MHz	Pin 9	V_{SFM}	50			mV
AM Input Sensitivity, $R_G = 50\ \Omega$ AMOSC						
$f_i = 0.5$ to 35 MHz	Pin 11	V_{SAM}	25			mV
Oscillator Input Sensitivity, $R_G = 50\ \Omega$ OSCIN						
$f_i = 0.1$ to 15 MHz	Pin 18	V_{SOSC}	100			mV
Switching Output SWO 1, SWO 2, SWO 3, SWO 4 (Open Drain)						
Output voltage LOW	Pin 5, 6, 7, 8 $I_L = 1\text{ mA}$	V_{SWOL}		200	400	mV
Output leakage current HIGH	Pin 5, 6, 7, 8 $V_5, V_6, V_7, V_8 = 20\text{ V}$	I_{OHL}			100	nA
Phase Detector PDFM						
Output current 1	Pin 13	$\pm I_{PDFM}$	400	500	600	μA
Output current 2	Pin 13	$\pm I_{PDFM}$	100	125	150	μA
Leakage current	Pin 13	$\pm I_{PDFML}$			20	nA
Phase Detector PDAM						
Output current 1	Pin 14	$\pm I_{PDAM}$	75	100	125	μA
Output current 2	Pin 14	$\pm I_{PDAM}$	20	25	30	μA
Leakage current	Pin 14	$\pm I_{PDAML}$			20	nA
Analogue Output PDFMO, PDAMO						
Saturation voltage LOW HIGH	Pin 12, 15 $I = 15\text{ mA}$	V_{satL} V_{satH}	11.5	200 11.95	400	mV V
I ² C Bus SCL, SDA, AS						
Input voltage HIGH LOW	Pin 2, 3, 4	V_{iBUS}	3.0 0		V_{DD} 1.5	V V
Output voltage Acknowledge LOW	Pin 3 $I_{SDA} = 3\text{ mA}$	V_O			0.4	V
Clock frequency	Pin 2	f_{SCL}			100	kHz
Rise time SDA, SCL	Pin 2, 3	t_r			1	μs
Fall time SDA, SCL	Pin 2, 3	t_f			300	ns
Period of SCL HIGH LOW	Pin 2 HIGH LOW	t_H t_L	4.0 4.7			μs μs

Parameters	Test conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Setup Time						
Start condition		t_{sSTA}	4.7			μs
Data		t_{sDAT}	250			ns
Stop condition		t_{sSTOP}	4.7			μs
Time the bus must be free before a new transmission can be started		t_{wSTA}	4.7			μs
Hold Time						
Start condition		t_{hSTA}	4.0			μs
DATA		t_{hDAT}	0			μs

Bus timing

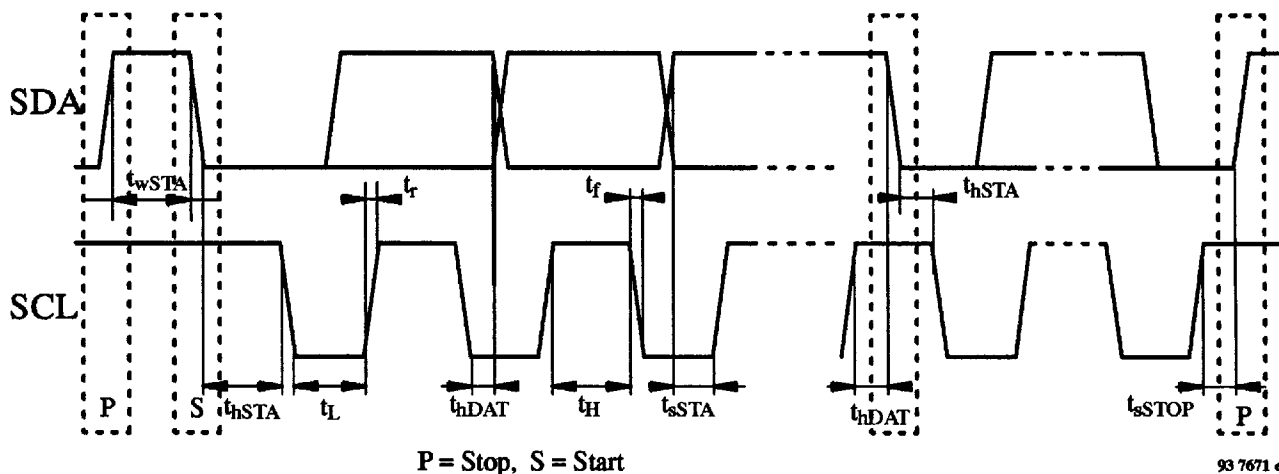
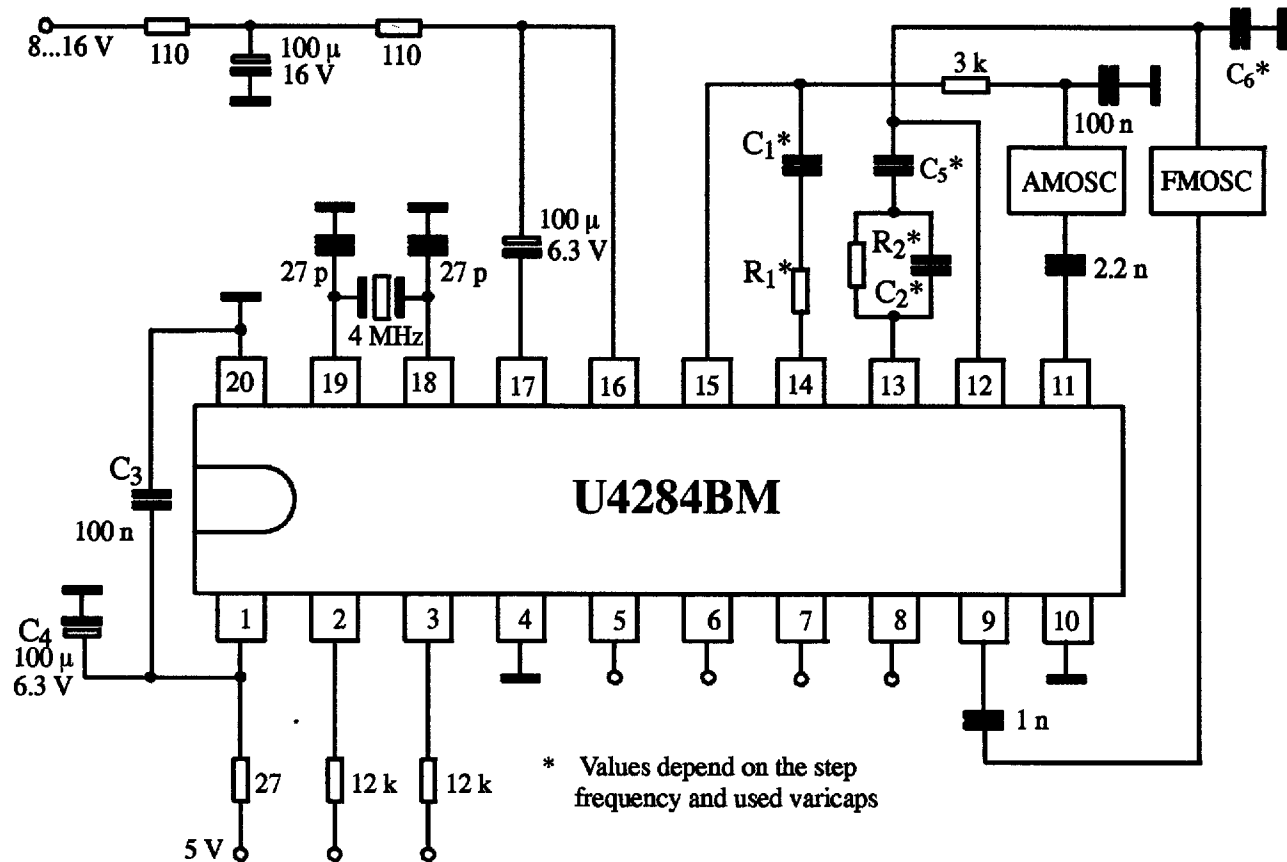


Figure 4

The following hints are recommended:

- $C_3 = 100 \text{ nF}$ should be very close to Pin 1 (V_{DD}) and Pin 20 (GND 1)
- GND 2 (Pin 10 - analogue ground) and GND 1 (Pin 20 - digital ground) must be connected according to figure 6
- 4 MHz quartz must be very close to Pin 18 and Pin 19
- Components of the charge pump (C_1/R_1 for AM and C_2/R_2 for FM) should be very close to Pin 14 with respect to Pin 13.

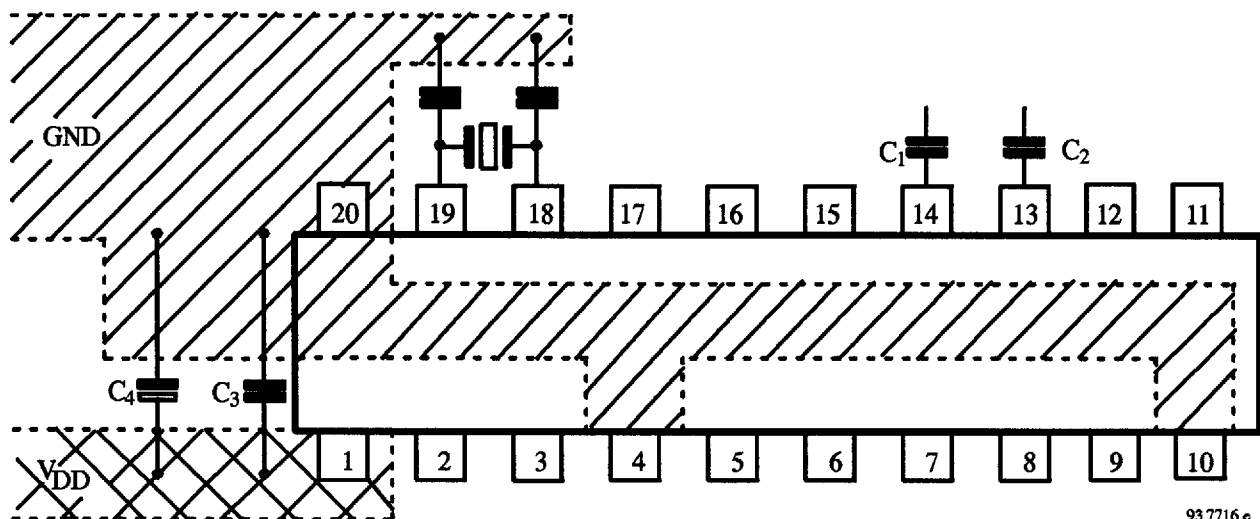
Application circuit



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Figure 5

PCB-layout



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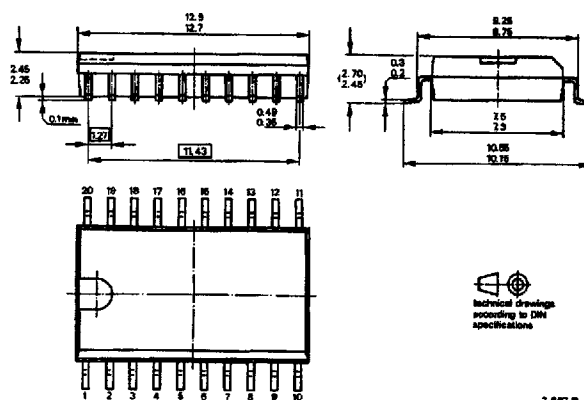
Figure 6

Ordering and Package Information

Extended type number	Package	Remarks
U4284BM-BFP	SO 20 plastic	
U4284BM-BFPG3	SO 20 plastic	Taping according to IEC-286-3
U4284BM-BFS	SSO 20 plastic	
U4284BM-BFSG3	SSO 20 plastic	Taping according to IEC-286-3

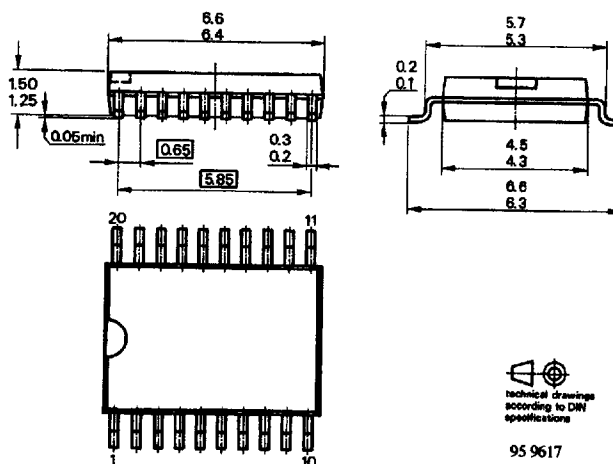
Dimensions in mm

Package: SO 20



2 697 0

Package: SSO 20



95 9617