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SYNCHRONOUS DRAM MODULE

512M Bytes (64M x 64 bits)

240 Pin DDR2 SDRAM Unbuffered DIMM

based on 8 pcs 64M x 8 DDR2 SDRAM 8K Refresh

FEATURES

- 240-pin, dual in-line memory module (DIMM)
- Fast data transfer rates: PC2-3200 or PC2-4200
- Utilizes 400 MT/s and 533 MT/s DDR2 SDRAM components
- VDD = +1.8V ± 0.1V, VDDQ = +1.8V ± 0.1V
- VDDSDP = +1.7V to +3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, /DQS) option
- Four-bit prefetch architecture
- Differential clock inputs (CK, /CK)
- Commands entered on each rising CK edge
- DQS edge-aligned with data for READs
- DQS center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four or eight internal device banks for concurrent operation
- Data mask (DM) for masking write data
- Programmable /CAS latency (CL): 3 and 4
- Posted /CAS additive latency (AL): 0, 1, 2, 3, and 4
- WRITE latency = READ latency - 1 t_{CK}
- Programmable burst lengths: 4 or 8
- READ burst interrupt supported by another READ
- WRITE burst interrupt supported by another WRITE
- Adjustable data-output drive strength
- Concurrent auto precharge option is supported
- Auto Refresh (CBR) and Self Refresh Mode
- 7.8125µs maximum average periodic refresh interval
- 64ms, 8,192-cycle refresh
- Off-chip driver (OCD) impedance calibration
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Gold edge contacts
- PCB : Height (1180mil), single sided component

ABSOLUTE MAXIMUM RATINGS

• Voltage Relative to GND	-1.0 to + 2.3V
• Operating Temperature	0 to + 65°C
• Storage Temperature	-55°C to + 100°C
• Short circuit Output Current	50mA
• Power Dissipation	8W

PART IDENTIFICATION

PART NO.	REF. CYCLE	SDRAM PACKAGE	PLATING
UG64T6400L8DU	8K	CSP	Gold

SPEED INFORMATION

Module Marking	CAS Latency	SPEED	
-4AL	CL3 (PC3200)	5.0ns	400Mps@
-5AL	CL4 (PC4200)	3.75ns	533Mps@

REVISION HISTORY

Mar 30, 2005

Rev - A Product brief released.

PIN ASSIGNMENT (Front View)

240-Pin DIMM

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	61	A4	121	VSS	181	VDDQ
2	VSS	62	VDDQ	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	VDD	124	VSS	184	VDD
5	VSS	65	VSS	125	DM0/DQS9	185	CK0
6	/DQS0	66	VSS	126	NC/ /DQS9	186	/CK0
7	DQS0	67	VDD	127	VSS	187	VDD
8	VSS	68	NC	128	DQ6	188	A0
9	DQ2	69	VDD	129	DQ7	189	VDD
10	DQ3	70	A10/AP	130	VSS	190	BA1
11	VSS	71	BA0	131	DQ12	191	VDDQ
12	DQ8	72	VDDQ	132	DQ13	192	/RAS
13	DQ9	73	/WE	133	VSS	193	/S0
14	VSS	74	/CAS	134	DM1/DQS10	194	VDDQ
15	/DQS1	75	VDDQ	135	NC/ /DQS10	195	ODT0
16	DQS1	76	NC	136	VSS	196	A13
17	VSS	77	ODT1	137	CK1	197	VDD
18	/RESET	78	VDDQ	138	/CK1	198	VSS
19	NC	79	VSS	139	VSS	199	DQ36
20	VSS	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	VSS
22	DQ11	82	VSS	142	VSS	202	DM4/DQS13
23	VSS	83	/DQS4	143	DQ20	203	NC/ /DQS13
24	DQ16	84	DQS4	144	DQ21	204	VSS
25	DQ17	85	VSS	145	VSS	205	DQ38
26	VSS	86	DQ34	146	DM2/DQS11	206	DQ39
27	/DQS2	87	DQ35	147	NC/ /DQS11	207	VSS
28	DQS2	88	VSS	148	VSS	208	DQ44
29	VSS	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	VSS
31	DQ19	91	VSS	151	VSS	211	DM5/DQS14
32	VSS	92	/DQS5	152	DQ28	212	NC/ /DQS14
33	DQ24	93	DQS5	153	DQ29	213	VSS
34	DQ25	94	VSS	154	VSS	214	DQ46
35	VSS	95	DQ42	155	DM3/DQS12	215	DQ47
36	/DQS3	96	DQ43	156	NC/ /DQS12	216	VSS
37	DQS3	97	VSS	157	VSS	217	DQ52
38	VSS	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	VSS
40	DQ27	100	VSS	160	VSS	220	CK2
41	VSS	101	SA2	161	NC	221	/CK2
42	NC	102	NC(TEST)	162	NC	222	VSS
43	NC	103	VSS	163	VSS	223	DM6/DQS15
44	VSS	104	/DQS6	164	NC	224	NC/ /DQS15
45	NC	105	DQS6	165	NC	225	VSS
46	NC	106	VSS	166	VSS	226	DQ54
47	VSS	107	DQ50	167	NC	227	DQ55
48	NC	108	DQ51	168	NC	228	VSS
49	NC	109	VSS	169	VSS	229	DQ60
50	VSS	110	DQ56	170	VDDQ	230	DQ61
51	VDDQ	111	DQ57	171	NC	231	VSS
52	CKE0	112	VSS	172	VDD	232	DM7/DQS16
53	VDD	113	/DQS7	173	A15	233	NC/ /DQS16
54	NC	114	DQS7	174	A14	234	VSS
55	NC	115	VSS	175	VDDQ	235	DQ62
56	VDDQ	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	VSS
58	A7	118	VSS	178	VDD	238	VDDSPD
59	VDD	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

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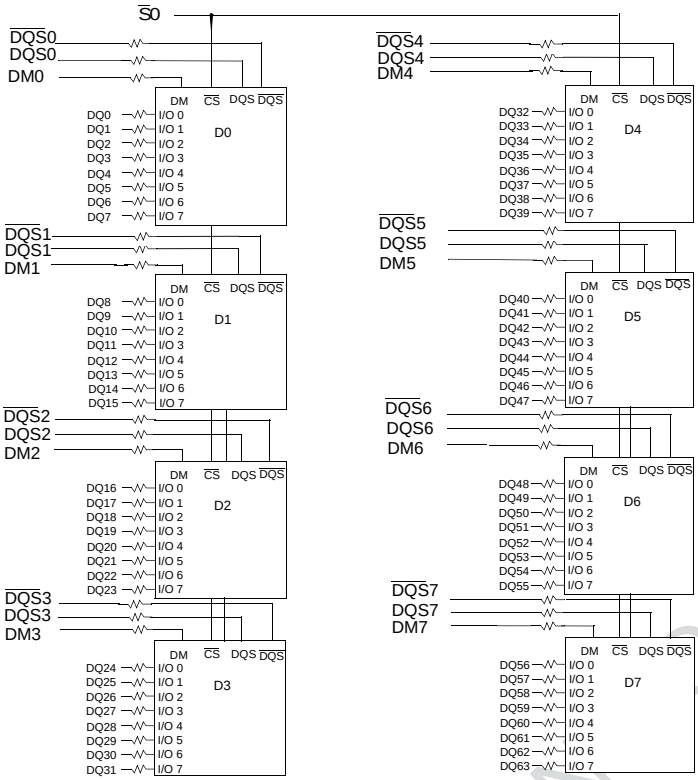
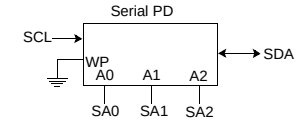
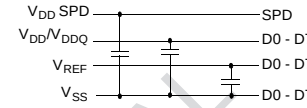
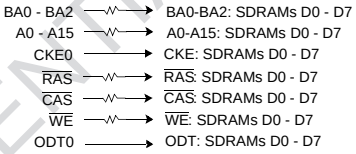
Functional Block Diagram









Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/$\overline{DQS}$/ODT/DM/CKE/$\overline{S}$ relationships must be maintained as shown.
3. DQ, DQS, DM/DQS/$\overline{DQS}$ resistors: Refer to associate topology diagram
4. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: Refer to associate topology diagram

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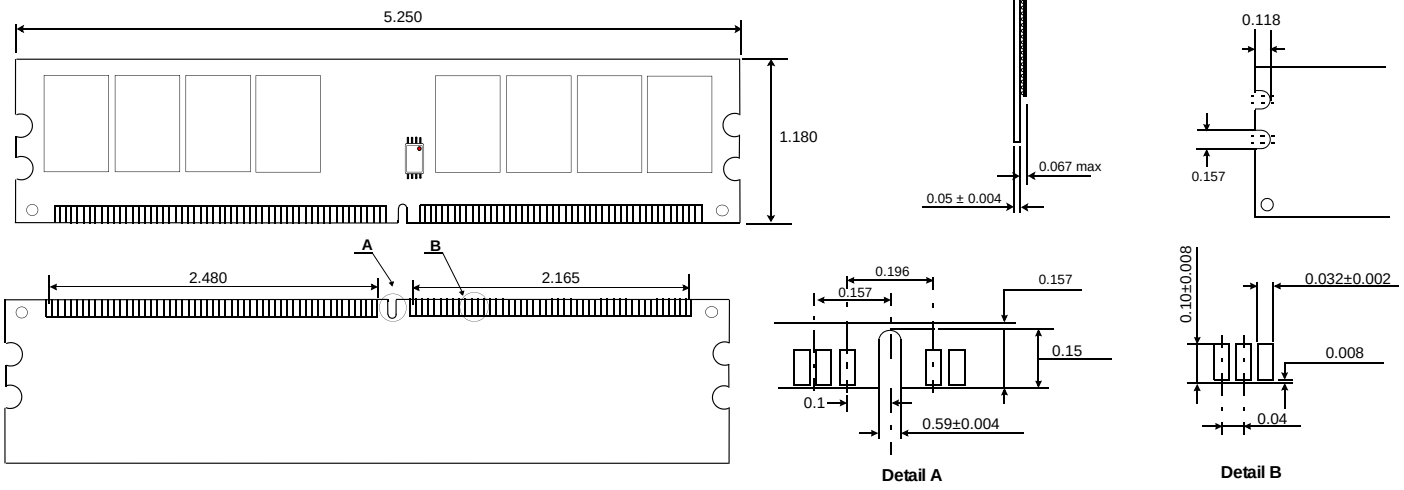
Physical Dimension



Tolerances : ± 0.005 unless otherwise specified

Units : Inches

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