256K x 32 Synchronous Graphics RAM

Features

- Fully synchronous; all signals registered on positive edge of system clock.
- Internal pipelined operation; column address can be changed every clock cycle.
- Dual internal banks for hiding row precharge; Each bank is 128k x 32.
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Burst Read with Single Write
- Programmable $\overline{CAS}$ Latency: 1, 2, 3
- 8 column Block Write and Write-per-Bit modes
- 100Mhz Block Write operation
- Two Color Registers
- Independent byte operation via DQM_{0-3}
- Auto Precharge and Auto Refresh modes
- 1K Refresh cycles/16ms
- 1K Refresh cycles/128ms for Self Refresh parts
- LVTTL- compatible inputs and outputs
- Single 3.3V $\pm$ 0.3
- 100-pin LQFP (0.65mm lead pitch)

Options	Marking
Timing 7R5ns Access (≤ 133 Mhz clock rate) 10ns Access (≤ 100 Mhz clock rate) 12ns Access (≤ 83 Mhz clock rate)	 -7R5 -10 -12
Self Refresh (Special part)	P
Plastic Package 100-pin LQFP (0.65mm lead pitch)	

Key Timing Parameters

Speed Grade	Clock Frequency (MHz)	Access Time (ns)	Setup Time (ns)	Hold Time (ns)
-7R5	133	7	2.5	1.0
-10	100	9	3.0	1.0
-12	83	11	3.5	1.5

Description

The IBM 256K x 32 SGRAM is a high speed 8Mb CMOS DRAM with built-in graphics features. It is internally configured as a dual bank 128K x 32 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal CLK). Each bank is organized as a 512 rows x 256 columns x 32 bits.

Read/Write to the SGRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations. By having a Programmable Mode Register, and Load Special Mode Register the system can choose Read or Write burst lengths of 1, 2, 4, or 8 locations or the Full Page with burst termination option.

An Auto Precharge function may be enabled to provide a self-timed precharge that is initiated at the end of the burst sequence.

The SGRAM uses an internal pipelined architecture to achieve high speed operation, which also allows the column address to be changed on every clock cycle to achieve a high-speed fully random access. Precharging one bank while accessing the alternate bank will hide the precharge cycles, and provide seamless high speed random operation.

The SGRAM differs from the Synchronous DRAM (SDRAM) by providing an 8 column Block Write function and a Write-per-Bit (WPB) function. The Block Write and WPB functions may be combined with individual byte enables DQM_0-DQM_3.

The part is designed to operate at 3.3V only. An Auto Refresh mode is provided along with a power saving Power Down mode. All inputs and outputs are LVTTL compatible.

Applications

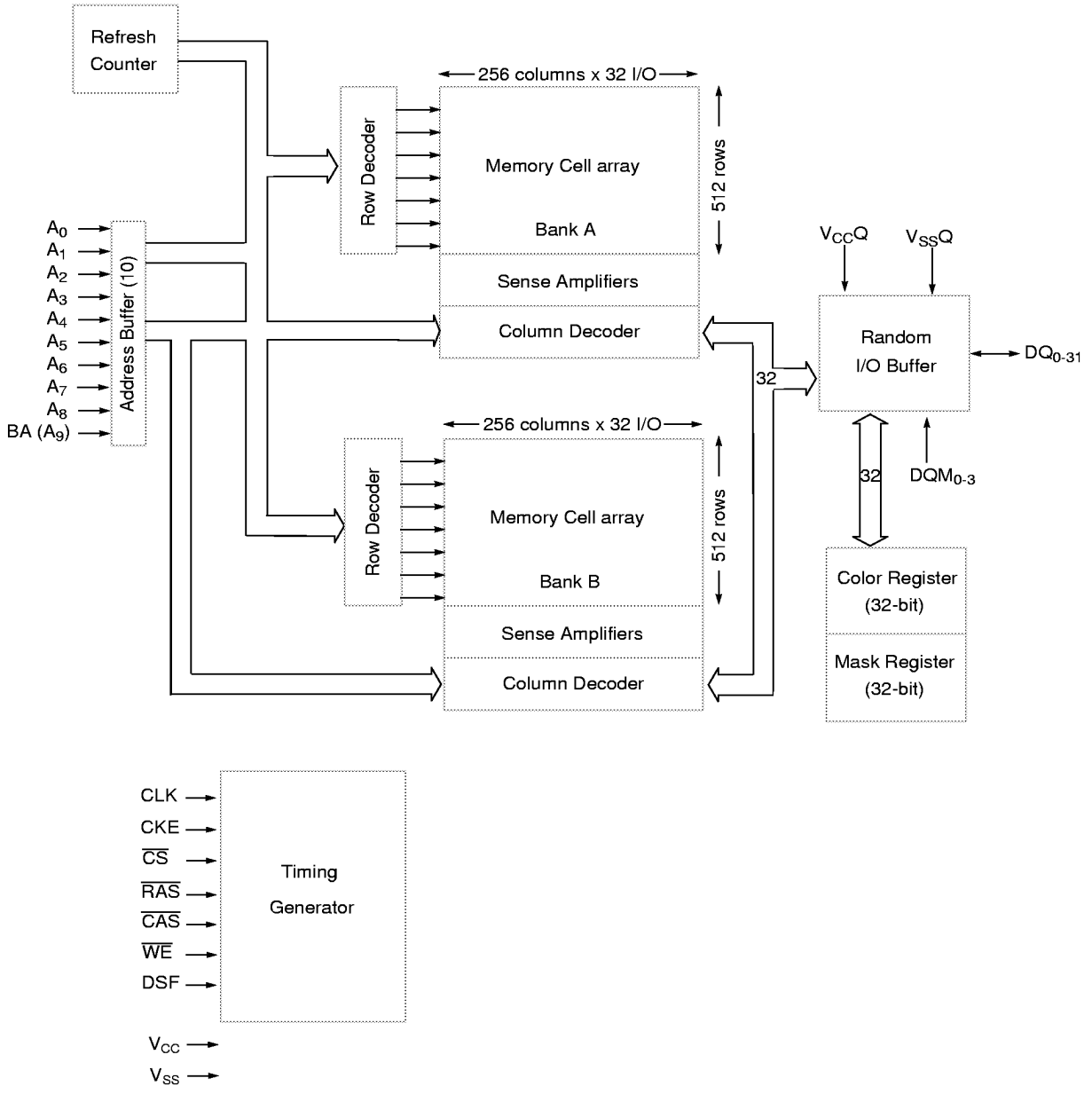
- Frame buffer for PC 2D/3D graphics applications
- One high speed device to displace two 256K x16 DRAMs at 2x performance
- High speed buffer for laser printers
- High speed buffer for RAID systems and disk drives
- Network and communication applications
- SET-TOP box application
- Games application
- Multimedia due to multiple bank architecture

Ordering Information

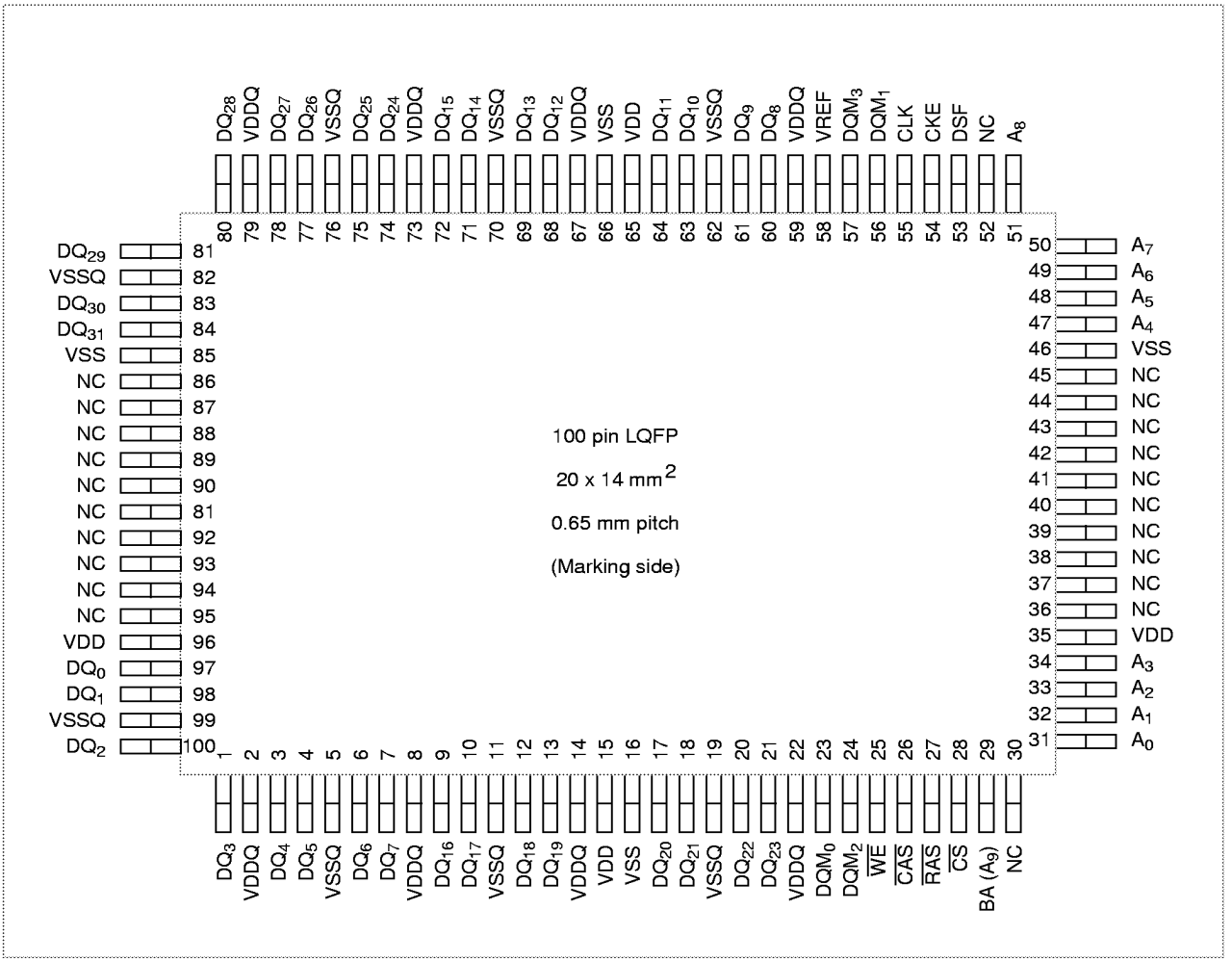
Part Number	Features	Speed	Voltage	Package	Notes
IBM038329NQ6A - 7R5	133 MHz, 4$\overline{BE}$, sync	8	3.3V	20X14 mm^2 100-pin LQFP (0.65min lead pitch)	1
IBM038329NQ6A - 10	100 MHz, 4$\overline{BE}$, sync	10			1
IBM038329NQ6A - 12	83 MHz, 4$\overline{BE}$, sync	12			1
IBM038329PQ6A - 7R5	133 MHz, 4$\overline{BE}$, sync	8			2
IBM038329PQ6A - 10	100 MHz, 4$\overline{BE}$, sync	10			2
IBM038329PQ6A - 12	83 MHz, 4$\overline{BE}$, sync	12			2

1. Low Power 8-Mb SGRAM parts.
2. Long Retention, extra low power 8-Mb SGRAM parts.

Block Diagram



Pin Configurations



Symbol	Function
A_0-BA (A_9)	Address Inputs
A_0-A_8	Row Address Inputs
A_0-A_8	Column Address Inputs
BA (A_9)	Bank Select
$\overline{CS}$	Chip Select
$\overline{CAS}$	Column Address Strobe
CKE	Clock Enable
CLK	System Clock Input
DQ_0-DQ_{31}	Data Inputs/Outputs
DQM_0-DQM_3	DQ Mask Enable

Symbol	Function
DSF	Special Function Enable
NC	No Connection
$\overline{RAS}$	Row Address Strobe
V_{DD}	Supply Voltage
V_{DDQ}	Supply Voltage for DQs
V_{REF}	Reference Input
V_{SS}	Ground
V_{SSQ}	Ground for DQs
$\overline{WE}$	Write Enable

Note: A_9 has been renamed BA to match JEDEC 8Mb nomenclature.

Signal Descriptions

Name	I/O	Function
A_0-A_8, BA (A_9)	I	Address bits A_0-A_8 are row addresses when Active command is activated. Address bits A_0-A_7 are column addresses when $\overline{CAS}$ is active. Address bit A_8, when $\overline{CAS}$ is active, enables/disables Auto Precharge. Address bit BA (A_9) selects which of the two memory banks is to be used.
$\overline{CAS}$	I	$\overline{CAS}$ is part of the input command to the SGRAM. See truth table for details.
CKE	I	Clock Enable disables the clock internally, thus allowing data to remain on the output for several CLK cycles. Clock Enable is also used as part of the input command to specify self-refresh.
CLK	I	CLK is driven by the system clock. All SGRAM input signals are sampled on the positive edge of CLK. The CLK also increments the internal burst counter and controls the output registers.
$\overline{CS}$	I	Chip Select indicates that the command on the input lines is for this device. If $\overline{CS}$ is high, the input command(s) will be ignored.
DQ_0-DQ_{31}	I/O	Data Input/Output lines transfer data between the memory array and the system bus. These are also input mask bits for Write-per-Bit. When Block Write is activated, DQs provide column address mask.
DQM_0-DQM_3	I	During Read, DQM=1 turns off the output buffers. During Write, DQM=1 prevents a write to the current memory location. DQM_0 corresponds to the lowest byte (DQ_0-DQ_7). DQM_1 corresponds to $DQ_{8\text{-}15}$. DQM_2 corresponds to $DQ_{16\text{-}23}$. DQM_3 corresponds to $DQ_{24\text{-}31}$.
$\overline{RAS}$	I	$\overline{RAS}$ is part of the input command to the SGRAM. See truth table for details.
V_{REF}	I	Reference voltage input for SSTL operation.
$\overline{WE}$	I	Write Enable is part of the input command. See truth table or details.

Operative Command Table (Part 1 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Add	Command	Action	Notes
Idle	H	X	X	X	X	X	INHBT	Nop or Power Down	5
	L	H	H	X	X	X	NOP or BST	Nop or Power Down	5
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	3
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	3
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	
	L	L	H	H	L	BA, RA	ACT	Row Active: No I/O Mask	
	L	L	H	H	H	BA, RA	ACTM	Row Active: I/O Mask	
	L	L	H	L	X	BA, PA	PRE/PREAL	Nop	
	L	L	L	H	X	X	REF/SREF	Refresh or Self Refresh	6
	L	L	L	L	L	Op-Code	LMR	Mode Register Access	
	L	L	L	L	H	Op-Code	LSMR	Special Mode Register Access	
Row Active	H	X	X	X	X	X	INHBT	Nop	
	L	H	H	X	X	X	NOP or BST	Nop	
	L	H	L	H	X	BA, CA, AP	RD/RDA	Begin Read: Determine AP	11
	L	H	L	L	L	BA, CA, AP	WR/WRA	Begin Write: Determine AP	11
	L	H	L	L	H	BA, CA, AP	BW/BWA	Block Write: Determine AP	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	
	L	L	H	L	X	BA, PA	PRE/PREAL	Precharge	8
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	Special Mode Register Access	

1. H:High level, L:Low level, X:High or low level (Don't care), V:Valid data input.
2. All entries assume that CKE was active (High level) during the preceding clock cycle.
3. Illegal to bank specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
5. If both are idle, and CKE is inactive (Low level), the device will enter Power Down Mode. All inputs buffers except CKE will be disabled.
6. If both banks are idle, and CKE is inactive (Low level), the device will enter Self Refresh Mode. All input buffer except CKE will be disabled.
7. Illegal if t_{RRD} is not satisfied.
8. Illegal if t_{RAS} is not satisfied.
9. Must satisfy burst interrupt condition.
10. Must mask preceding data which don't satisfy t_{DPL}.
11. Illegal if t_{RCD} is not satisfied.

RA = Row Address (A_0 - A_8) BA = Bank Address (BA) PA = Prechare All (A_8)
NOP = No Operation Command CA = Column Address (A_0 - A_7) AP = Auto Precharge (A_8)

Operative Command Table (Part 2 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Add	Command	Action	Notes
Read	H	X	X	X	X	X	INHBT	Continue Burst to End -> Row Active	
	L	H	H	X	X	X	NOP	Continue Burst to End -> Row Active	
	L	H	H	L	X	X	BST	Burst Stop -> Row Active	
	L	H	L	H	X	BA, CA, AP	RD/RDA	Term Burst, New Read: Determine AP	9
	L	H	L	L	L	BA, CA, AP	WR/WRA	Term Burst, Start Write: Determine AP	4, 9
	L	H	L	L	H	BA, CA, AP	BW/BWA	Term Burst, Start Block Write: Determine AP	4, 9
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	3
	L	L	H	L	X	BA, PA	PRE/PREAL	Term Burst, Precharging	
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	ILLEGAL	
Write	H	X	X	X	X	X	INHBT	Continue Burst to End -> Row Active	
	L	H	H	X	X	X	NOP	Continue Burst to End -> Row Active	
	L	H	H	L	X	X	BST	Burst Stop -> Row Active	
	L	H	L	H	X	BA, CA, AP	RD/RDA	Term Burst, New Read: Determine AP	9
	L	H	L	L	L	BA, CA, AP	WR/WRA	Term Burst, Start Write: Determine AP	4, 9
	L	H	L	L	H	BA, CA, AP	BW/BWA	Term Burst, Start Block Write: Determine AP	4, 9
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	3
	L	L	H	L	X	BA, PA	PRE/PREAL	Term Burst, Precharging	10
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	ILLEGAL	

1. H:High level, L:Low level, X:High or low level (Don't care), V:Valid data input.
2. All entries assume that CKE was active (High level) during the preceding clock cycle.
3. Illegal to bank specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
5. If both are idle, and CKE is inactive (Low level), the device will enter Power Down Mode. All inputs buffers except CKE will be disabled.
6. If both banks are idle, and CKE is inactive (Low level), the device will enter Self Refresh Mode. All input buffer except CKE will be disabled.
7. Illegal if t_{RRD} is not satisfied.
8. Illegal if t_{RAS} is not satisfied.
9. Must satisfy burst interrupt condition.
10. Must mask preceding data which don't satisfy t_{DPL}.
11. Illegal if t_{RCD} is not satisfied.

RA = Row Address (A_0 - A_8) BA = Bank Address (BA) PA = Prechare All (A_8)
NOP = No Operation Command CA = Column Address (A_0 - A_7) AP = Auto Precharge (A_8)

Operative Command Table (Part 3 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Add	Command	Action	Notes
Read with Auto Pre-charge	H	X	X	X	X	X	INHBT	Continue Burst to End -> Precharging	
	L	H	H	X	X	X	NOP	Continue Burst to End -> Precharging	
	L	H	H	L	X	X	BST	ILLEGAL	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	3
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	3
	L	L	L	H	X	X	REF/SREF	ILLEGAL	3
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	ILLEGAL	
Write with Auto Pre-charge	H	X	X	X	X	X	INHBT	Continue Burst to End -> Precharging	
	L	H	H	X	X	X	NOP	Continue Burst to End -> Precharging	
	L	H	H	L	X	X	BST	ILLEGAL	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	3
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	3
	L	L	L	H	X	X	REF/SREF	ILLEGAL	3
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	ILLEGAL	

1. H:High level, L:Low level, X:High or low level (Don't care), V:Valid data input.
2. All entries assume that CKE was active (High level) during the preceding clock cycle.
3. Illegal to bank specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
5. If both are idle, and CKE is inactive (Low level), the device will enter Power Down Mode. All inputs buffers except CKE will be disabled.
6. If both banks are idle, and CKE is inactive (Low level), the device will enter Self Refresh Mode. All input buffer except CKE will be disabled.
7. Illegal if t_{RRD} is not satisfied.
8. Illegal if t_{RAS} is not satisfied.
9. Must satisfy burst interrupt condition.
10. Must mask preceding data which don't satisfy t_{DPL}.
11. Illegal if t_{RCD} is not satisfied.

RA = Row Address (A_0 - A_8) BA = Bank Address (BA) PA = Prechare All (A_8)
NOP = No Operation Command CA = Column Address (A_0 - A_7) AP = Auto Precharge (A_8)

Operative Command Table (Part 4 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Add	Command	Action	Notes
Precharging	H	X	X	X	X	X	INHBT	Nop -> Enter Idle after t_{RP}	
	L	H	H	X	X	X	NOP	Nop -> Enter Idle after t_{RP}	
	L	H	H	L	X	X	BST	Nop -> Enter Idle after t_{RP}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	3
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	3
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	3
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	3
	L	L	H	L	X	BA, PA	PRE/PREAL	Nop -> Enter Idle after t_{RP}	
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	Load Special Mode Register	
Row Activating	H	X	X	X	X	X	INHBT	Nop -> Enter Row Active after t_{RCD}	
	L	H	H	X	X	X	NOP	Nop -> Enter Row Active after t_{RCD}	
	L	H	H	L	X	X	BST	Nop -> Enter Row Active after t_{RCD}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	3
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	3
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	3
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3, 7
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	3, 7
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	3
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	Load Special Mode Register	

1. H:High level, L:Low level, X:High or low level (Don't care), V:Valid data input.
2. All entries assume that CKE was active (High level) during the preceding clock cycle.
3. Illegal to bank specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
5. If both are idle, and CKE is inactive (Low level), the device will enter Power Down Mode. All inputs buffers except CKE will be disabled.
6. If both banks are idle, and CKE is inactive (Low level), the device will enter Self Refresh Mode. All input buffer except CKE will be disabled.
7. Illegal if t_{RRD} is not satisfied.
8. Illegal if t_{RAS} is not satisfied.
9. Must satisfy burst interrupt condition.
10. Must mask preceding data which don't satisfy t_{DPL}.
11. Illegal if t_{RCD} is not satisfied.

RA = Row Address (A_0 - A_8) BA = Bank Address (BA) PA = Prechare All (A_8)
NOP = No Operation Command CA = Column Address (A_0 - A_7) AP = Auto Precharge (A_8)

Operative Command Table (Part 5 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Add	Command	Action	Notes
Write Recovering	H	X	X	X	X	X	INHBT	Nop -> Enter Row Active after t_{WR}	
	L	H	H	X	X	X	NOP	Nop -> Enter Row Active after t_{WR}	
	L	H	H	L	X	X	BST	Nop -> Enter Row Active after t_{WR}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	Start Read, Determine AP	4
	L	H	L	L	L	BA, CA, AP	WR/WRA	New Write, Determine AP	
	L	H	L	L	H	BA, CA, AP	BW/BWA	New Block Write, Determine AP	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	3
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	3
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	Load Special Mask Register	
Write Recovering with Auto Precharge	H	X	X	X	X	X	INHBT	Nop -> Enter Precharge after t_{WR}	
	L	H	H	X	X	X	NOP	Nop -> Enter Precharge after t_{WR}	
	L	H	H	L	X	X	BST	Nop -> Enter Precharge after t_{WR}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	3, 4
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	3
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	3
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	3
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	3
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	3
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	ILLEGAL	

1. H:High level, L:Low level, X:High or low level (Don't care), V:Valid data input.
2. All entries assume that CKE was active (High level) during the preceding clock cycle.
3. Illegal to bank specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
5. If both are idle, and CKE is inactive (Low level), the device will enter Power Down Mode. All inputs buffers except CKE will be disabled.
6. If both banks are idle, and CKE is inactive (Low level), the device will enter Self Refresh Mode. All input buffer except CKE will be disabled.
7. Illegal if t_{RRD} is not satisfied.
8. Illegal if t_{RAS} is not satisfied.
9. Must satisfy burst interrupt condition.
10. Must mask preceding data which don't satisfy t_{DPL}.
11. Illegal if t_{RCD} is not satisfied.

RA = Row Address (A_0 - A_8) BA = Bank Address (BA) PA = Prechare All (A_8)
NOP = No Operation Command CA = Column Address (A_0 - A_7) AP = Auto Precharge (A_8)

Operative Command Table (Part 6 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Add	Command	Action	Notes
Refreshing	H	X	X	X	X	X	INHBT	Nop -> Enter Idle after t_{RC}	
	L	H	H	X	X	X	NOP	Nop -> Enter Idle after t_{RC}	
	L	H	H	L	X	X	BST	Nop -> Enter Idle after t_{RC}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	OP-CODE	LSMR	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	INHBT	Nop -> Enter Idle after 2Clocks	
	L	H	H	X	X	X	NOP	Nop -> Enter Idle after 2Clocks	
	L	H	H	L	X	X	BST	Nop -> Enter Idle after 2Clocks	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	ILLEGAL	

1. H:High level, L:Low level, X:High or low level (Don't care), V:Valid data input.
2. All entries assume that CKE was active (High level) during the preceding clock cycle.
3. Illegal to bank specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
5. If both are idle, and CKE is inactive (Low level), the device will enter Power Down Mode. All inputs buffers except CKE will be disabled.
6. If both banks are idle, and CKE is inactive (Low level), the device will enter Self Refresh Mode. All input buffer except CKE will be disabled.
7. Illegal if t_{RRD} is not satisfied.
8. Illegal if t_{RAS} is not satisfied.
9. Must satisfy burst interrupt condition.
10. Must mask preceding data which don't satisfy t_{DPL}.
11. Illegal if t_{RCD} is not satisfied.

RA = Row Address (A_0 - A_8) BA = Bank Address (BA) PA = Prechare All (A_8)
NOP = No Operation Command CA = Column Address (A_0 - A_7) AP = Auto Precharge (A_8)

Function Truth Table

Operation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	BA (A_9)	A_8	A_7-A_0	MNE
	n-1	n										
Device Deselect	H	X	H	X	X	X	X	X	X	X	X	INHBT
No Operation	H	X	L	H	H	H	X	X	X	X	X	NOP
Load Mode Register	H	X	L	L	L	L	L	X	OP CODE			LMR
Load Special Mode Register	H	X	L	L	L	L	H	X	OP CODE			LSMR
Row Activate	H	X	L	L	H	H	L	X	BS	Row Addr		ACT
Row Activate w/WPB	H	X	L	L	H	H	H	X	BS	Row Addr		ACTM
Read	H	X	L	H	L	H	X	X	BS	L	Col.	RD
Read w/ Auto Percharge	H	X	L	H	L	H	X	X	BS	H	Col.	RDA
Write Command	H	X	L	H	L	L	L	X	BS	L	Col.	WR
Write w/ Auto Precharge	H	X	L	H	L	L	L	X	BS	H	Col.	WRA
Block Write	H	X	L	H	L	L	H	X	BS	L	Col.	BW
Block Write w/ Auto Precharge	H	X	L	H	L	L	H	X	BS	H	Col.	BWA
Burst Termination	H	X	L	H	H	L	X	X	X	X	X	BST
Precharge Single Bank	H	X	L	L	H	L	X	X	BS	L	X	PRE
Precharge All Banks	H	X	L	L	H	L	X	X	X	H	X	PREAL
Auto Refresh	H	H	L	L	L	H	X	X	X	X	X	REF
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	X	SREF(EN)
Self Refresh Exit	L L	H H	H L	X H	X H	X H	X X	X X	X X	X X	X X	SREF(EX)
Power Down Mode (entry)	H	L	H	X	X	X	X	X	X	X	X	PDN-(EN)
Power Down Mode (entry)	H	L	L	H	H	H	X	X	X	X	X	PDN-(EN)
Power Down Mode (exit)	L	H	X	X	X	X	X	X	X	X	X	PDN-(EX)

1. All inputs are latched on the rising edge of the CLK.
2. LMR, LSMR, REF, and SREF commands should be issued only after both banks are deactivated (PREAL command).
3. ACT and ACTM command should be issued only after the corresponding bank has been deactivated (PRE command).
4. WR, WRA, RD, RDA should be issued after the corresponding bank has been activated (ACT command).
5. Auto Precharge command is not valid for full-page burst.
6. BW and BWA commands use mask register data only after ACTM command. DQM byte masking is active regardless of WPB mask.
7. Loading Mask Register: Initiate an LSMR cycle with address pin A_5=1 to load the Mask register with the Mask data present on DQ pins. Except A_5, all other address pins must be “0” during LSMR cycle while loading the Mask Register.
8. Loading Color Register: Initiate an LSMR cycle with address pin A_6=1 to load the Color register with the Color input data on DQ pins. Except A_6, all other address pins must be “0” during LSMR cycle while loading the Color register 0.
9. Any Write or Block Write cycles to the selected bank/row while active will be masked according to the contents of the mask register, in addition to the DQM signals and the column/byte mask information (the later for Block Writes only).
10. Block Writes are not burst oriented and always apply to the eight column locations selected by A_7-A_3.

Functional Description

IBM's 8Mb SGRAM is a dual bank 128K x 32 SDRAM with graphics features of Block Write and Masked Write. It consists of two banks. Each bank is organized as 512 rows x 256 columns x 32 bits.

Read and Write accesses are burst oriented. Accesses begin with the registration of an Active command which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and the row to be accessed. Address bit BA (A_9) selects the bank and address bits A_8-A_0 select the row. Address bits A_7-A_0 registered coincident with the Read and Write command are used to select the starting column location for the burst access.

Block Writes are not burst oriented and always apply to eight column locations selected by A_7-A_3. DQs registered at Write command are used to mask the selected columns. DQs registered coincident with the Active command are used as Write-per-Bit mask. DQs registered coincident with the Load Special Mode Register command are used as Color data (LC bit =1) or Persistent Mask (LM = 1). If LC and LM are both 1 in the same Load Special Mode Register command cycle, the data of the Mask and the Color Register will be unknown.

Initialization

SGRAMs must be initialized in a predefined manner to prevent undefined operation. Once power is applied, the SGRAM requires a 100µs delay prior to activating CKE. All inputs should be held high during this phase of power up. After a delay of 100µs or more, the CKE pin must be driven high before a positive clock (CLK) edge. The first command will be registered on the clock edge following t_{CKS}.

Both banks must then be pre-charged by issuing PREAL command, thereby placing the device in the “all banks idle” state. Once in the idle state, at least two Auto Refresh cycles must be performed. Once the Auto Refresh cycles are complete, the SGRAM is ready for Mode Register programming. Because the Mode Register will power up in an unknown state, it should be programmed prior to performing any operational command.

Register Definition

The following pages describe the Mode Register and Special Mode Register functions.

Mode Register

The Mode Register is used to define: a Burst Length, a Burst type, a Read Latency and an operating mode as shown in the diagram on page 16. The mode register is programmed via the Load Mode Register command and will retain the stored information until it is programmed again or the device loses power.The mode register must be loaded when both banks are idle and the controller must wait the specified time before initiating the subsequent command. Violating either of these requirements may result in unknown operation.

Burst Length

Read and Write operations to the SGRAM are burst oriented, with the burst length being programmable, as shown in the diagram on page 16. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types and a Full Page Burst is available for the sequential type. The Full Page Burst is used in conjunction with the Burst Terminate command to generate arbitrary burst lengths.

When a Read or Write command is issued, a block of columns equal to the burst length is selected. The block is defined by address bits A_7-A_1 when the burst length is set to 2, by A_7-A_2 for burst length is set to 4 and by A_7-A_3 when the burst length is set to 8. The lower order bit(s) are used to select the starting location within the block. The burst will wrap within the block if a boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved and the type is selected based on the setting of BT bit in the mode register. If BT is set to “0”, the burst type is sequential, if BT is “1”, the burst type is interleave.

Read Latency

The Read Latency is the delay in clock cycles between the registration of a Read command and the availability of the first piece of output data. The latency can be set to 1, 2 or 3 clocks. If a Read command is registered at clock edge n and the Read Latency is 2 clocks, the data will be available by clock edge n+2. The DQs will start driving as a result of the clock edge one cycle earlier (n+1) and provided the relevant access times are met, the data will be valid by clock edge n+2.

Operation Mode

In normal operation, the M_7-M_9 bits of Mode Register (MR) are set "0". The programmed burst length applies to both read and write bursts. If Bit M_7 is set equal to "1", two Color Registers are specified. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Load Special Mode Register (LSMR)

The Special Mode Register command is used to load the mask and color registers, which are used in Block Write and Masked Write cycles.The data to be written to either the color registers or the Mask Register is applied to the DQs and the control information is applied to the address inputs. During a LSMR cycle, if the address bit A_6 is "1", and all other address inputs are "0", the Color Register 0 will be loaded with the data on the DQs. If the address bits A_6 and A_7 are both set equal to "1" and Mode Register M_7 bit was already set equal to "1", Color Register 1 will be loaded with the data on the DQs.This color data is used for Block Write cycles. Similarly, when input A_5 is "1", and all other address inputs are "0" during a LSMR cycle, the mask register will be loaded with the data on the DQs.

Caution:
Never Set bit A_5 to "1" when A_6 and/or A_7 are set equal to "1" in the same Load Special Mode Register cycle to avoid unknown operation. (See "Special Mode Register Functions" on page 18.)

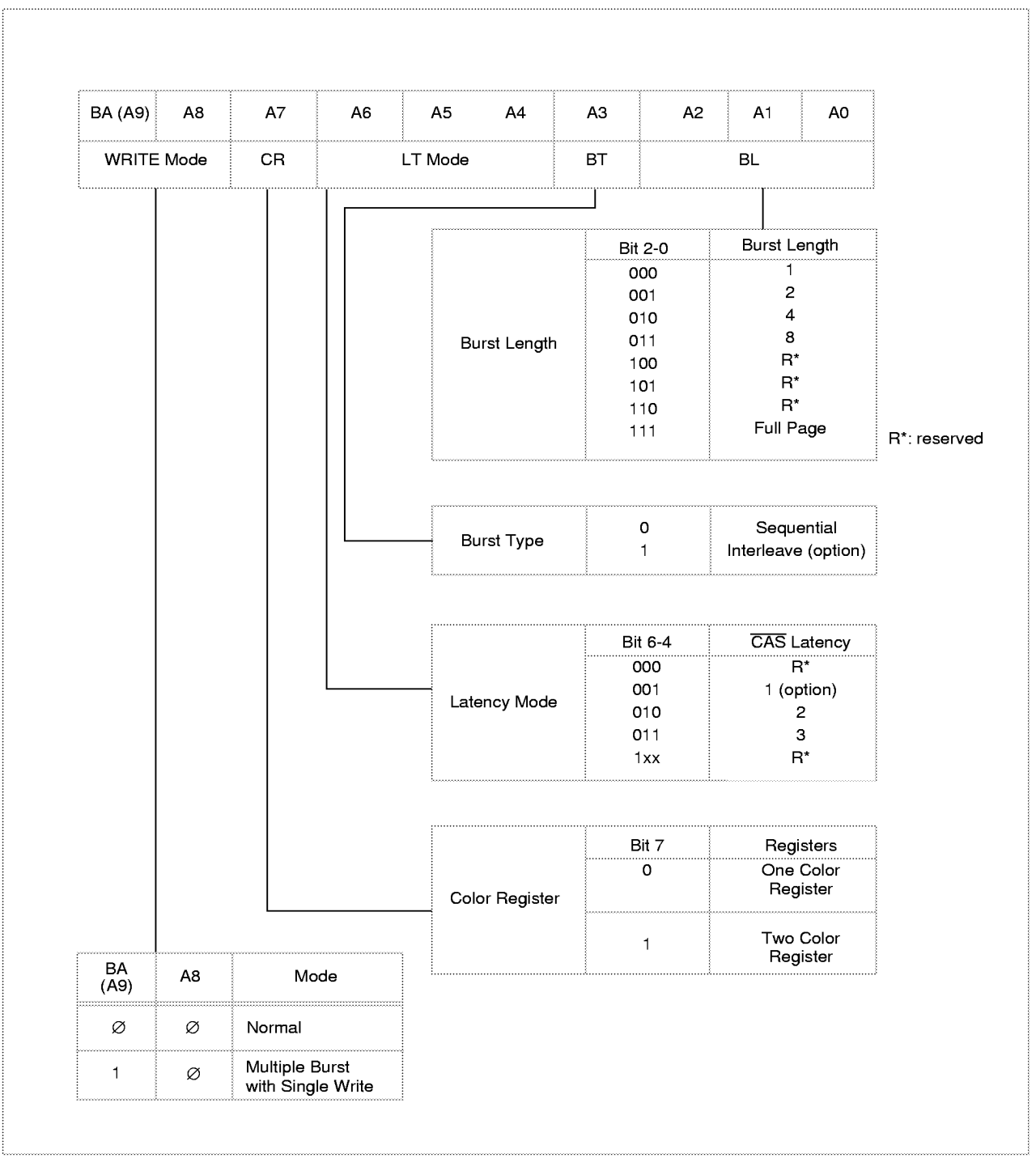
Color Registers

Two Color Registers (Color Register 0 and Color Register 1) are available in the devices as shown in the diagram on page 32. Each color register is a 32-bit register which supplies the data during Block Write cycles. The Color Register is loaded via a Load Special Mode Register command, as shown in the diagram on page 32 and will retain data until loaded again with a new data or until power is removed from the SGRAM.

Mask Register

The Mask Register (or the Write-per-Bit mask register) is a 32-bit register which acts as a per-bit mask during Masked Write and Masked Block Write cycles. The Mask Register is loaded via the Load Special Mode Register command and will retain data until loaded again or until power is removed from the SGRAM.

Mode Register Functions



Burst Length and Sequence

Burst of two

Starting Address (Column Address A_0)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0,1	0,1
1	1,0	1,0

Burst of four

Starting Address (Column Address A_1- A_0)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0 (00B)	0,1,2,3	0,1,2,3
1 (01B)	1,2,3,0	1,0,3,2
2 (10B)	2,3,0,1	2,3,0,1
3 (11B)	3,0,1,2	3,2,1,0

Burst of eight

Starting Address (Column Address A_1- A_0)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0 (000B)	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
1 (001B)	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
2 (010B)	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
3 (011B)	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
4 (100B)	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
5 (101B)	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
6 (110B)	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
7 (111B)	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0

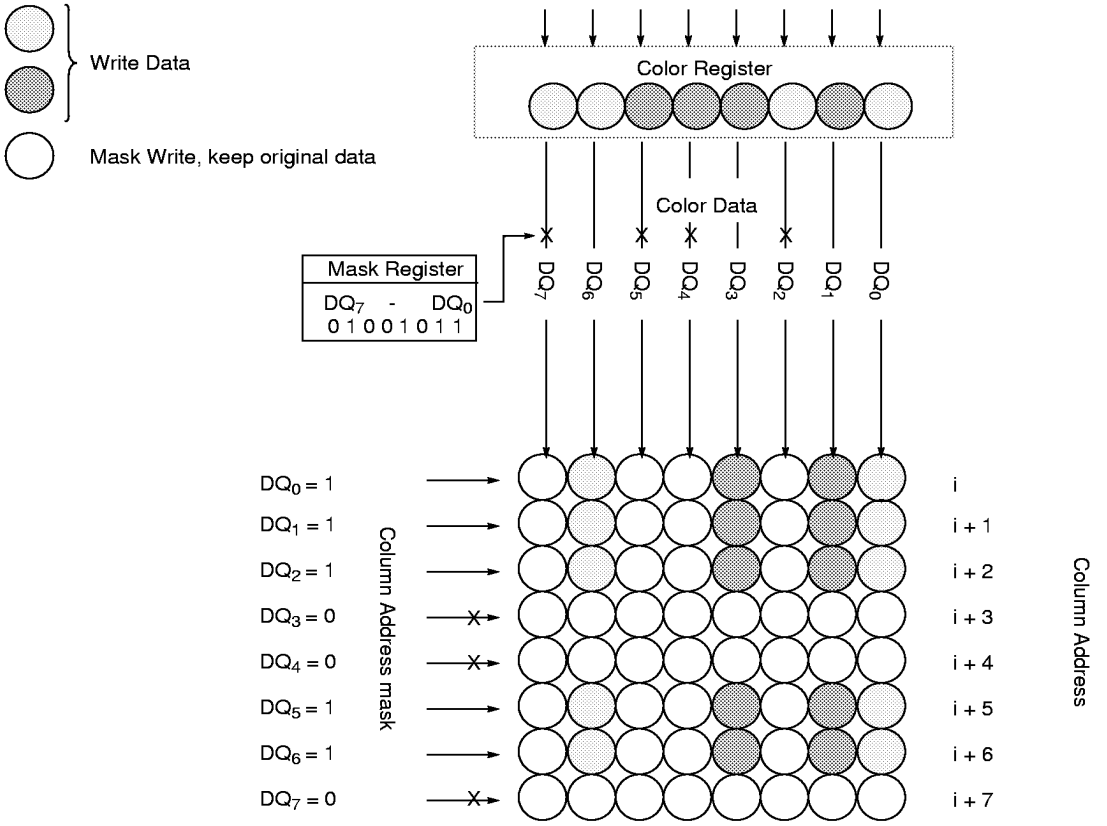
Full Page Burst

Full Page Burst is an extension of the above tables of Sequential Addressing with the burst length being 256.

Special Mode Register Functions

Address Bits										Functions
BA (A_9)	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
0	0	0	0	0	0	0	0	0	0	Do not load
0	0	0	0	1	0	0	0	0	0	Enable Mask
0	0	0	1	0	0	0	0	0	0	Load Color Register 0
0	0	1	1	0	0	0	0	0	0	Load Color Register 1

Block Write Illustration



Column Mask

DQ_{0-7}:	Column Mask for DQ_{0-7}
DQ_{8-15}:	Column Mask for DQ_{8-15}
DQ_{16-23}:	Column Mask for DQ_{16-23}
DQ_{24-31}:	Column Mask for DQ_{24-31}

Write-per-Bit

Mask Data = Mask Register + DQM_i

Commands

The Function Truth Table on page 12 provides a quick reference of available commands.

Device Deselect (INHBT)

The device deselect or inhibit function prevents commands from being executed by the SGRAM, regardless of whether the CLK signal is enabled. The device is effectively deactivated ($\overline{CS}$ is high).

No Operation (NOP)

The NOP command is used to perform a no operation to an SGRAM which is selected ($\overline{CS}$ is low). This prevents unwanted commands being registered during idle or wait states. The execution of the command(s) already in progress will not be affected

Load Mode Register (LMR)

The Mode Register is loaded via address input pins BA (A_9)-A_0. ***The LMR command can only be issued when both banks are idle, and a subsequent executable command can not be issued until t_{MTC} (1 CLK cycle Latency) is met.***

Load Special Mode Register (LSMR)

LSMR command is used to load either the Color Register or the Mask Register at a time. The control information is provided on inputs BA (A_9)-A_0, while the data for the Color or Mask Register is provided on the DQs. The LSMR command can be issued when both banks are idle, or one or both are active but with no Read, Write or Block Write accesses in progress. ***A subsequent command can not be issued until t_{SML} (2 clocks latency) is met.***

Active (ACT)

The ACT command is used to open (or activate) a row in a particular bank. The value on BA (A_9) selects the bank and the address provided on input pins A_8-A_0 selects the row. This row remains open for accesses until a Precharge command is issued to the bank. ***A Precharge command must be issued before opening a different row in the same bank.***

Active with WPB (ACTM)

ACTM command is similar to the ACT command, except that the Write-per-Bit mask is activated. Any Write or Block Write cycles to the selected bank/row while active will be masked according to the contents of the Mask Register.

Read (RD)

The Read command is used to initiate a burst read access to an active row. The value on BA (A_9) selects the bank and the address provided on inputs A_7-A_0 selects the starting column location. The value on A_8 determines whether or not Auto Precharge is used. If A_8 is “1”, Auto Precharge is used. If Auto Precharge is selected, the row being accessed will be precharged at the end of the read burst; if Auto Precharge is not selected, the row will remain open for subsequent accesses. ***If a particular DQM was registered high, the corresponding DQs appearing 2 clocks later on the output pins will be High-Z.***

Write (WR)

The Write command is used to initiate a burst write access to an active row. The value on BA (A_9) selects the bank and the address provided on inputs A_7-A_0 selects the starting column location. The value on A_8 determines whether or not Auto Precharge is used. If A_8 is "1", Auto Precharge is used. If Auto Precharge is selected, the row being accessed will be precharged at the end of write burst; if Auto Precharge is not selected, the row will remain open for subsequent accesses. ***If a particular DQM is registered high, the corresponding data inputs will be ignored and the write will not be executed to that byte location.***

Block Write (BW)

The Block Write command is used to write a single data value to the block of eight consecutive column locations addressed by inputs A_7-A_3. The data is provided by the Color Register which must be loaded prior to the Block Write cycle by invoking LSMR cycle. The input data on DQs which is registered coincident with the Block Write command is used to mask specific column/byte combinations within the block. ***The DQM signals operate the same way as for Write cycles, but are applied to all eight columns in the selected block.***

Precharge (PRE)

The Precharge command is used to deactivate the open row in a particular bank or the open row in both banks. The bank(s) will be available for row access some specified time (t_{RP}) after the Precharge command is issued. Input A_8 determines whether one or both banks are to be precharged, input BA (A_9) selects the bank. If A_8 is "1", both banks are to be precharged and BA (A_9) is "don't care." Once a bank is precharged (or deactivated), it is in the idle state and must be activated prior to any Read, Write, or Block Write commands being issued to that bank.

Auto Precharge (PREA)

The Auto Precharge feature allows the user to issue a Read, Write, or Block Write command that automatically performs a precharge upon the completion of the Block Write access or Read or Write burst, ***except in the Full Page Burst mode, where it has no effect.***

The use of this feature eliminates the need to "manually" issue a Precharge command during the functional operation of the SGRAM.

Burst Terminate (BST)

The Burst Terminate command is used to truncate either fixed-length or Full Page Bursts.

Auto Refresh (REF)

Auto Refresh is used to refresh the various rows in the SGRAM and is analogous to $\overline{CAS}$-before-$\overline{RAS}$ (CBR) in DRAMs. This command must be issued each time a refresh is required. The addressing is generated by the internal refresh counter, therefore, the address bits are "don't care" during a CBR cycle. The SGRAM requires that 1024 rows to be refreshed every 16ms (t_{REF}). This refresh can be accomplished either by providing a Auto Refresh command every 16.6µs or all 1024 Auto Refresh commands can be issued in a burst at the minimum cycle rate (t_{RC} =100ns) once every 16ms.

Self Refresh (SREF)

The Self Refresh command can be used to retain data in the SGRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the SGRAM retains data without external clocking. Once the SREF command is registered, all the inputs to the SGRAM become “don't care” with the exception of CKE, which must remain low. Once SREF mode is engaged, the SGRAM provides its own internal clocking, causing it to perform its own Auto Refresh cycles. The SGRAM may remain in Self Refresh mode for an indefinite period. The procedure for exiting requires a sequence of commands. First, the system clock must be stable prior to CKE going high. ***Once CKE is high, the SGRAM must have NOP commands issued for t_{XSR} (100ns), because of the time required for the completion of any bank currently being internally refreshed.***

Stub Series Terminated Logic (SSTL)

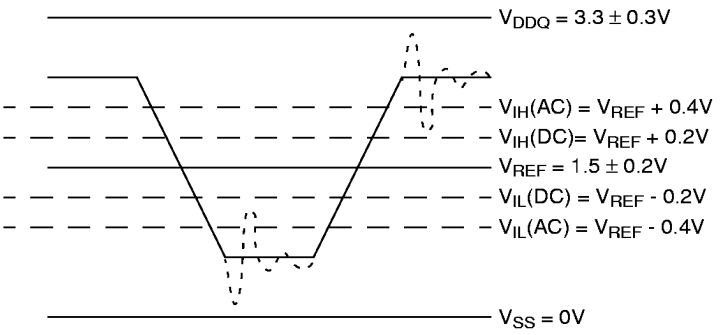
DC Input Levels

SSTL DC input levels reduce the effects of ringing and define the final logic state unambiguously. Once a receiver input has crossed a DC level, it will change and maintain the new state.

AC Input Levels

SSTL AC input levels must be met for the receiver to meet the timing specifications.

SSTL Input Levels (V_{DDQ}=3.3V)



SSTL Supply Voltage Levels

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	Device Supply Voltage	V_{DDQ}	No Requirement		V	
V_{DDQ}	Output Supply Voltage	3.0	3.3	3.6	V	1
V_{REF}	Input Reference Voltage	1.3	1.5	1.7	V	2
V_{TT}	Termination Voltage	V_{REF}-0.05	V_{REF}	V_{REF}+0.05	V	3

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. Peak to peak AC noise on V_{REF} may not exceed 2% V_{REF} (DC). V_{REF} is also expected to track noise variations in V_{DDQ}.
3. V_{TT} of the transmitting device must track V_{REF} of the receiving device.

SSTL Input AC/DC Logic Levels

Symbol	Parameter	Min	Max	Units	Notes
V_{IH} (DC)	DC Input Logic High	V_{REF}+0.20	V_{DDQ}+0.3	V	1
V_{IH} (AC)	AC Input Logic High	V_{REF}+0.40	—	V	
V_{IL} (DC)	DC Input Logic Low	-0.30	V_{REF}-0.20	V	
V_{IL} (AC)	AC Input Logic Low	—	V_{REF}-0.40	V	

1. The relationship of the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of V_{IH} (max) (input overdrive) it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_3 inputs but has no SSTL_3 outputs (e.g., a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.9V (High corner V_{DDQ}+300mV).

SSTL AC Test Conditions

Symbol	Parameter	Value	Units	Notes
V_{REF}	Input Reference Voltage	0.45*V_{DDQ}	V	1
V_{SWING} (max)	Input Signal Maximum Peak to Peak Swing	2.0	V	1, 2
SLEW	Input Signal Minimum Slew Rate	1.0	V/ns	3

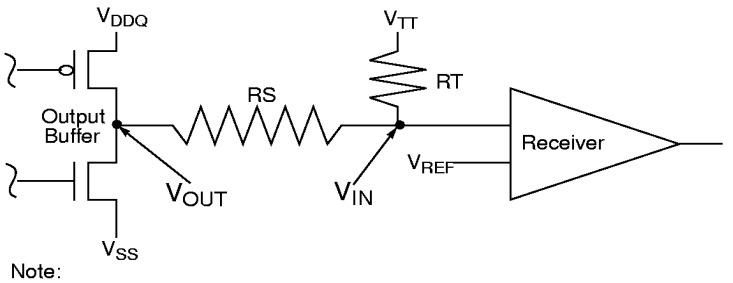
1. Input waveform timing is referenced to the input signal crossing the V_{REF} level applied to the device.
2. Compliant devices must still meet the V_{IH} (AC) and V_{IL} (AC) specifications under actual use conditions.
3. The 1V/ns input signal minimum slew rate is to be maintained in the V_{IL} max (AC) to V_{IL} min (AC) range of the input signal swing.

SSTL Output Buffers

The input voltage provided to the receiver depends on three parameters:

- V_{DDQ} and current drive capabilities of the output buffer
- Termination voltage
- Termination resistance

Typical SSTL Output Buffer (Driver)



Note:
V_{IN} must be at least 400mV above or below V_{REF} as a result of V_{OUT} attaining its maximum low or its min-mum high value.

There are two classes of output drivers:

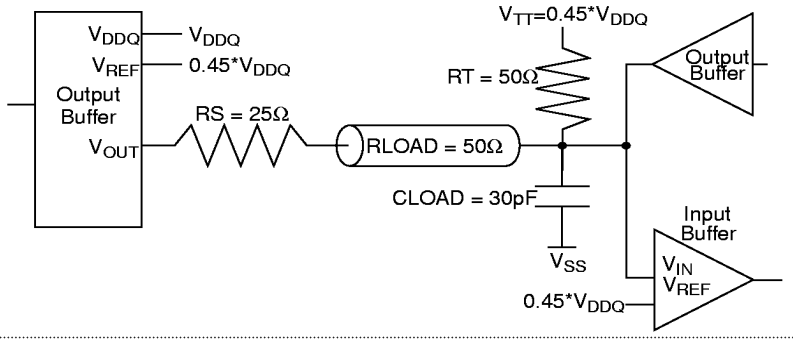
- Class I: RS = 25Ω, RT = 50Ω, I_{RT} = 8mA (for V_{IN} = $V_{REF} \pm 0.4V$)
- Class II: RS = 25Ω, RT = 25Ω, I_{RT} = 16mA (for V_{IN} = $V_{REF} \pm 0.4V$)

SSTL Output Buffer Characteristics

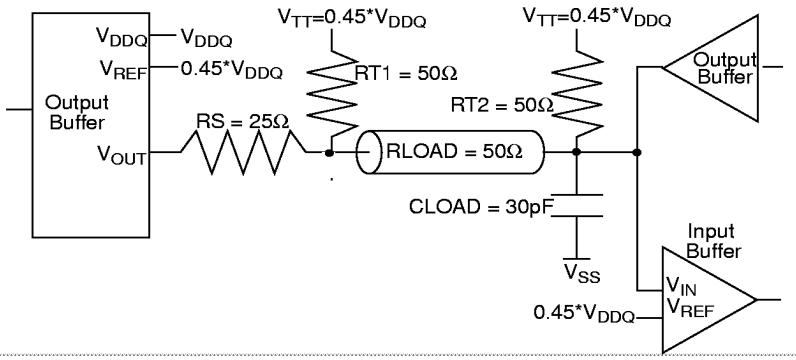
Symbol	Parameter	Class I	Class II	Units	Notes
V_{OH}	Minimum Required Output Pull-up under AC Test Load	V_{TT} + 0.6	V_{TT} + 0.8	V	
V_{OL}	Maximum Required Output Pull-down under AC Test Load	V_{TT} – 0.6	V_{TT} – 0.8	V	
V_{OTR}	Input Signal Minimum Slew Rate	0.45*V_{DDQ}	0.45*V_{DDQ}	V	1
I_{OH}	Output Minimum Source DC Current	8	16	mA	3, 4
I_{OL}	Output Minimum Sink DC Current	8	16	mA	4, 5
RT	Termination Resistor	50	25	Ω	
RS	Series Resistor	25	25	Ω	

1. Since V_{IN} must be at least 0.4V above or below V_{REF} as a result of V_{OUT}, using a series resistor of 50Ω for a Class I output driver this translates into the minimum requirement of a 0.6V swing relative to V_{TT}, and for a Class II driver with a series resistor of 25Ω, this results in a minimum requirement of a 0.8V swing relative to V_{TT}.
2. The V_{DDQ} of the device under test is referenced.
3. V_{DDQ} = 3.0V; V_{OUT} = V_{DDQ} – 1.1V.
4. The DC value of V_{REF} applied to the receiving device is expected to be set to V_{TT}.
5. V_{DDQ} = 3.0V; V_{OUT} = 0.7V.

SSTL Push-Pull Output Buffer Designed for symmetrically single parallel terminated loads with series resistor (Class I) for signals and address lines.



SSTL Push-Pull Output Buffer Designed for symmetrically double parallel terminated loads with series resistor (Class II) for DQs**.**



Absolute Maximum Ratings

Parameter	Min	Max	Notes
Voltage on V_{CC}/V_{CCQ} supply relative to V_{SS}	-1V	4.6V	1
Voltage on input/output pins	-1V	4.6V	1
Operating Temperature, T_A (ambient)	0°C	70°C	1
Storage Temperature	-55°C	150°C	1
Power Dissipation		1W	1
Short Circuit Output Current		50mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Operating Specifications and Conditions ($0°C \geq T_A \leq 70°C$; $V_{CC}/V_{CCQ} = 3.3V \pm 0.3V$)

Symbol	Parameter	Min	Type	Max	Unit
V_{CC}/V_{CCQ}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High (Logic 1) Voltage, all inputs	2.0	-	V_{CC} + 0.3	V
V_{IL}	Input Low (Logic 0) Voltage, all inputs	-.5	-	0.8	V
V_{OH}	Output High (I_{OUT} = -2mA)	2.4	-	-	V
V_{OL}	Output Low (I_{OUT} = 2mA)	-	-	0.4	V
I_L	Input Leakage Current Any Input 0V < V_{IN} < 3.6V (All other pins not under test = 0V)	-3	-	3	µA
I_{OZ}	Output Leakage Current (DQs are disabled; 0V < V_{OUT} < 0.4V)	-3	-	3	µA

Capacitance

Symbol	Parameter	Max	Unit	Notes
Ci_1	Input Capacitance: A_0 - BA (A_9)	5	pF	1
Ci_2	Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM, CLK, CKE, $\overline{CS}$, DSF	5	pF	1
Ci_0	Input/Output Capacitance: DQs	5	pF	1

1. This parameter is sampled. V_{CC}/V_{CCQ} = 3.3V±0.3V; f = 1MHz.

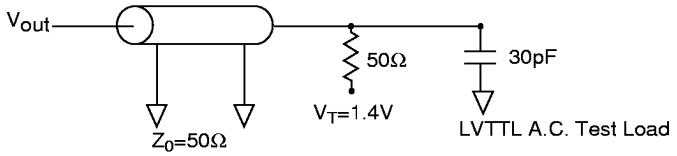
I_{CC} Specifications ($0°C \le T_A \le 70°C$; V_{CC}/V_{CCQ} = 3.3V 0.3V)

Symbol	Parameter	Test Condition	$\overline{CAS}$ Latency	Maximum			Unit	Notes
				-7R5	-10	-12		
I_{CC1}	Operating Current	Burst Length = 1 $t_{RC} \ge t_{RC}$(Min) $t_{CK} \ge t_{CK}$(Min) I_O = 0mA	3	275	185	180	mA	1
			2	250	175	170		
$I_{CC2}P$	Precharge Standby Current in Power Down Mode	CKE ≤ VIL(Max) t_{CK} =15ns		3	3	3	mA	
$I_{CC2}PS$		CKE ≤ VIL(Max) t_{CK} = Infinity		3	3	3		
$I_{CC2}N$	Precharge Standby Current in Non Power Down Mode	CKE ≥ VIH(Min) t_{CK} =15ns Input change every 30ns		45	45	45	mA	
$I_{CC2}NS$		CKE ≥ VIH(Min) t_{CK} =Infinity No input change		20	20	20		
$I_{CC3}P$	Active Standby Current in Power Down Mode	CKE ≤ VIL(Max) t_{CK} =15ns		3	3	3	mA	
$I_{CC3}PS$		CKE ≤ VIL(Max) t_{CK} = Infinity		3	3	3		
$I_{CC3}N$	Active Standby Current in Non Power Down Mode	CKE ≥ VIH(Min) t_{CK} =15ns Input change every 30ns		50	50	50	mA	
$I_{CC3}NS$		CKE ≥ VIH(Min) t_{CK} =Infinity No input change		25	25	25		
I_{CC4}	Operating Current (Burst Mode)	t_{RC} =Infinity I_O = 0mA Dual Bank Interleave Continuous	3	200	190	180	mA	1, 2
			2	150	140	130		
I_{CC5}	Auto Refresh Current	$t_{RC} \ge t_{RC}$(Min)	3	275	185	180	mA	3
			2	250	155	150		
I_{CC6}	Self Refresh Current	CKE = 0.2V		3	3	3	mA	

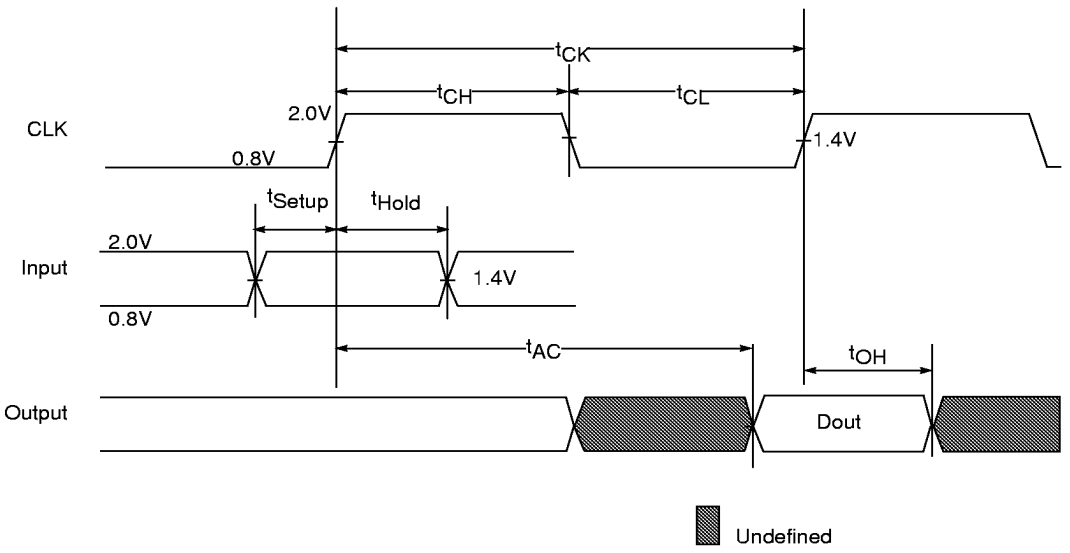
1. Measured with outputs open, inputs 0-3V.
2. Assumes minimum column address update cycle.
3. Refresh period is 16ms.

Timing Specifications and Conditions ($0°C \le t_A \le 70°C$; $V_{CC}/V_{CCQ} = 3.3V \pm 0.3V$)

1. All voltages are referenced to V_{SS} (GND).
2. Icc depends on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
3. Enables on-chip refresh and address counters.
4. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$).
5. An initial pause of 100ms is required after power up, followed by two Auto Refresh commands to ensure proper device operation.
6. The timing specifications assume a transition time (t_T = 1ns).
7. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with timing reference to 1.4V crossover point.



I/O Timing Diagrams



Timing Specifications

Symbol	qParameter	$\overline{CAS}$ Latency	-7R5		-10		-12		Units
			Min	Max	Min	Max	Min	Max	
t_{AC3} for 50 pF load	Access time from CLK (positive edge)	3	-	7	-	9	-	11	ns
t_{AC2} for 50 pF load		2	-	10	-	12	-	15	ns
t_{AH}	Address hold time		1.5	-	1.5	-	1.5	-	ns
t_{AS}	Address setup time		2.5	-	2.5	-	3.5	-	ns
t_{BPL}	Block Write to Precharge delay		7.5	-	10	-	12	-	ns
t_{BWC}	Block Write cycle time		7.5	-	10	-	12	-	ns
t_{CH}	$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, DQM hold time		1.0	-	1.0	-	1.0	-	ns
t_{CHI}	CLK high level width		3	-	3.5	-	4	-	ns
t_{CK3}	System clock cycle time	3	7.5	-	10	-	12	-	ns
t_{CK2}		2	12	-	15	-	18	-	ns
t_{CKH}	CKE hold time		1.0	-	1.0	-	1.0	-	ns
t_{CKS}	CKE setup time		2.5	-	2.5	-	3.5	-	ns
t_{CL}	CLK low level width		3	-	3.5	-	4	-	ns
t_{CS}	$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, DQM setup time		2.5	-	2.5	-	3.5	-	ns
t_{DH}	Date-in hold time		1.5	-	1.5	-	1.5	-	ns
t_{DS}	Data-in setup time		2.5	-	2.5	-	3.5	-	ns
t_{HZ}	Data-out high impedance time		3.5	10	3.5	10	3.5	10	ns
t_{LZ}	Data-out low impedance time		3	-	3	-	3	-	ns
t_{MTC}	Load Mode Register command to command		1	-	1	-	1	-	t_{CK}
t_{OH}	Data-out hold time		3.5	-	3.5	-	3.5	-	ns
t_{RAS}	Active to Precharge command period		45	120K	60	120K	72	120K	ns
t_{RC}	Auto Refresh and Active to Active command period		67.5	-	90	-	100	-	ns
t_{RCD}	Active to Read, Write or Block Write delay		22.5	-	30	-	36	-	ns
t_{REF}	Refresh Period (1024 cycles) for Non Self-Refresh parts		-	16	-	16	-	16	ms
t_{REF}	Refresh Period (1024 cycles) for Self-Refresh parts		-	128	-	128	-	128	ms
t_{RP}	Row Precharge time		22.5	-	30	-	36	-	ns
t_{RRD}	Active bank A to Active bank B command period		7.5	-	10	-	12	-	ns
t_{SML}	Load Special Mode Register command to command		1	-	1	-	1	-	t_{CK}
t_T	Transition time		1	30	1	30	1	30	ns
t_{WR}	Write recovery time		7.5	-	10	-	12	-	ns
t_{XSR}	Exit Self Refresh to Active command		100	-	100	-	100	-	ns

Detailed Operation

Initialization and Load Mode Register

The SGRAM must be initialized at power up time to prevent undefined operations. The diagram on page 32 shows this process in detail. The next step is to load the mode register to program the burst length, and burst type. The Load Mode Register and Special Mode Register functions have been described earlier.

The initialization of the device and loading of the Mode Register is shown in the diagram on page 32. If the device is not initialized prior to issuing a command, it may result in an undefined operation. The Mode Register should be loaded to let the device know about burst type, length of burst, $\overline{CAS}$ Latency, Sequence and number of Color Registers to be used.

Auto Refresh (REF)

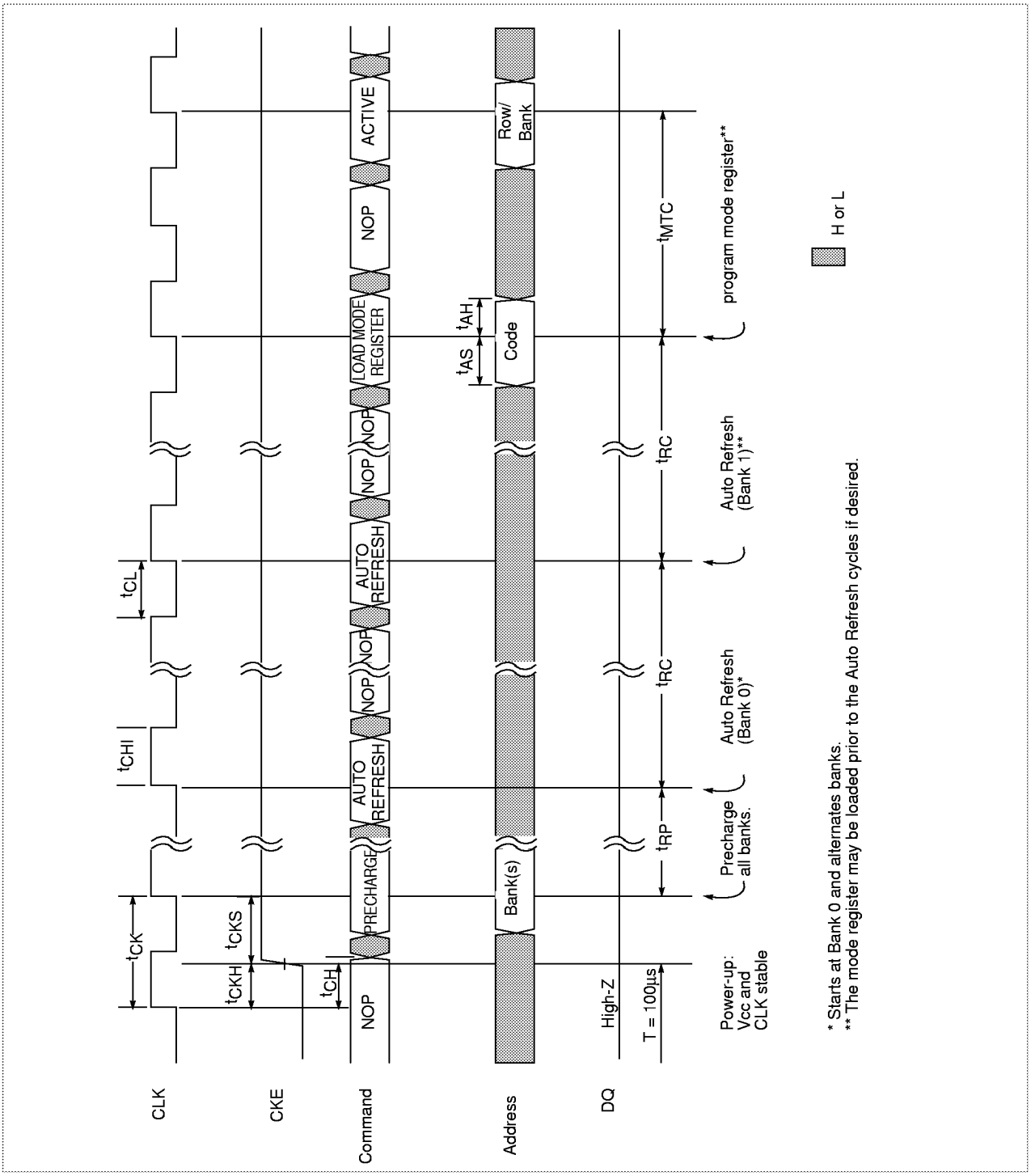
This mode is similar to CBR used in conventional DRAMs to refresh the DRAM rows.

This command is essential to refresh the volatile DRAM cells every 16ms. The device could be refreshed by issuing 1024 Auto Refresh cycles every 16ms or these refresh cycles could be interleaved between various operations as long as each DRAM cell is refreshed every 16ms or less.

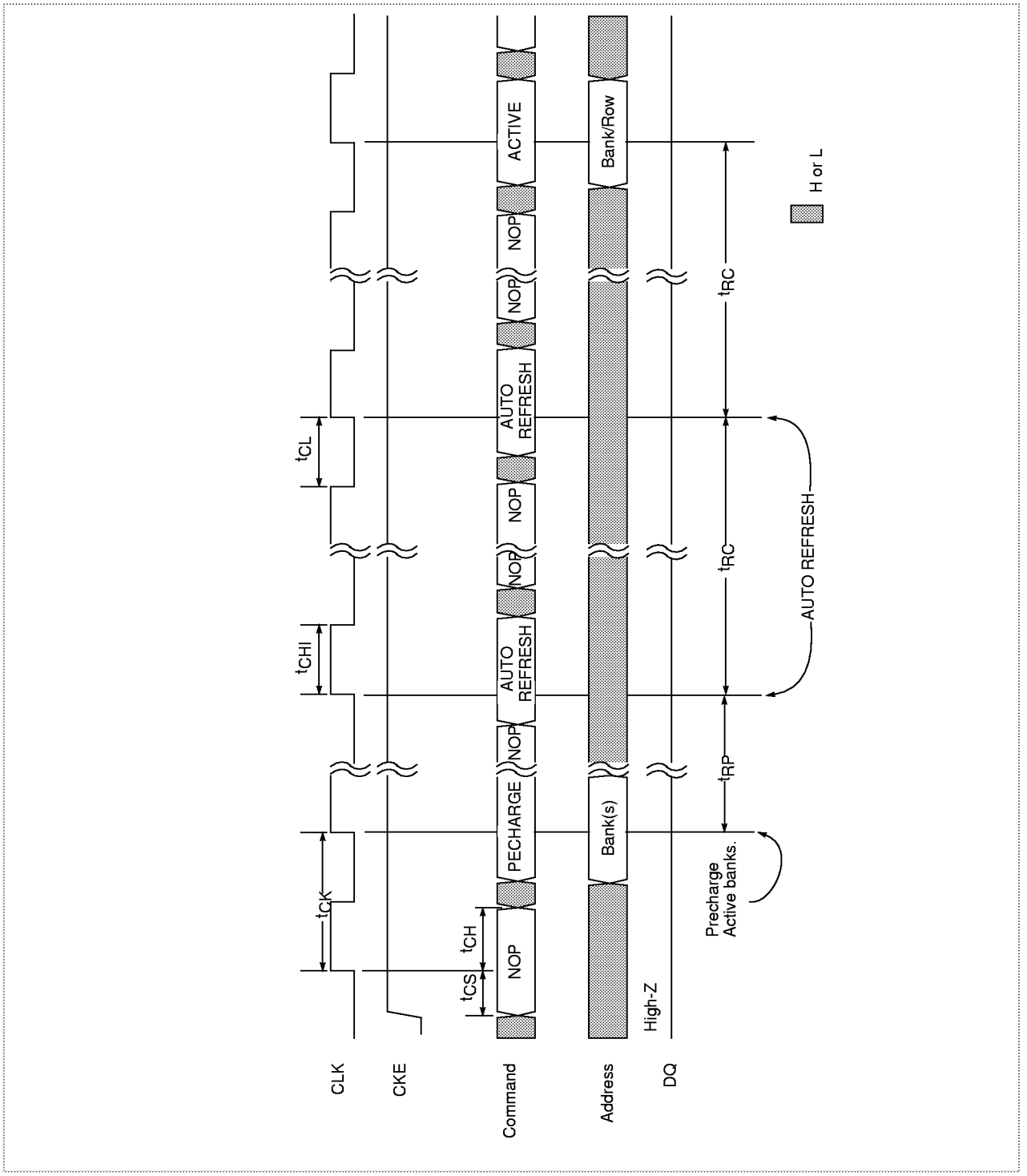
Logic Table for Auto Refresh Command Cycle

Mnemonic	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	BA (A_9)	A_8	A_7-A_0
REF	H	L	L	L	H	L	X	X	X	X

Initialize and Load Mode Register Operation



Auto Refresh Mode



Bank/Row Activation Command (ACT)

Before any Read or Write commands can be issued to a bank within the SGRAM, a row in that bank must be "opened". An Active command is used for this purpose. The Active command is also used to determine whether or not the Write-per-Bit mask is to be applied during Write and Block Write cycles within that row.

A subsequent Active command to a different row in the same bank can only be issued after the previous Active row has been "closed". The minimum time interval between successive Active commands to the same bank is defined by t_{RC}.

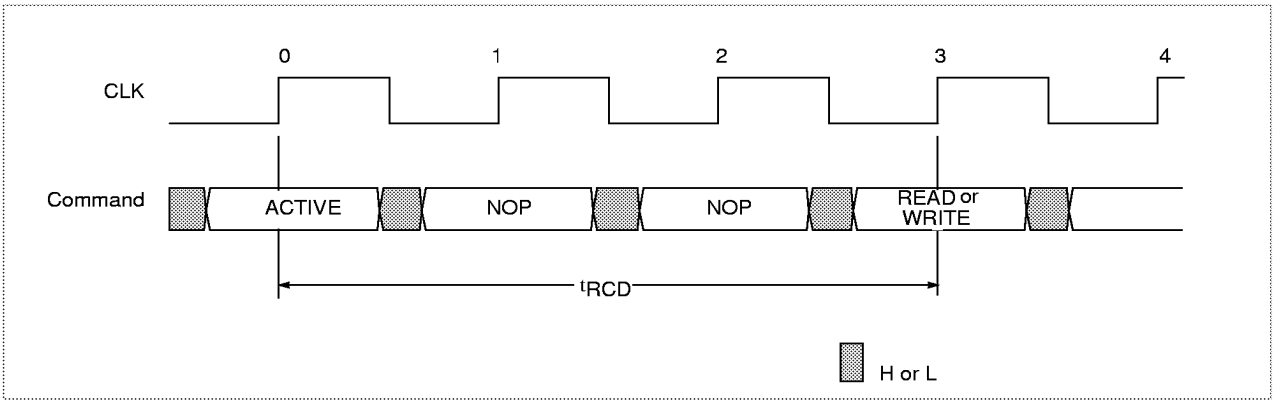
A subsequent Active command to the other bank can be issued while the first bank is being accessed, which results in a reduction of total row access overhead. The minimum time interval between successive Active commands to different banks is defined by t_{RRD}.

Logic Table for Active Command

Mnemonic	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	BA (A_9)	A_8	A_7-A_0
ACT	H	L	L	H	H	L	X	BS	Row Address	
ACTM	H	L	L	H	H	H	X	BS	Row Address	

The diagram on page 34 shows the Read/Write command delay in the same bank after the Active command has been registered. Also are shown the various timing parameters that are applicable to the Read/Write operations.

Example Meeting t_{RCD} (min) when $2 \leq t_{RCD}$ (min)/$t_{CK} \leq 3$



Read Command (RD)

The following pages describe in detail the Read operations with the help of timing diagrams for various cases.

Logic Table for Read Command

Mnemonic	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	BA (A_9)	A_8	A_7-A_0
RD	H	L	H	L	H	L	0/1	BS	L	Column
RDA	H	L	H	L	H	L	0/1	BS	H	Column

Read bursts are initiated with a Read command. The starting column address and the bank address are provided with the Read command and Auto Precharge is either enabled or disabled for that burst access. Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A Full Page Burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).

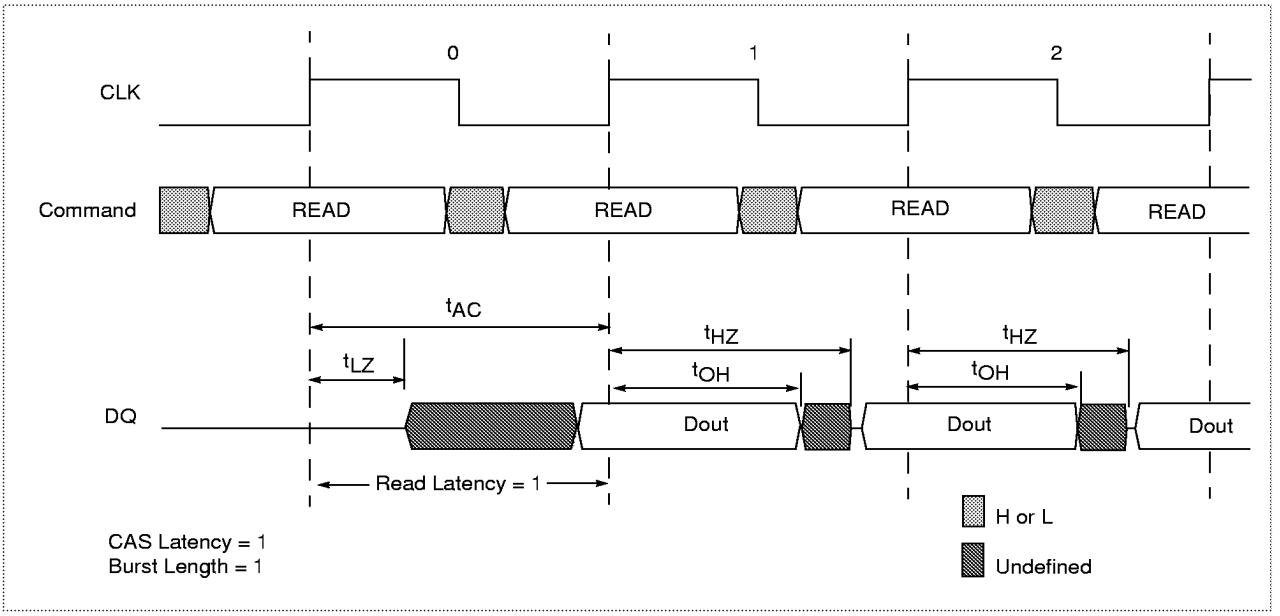
Various cases of Reads are shown. The user can use latency of one, two or three depending upon the system clock. A fixed-length Read Burst may be followed by or truncated with a Write burst or Block Write command (provided that Auto Precharge was not activated) and a Full Page Read burst may be truncated by a Write burst or Block Write command. The Write burst may be initiated on the clock edge immediately following the last (or last desired) data element from the Read burst, provided that I/O contention can be avoided. ***It is generally a good design practice that a single cycle delay must occur between the last data read and the Write command.***

The DQM inputs are used to avoid I/O contention as shown in the second diagram on page 40. The DQMs must be asserted High at least two clocks (DQM latency is two clocks for output buffers) prior to the Write command to suppress data-out due to the previous Read command. Once the Write command is registered, the output buffers will go High-Z (or remain High-Z) regardless of the state of DQM signals. The DQM signals must be de-asserted (DQM latency is zero clocks for input buffers) prior to the Write command to ensure that the written data is not masked. The first diagram on page 40 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and the second diagram on page 40 shows the case where the additional NOP is needed.

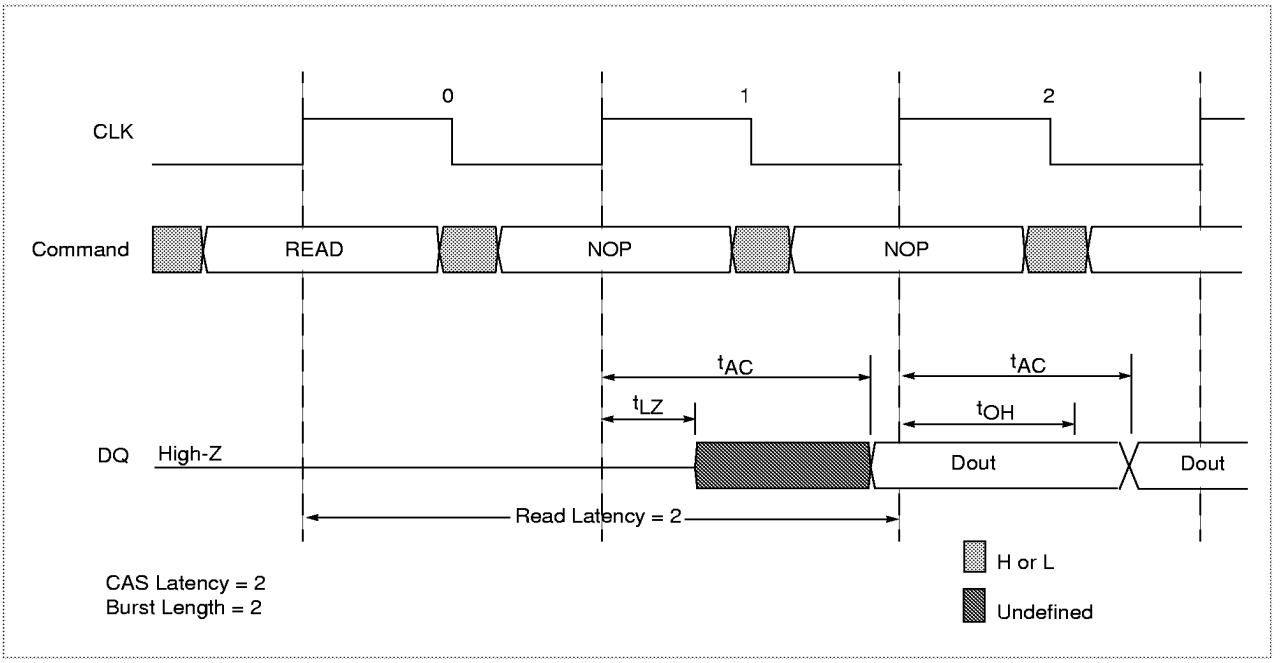
A fixed-length as well as a Full Page Read burst may be truncated with a Precharge command to the same bank. Note that the Precharge command should be issued one cycle before the clock edge at which the last desired data is valid. A subsequent command can not be issued to the same bank until t_{RP} is met. Part of the row precharge time is hidden during the access of the last data element. An Auto Precharge command can be used in place of Precharge command for fixed length bursts. The disadvantage of Auto Precharge command is that it does not truncate fixed-length bursts and does not apply to Full Page Bursts.The disadvantage of the Precharge is that it requires the command and address busses to be available at the appropriate time to issue the command.

The full-page, as well as fixed-length Read burst may be terminated with the Burst Terminate command. The fixed-length Burst with Auto Precharge can not be truncated by Burst Terminate command. ***The Burst Terminate command should be issued one cycle before the positive clock edge at which the last desired data element is valid.***

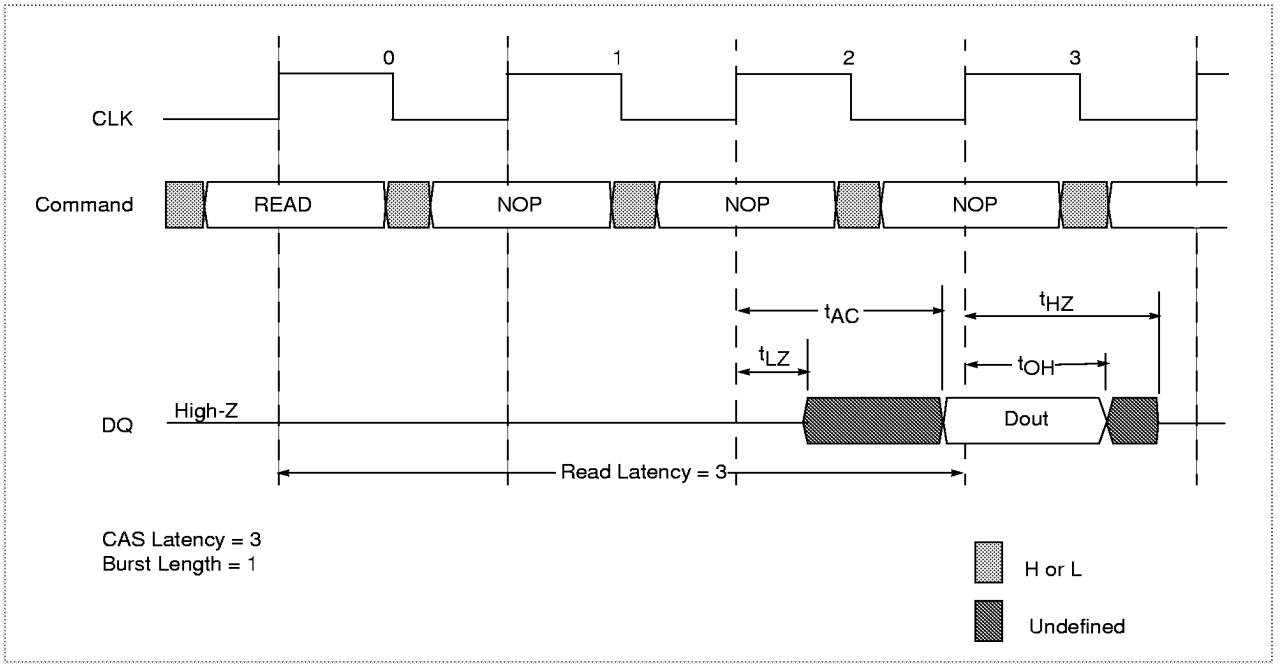
One Clock Read Latency Example



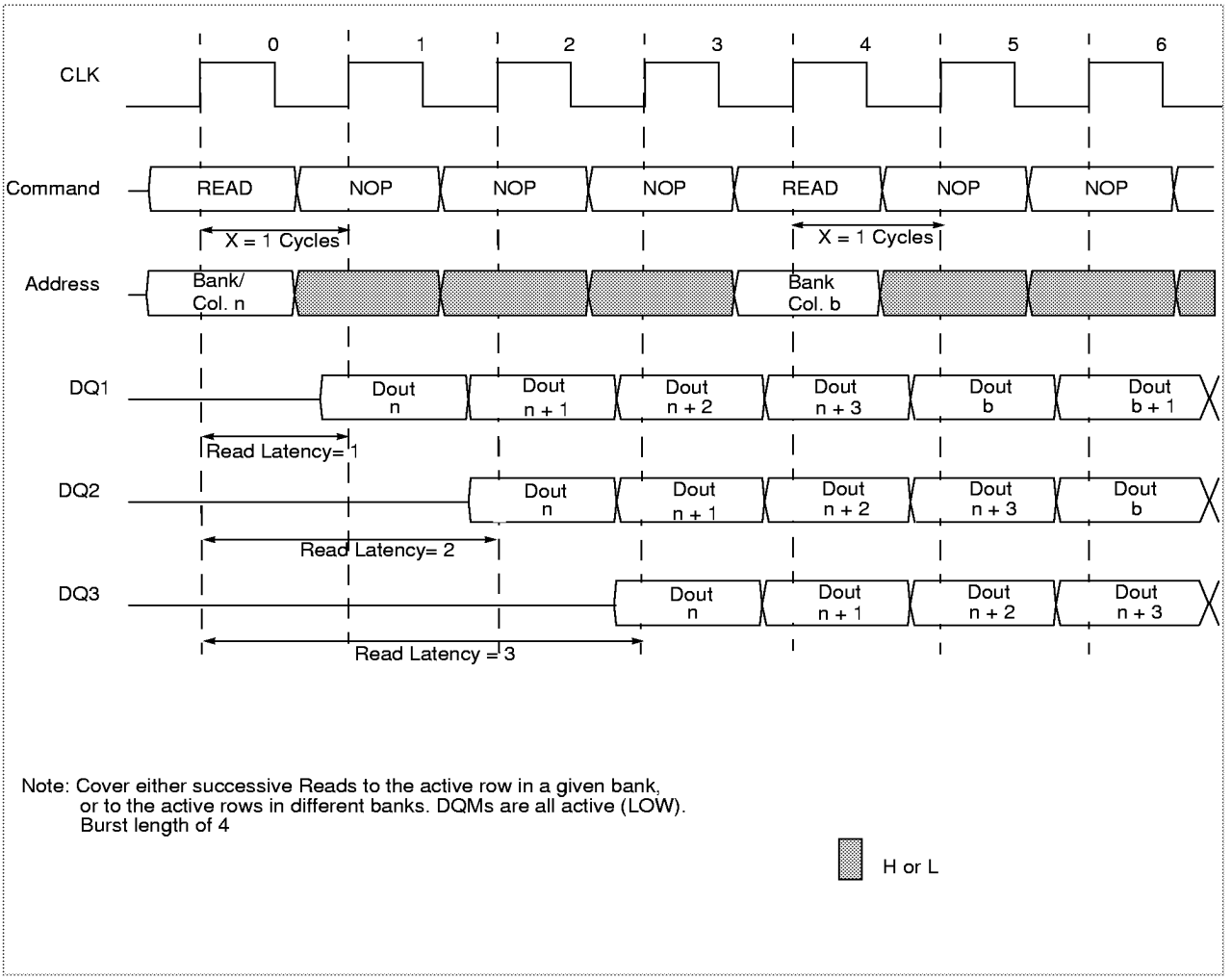
Read Burst with Read Latency = 2



Read Burst with Read Latency = 3

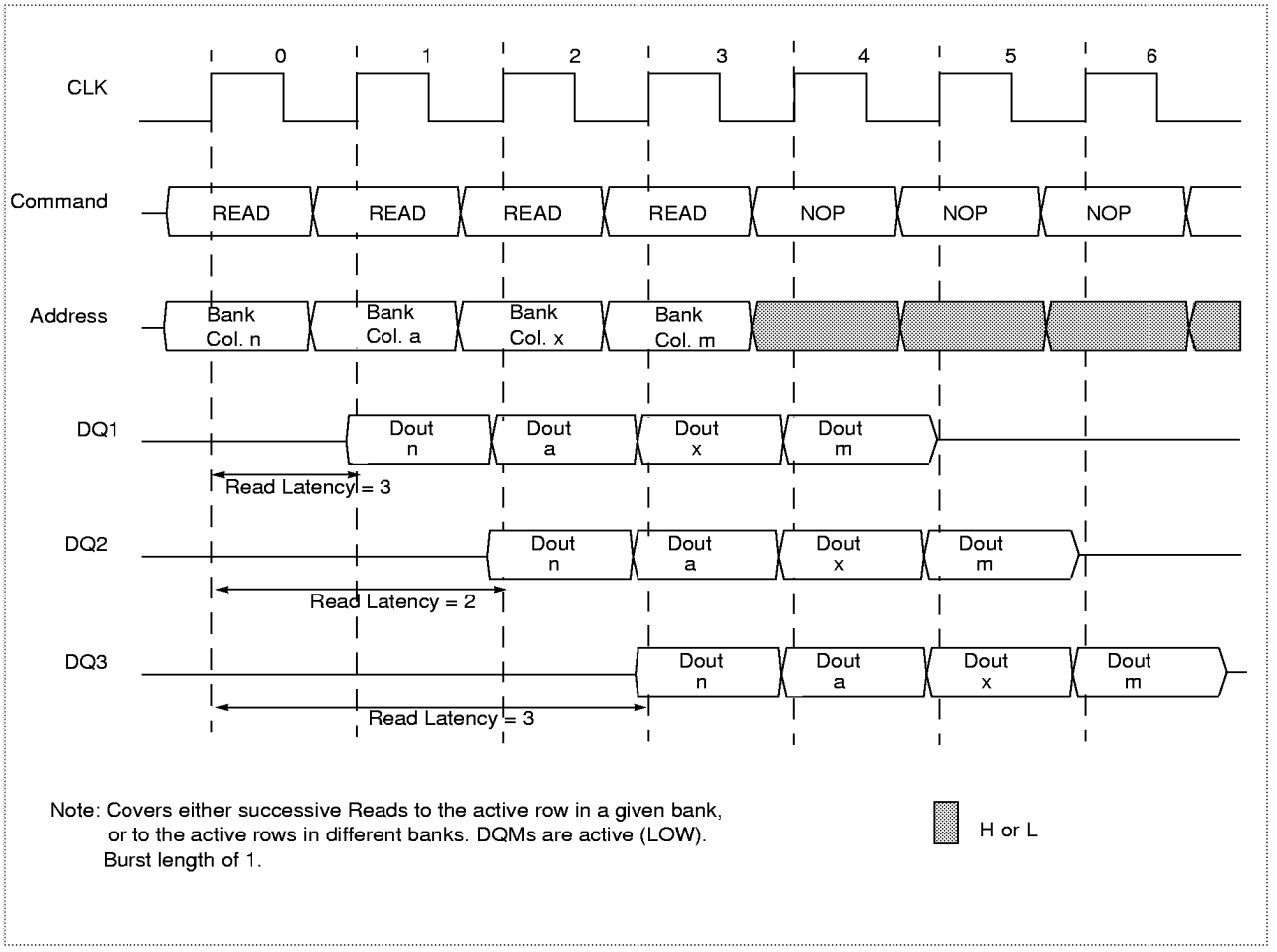


Consecutive Read Bursts, Read Latency = 1, 2, 3



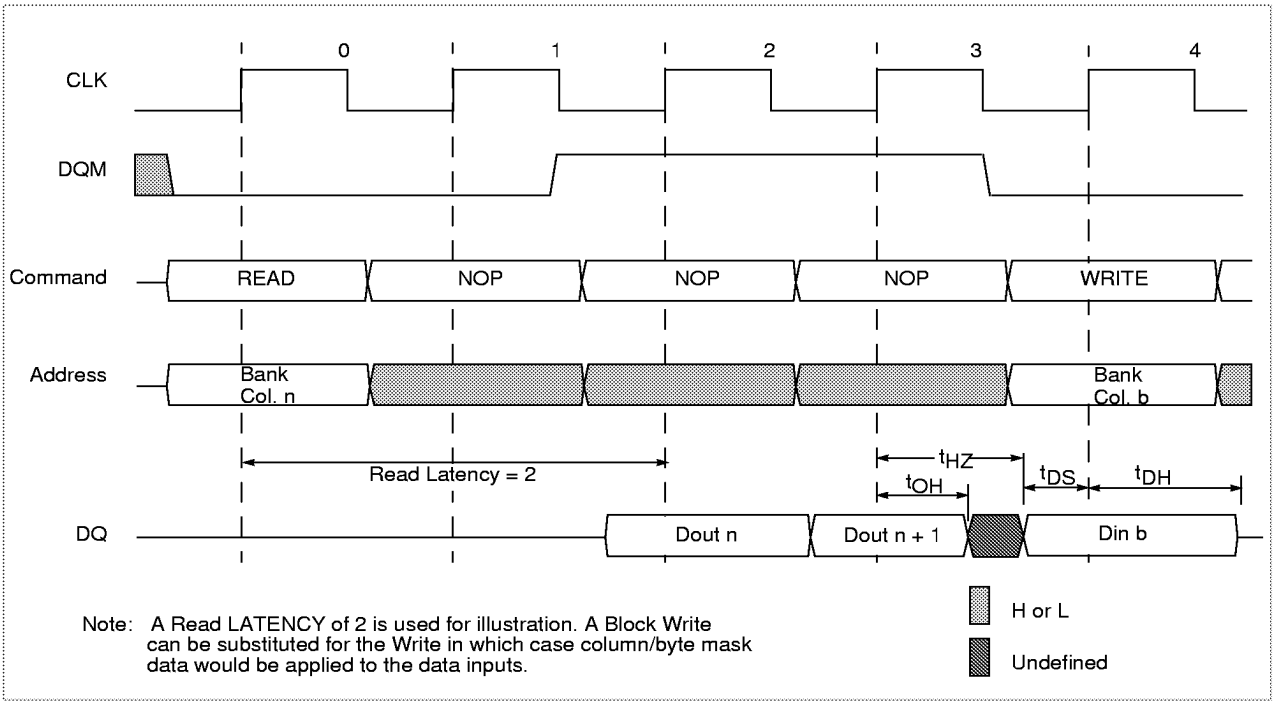
Note: Cover either successive Reads to the active row in a given bank,
or to the active rows in different banks. DQMs are all active (LOW).
Burst length of 4

Random Read Accesses within a Page, Read Latency = 1, 2, 3



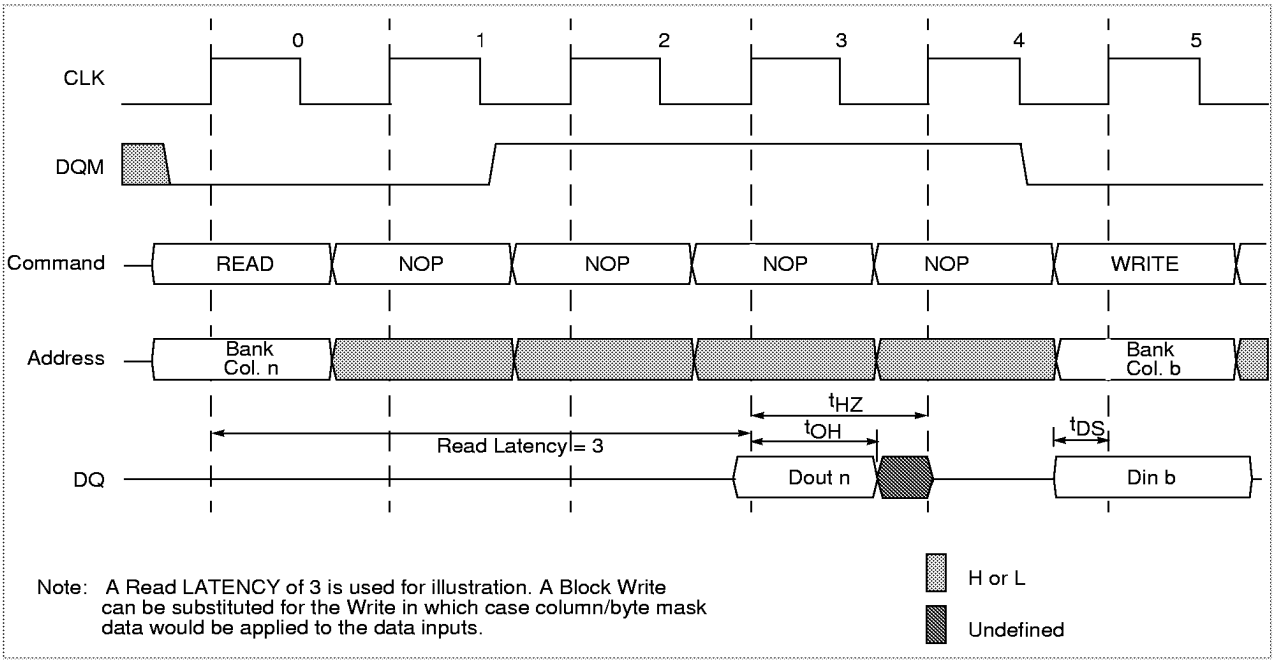
Note: Covers either successive Reads to the active row in a given bank, or to the active rows in different banks. DQMs are active (LOW). Burst length of 1.

Read to Write (or Block Write)



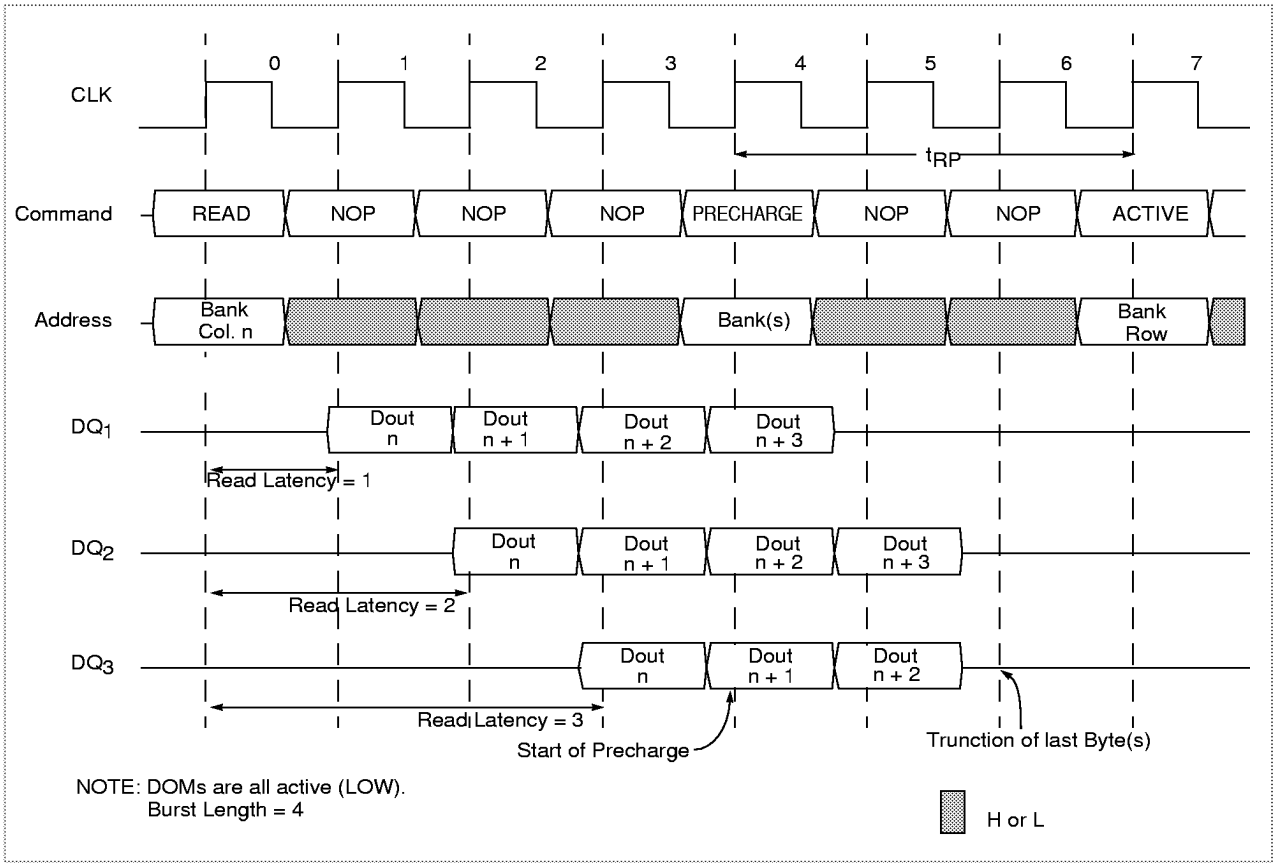
Note: A Read LATENCY of 2 is used for illustration. A Block Write can be substituted for the Write in which case column/byte mask data would be applied to the data inputs.

Read to Write with Extra Clock Cycle in between to avoid Contention

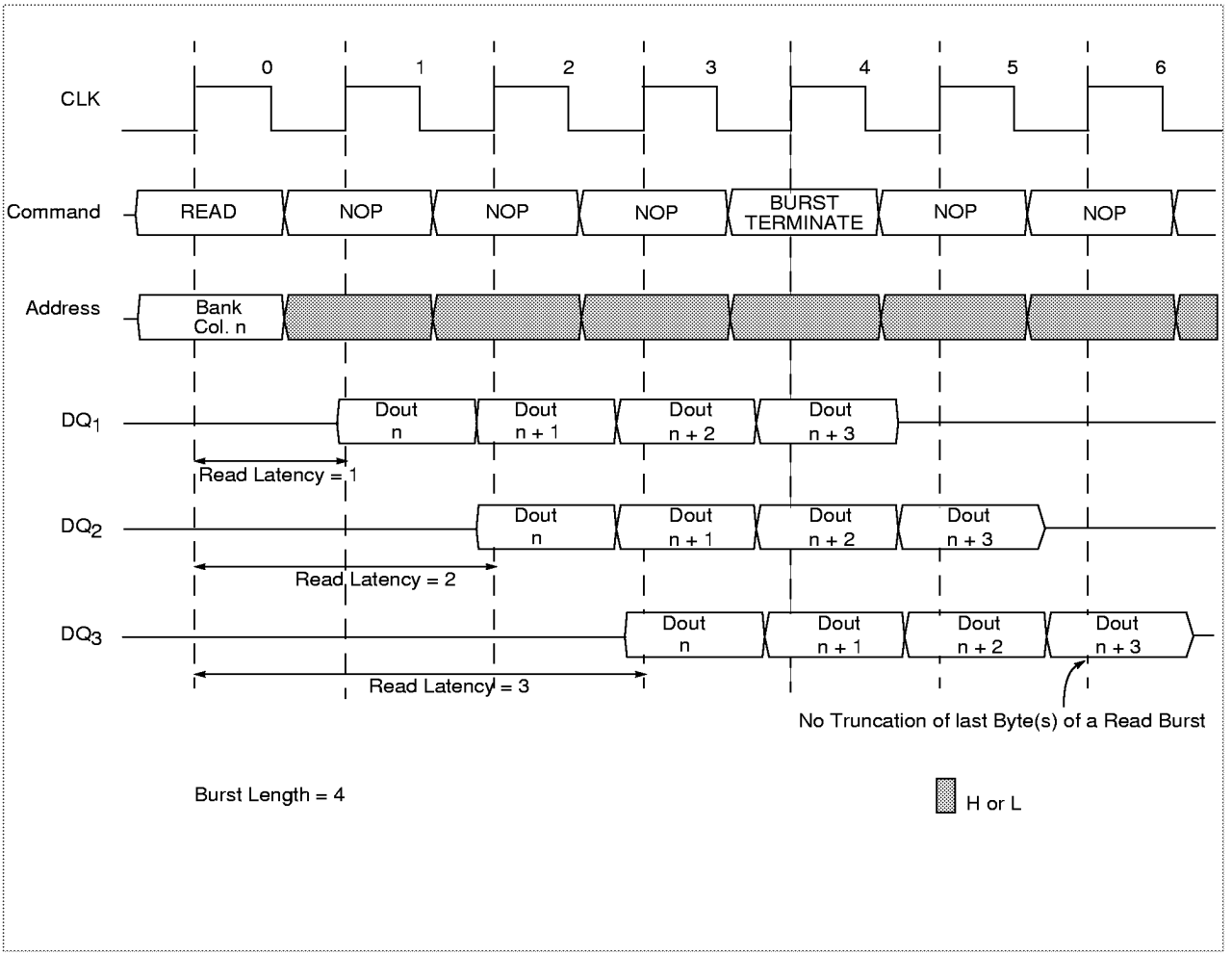


Note: A Read LATENCY of 3 is used for illustration. A Block Write can be substituted for the Write in which case column/byte mask data would be applied to the data inputs.

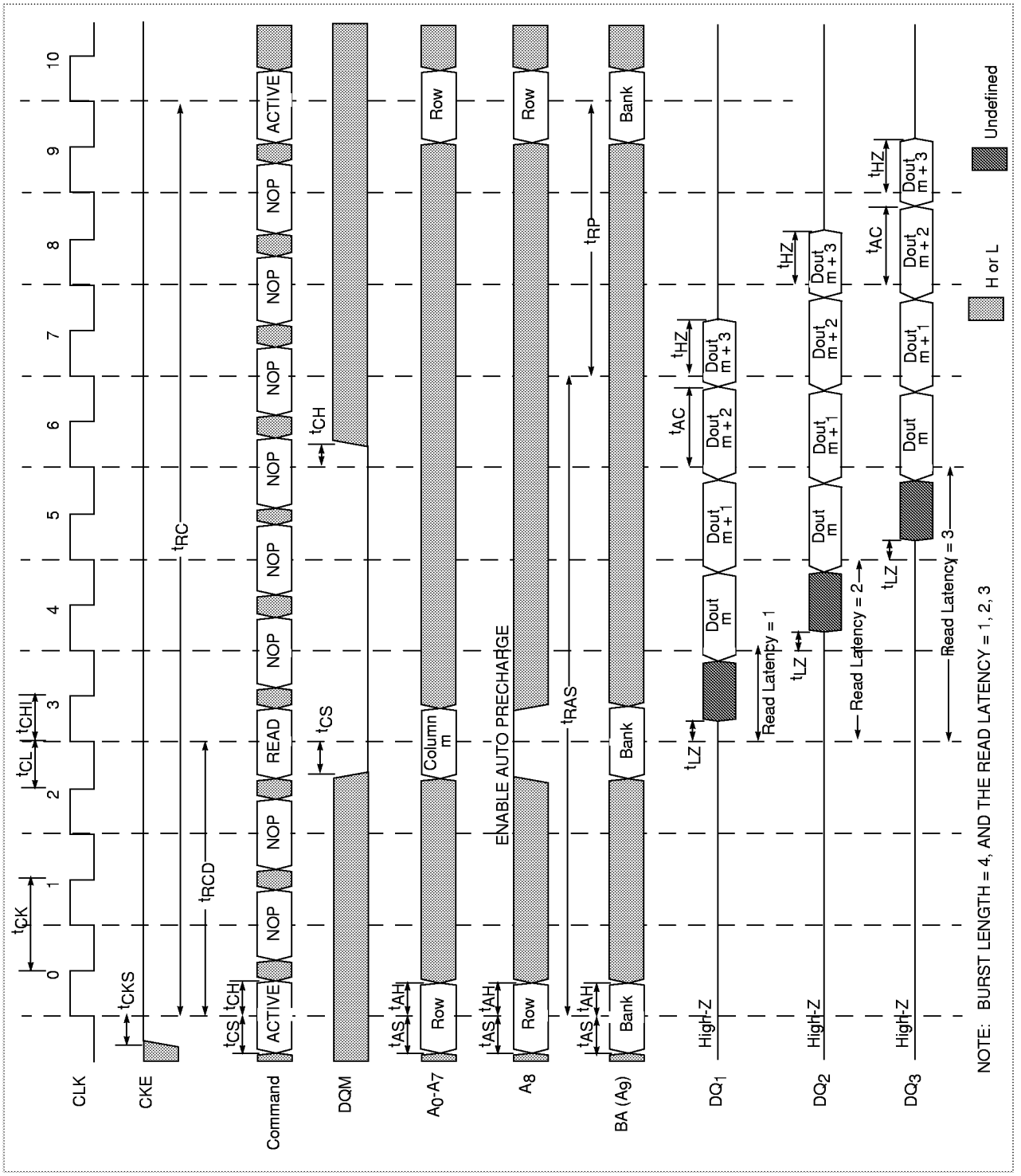
Read Interruption by Precharge Command, Read Latency = 1, 2, 3



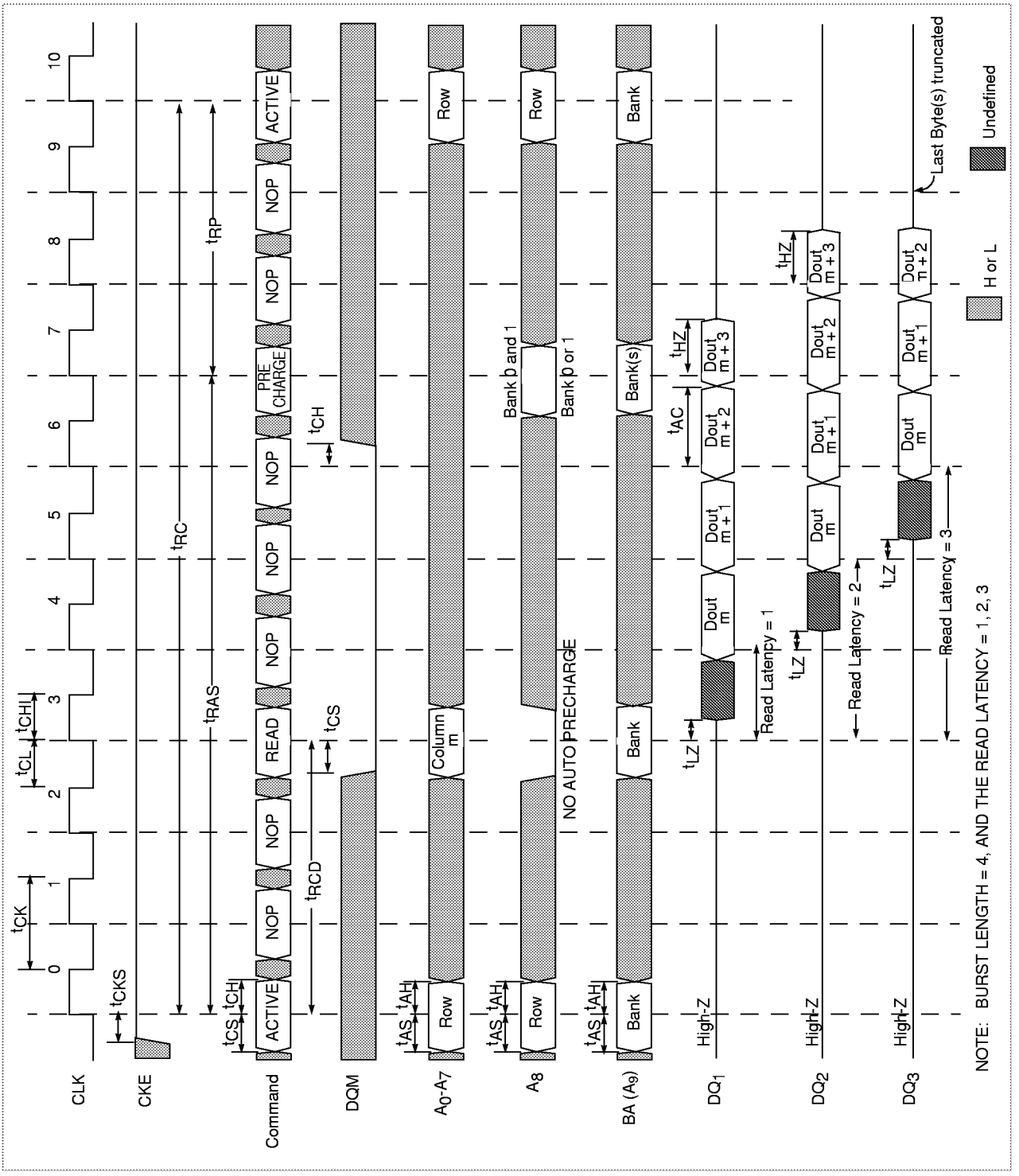
Terminating a Read Burst with a Burst Terminate command, Read Latency = 1, 2, 3



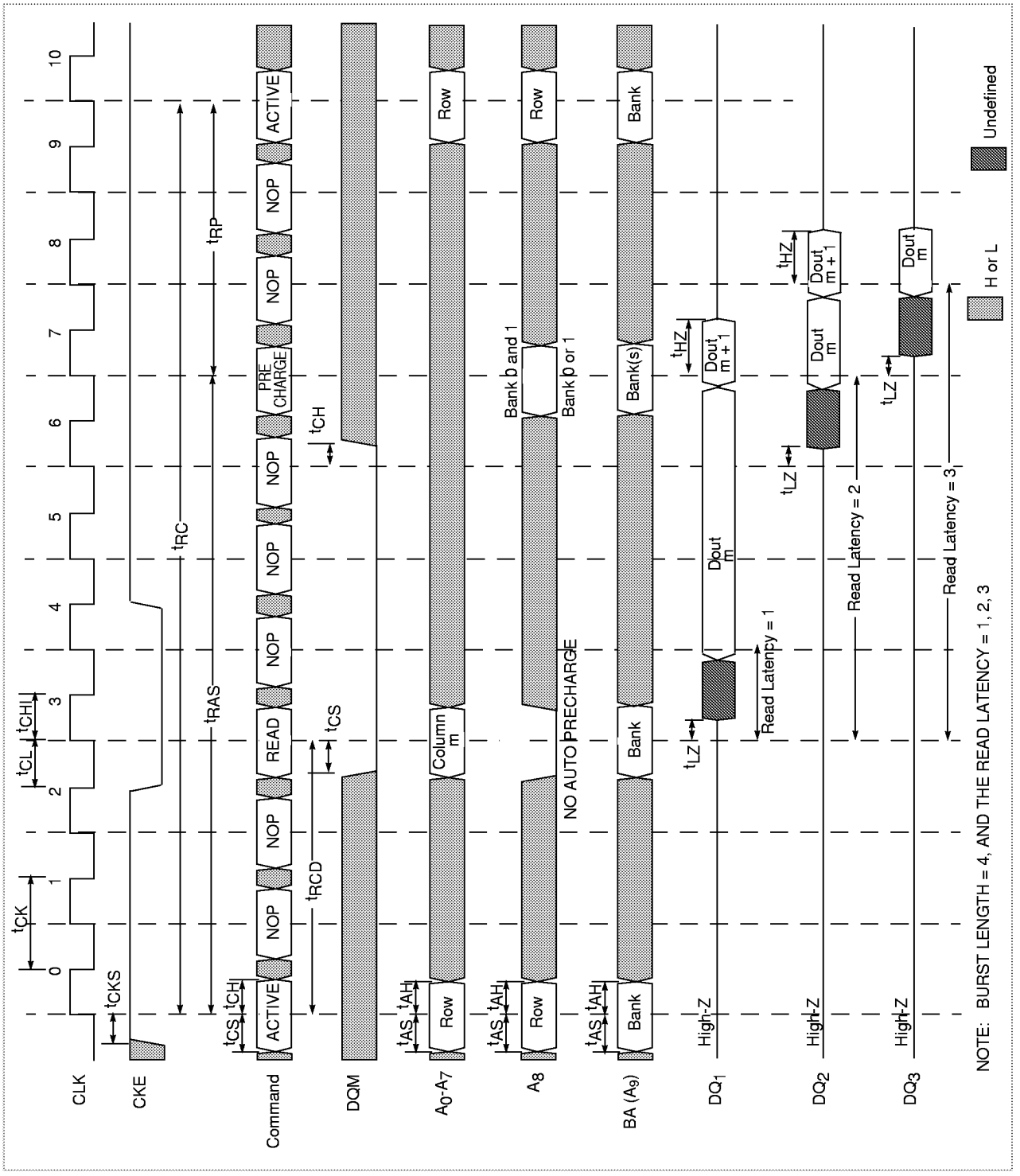
Read with Auto Precharge



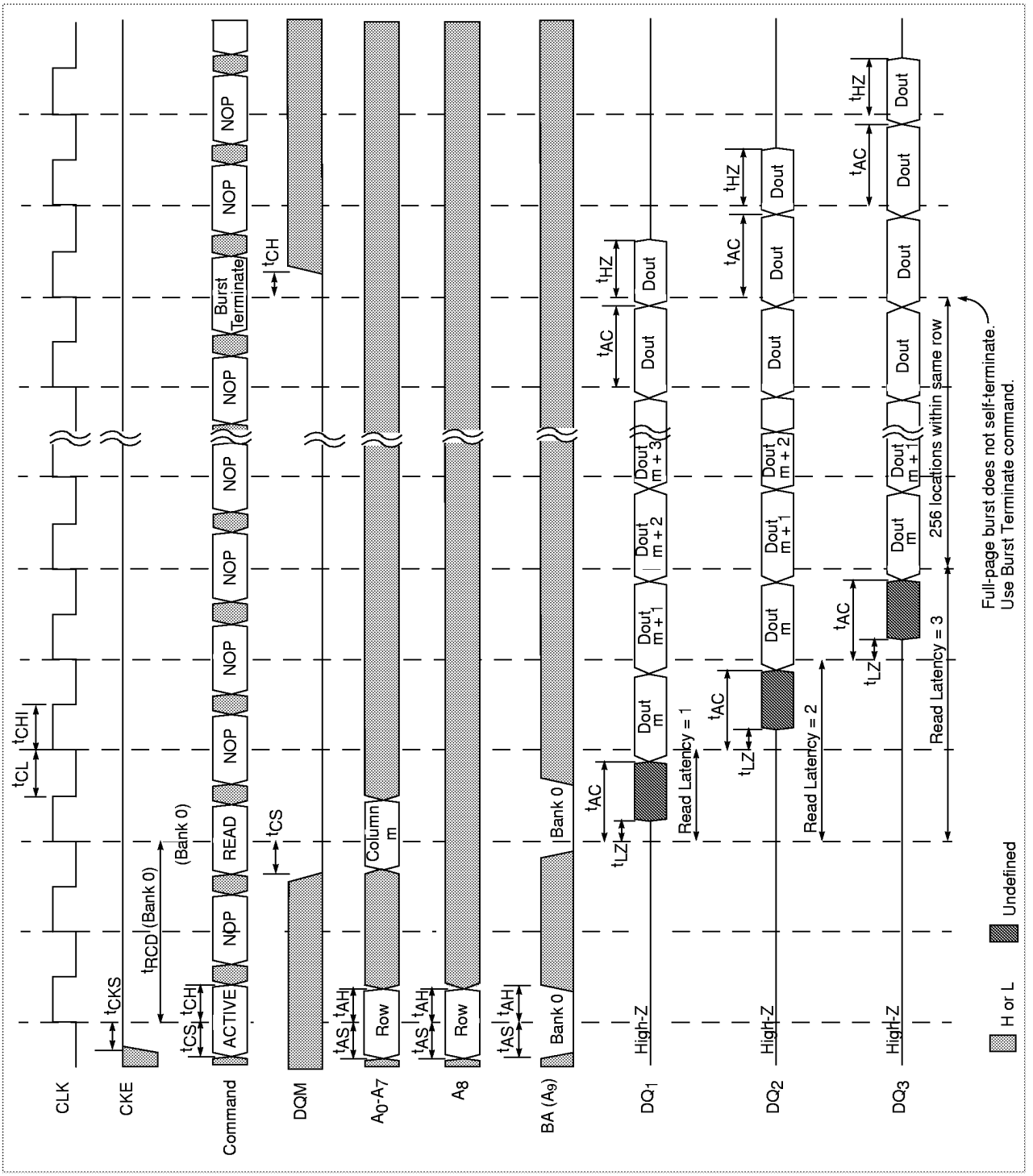
Read without Auto Precharge



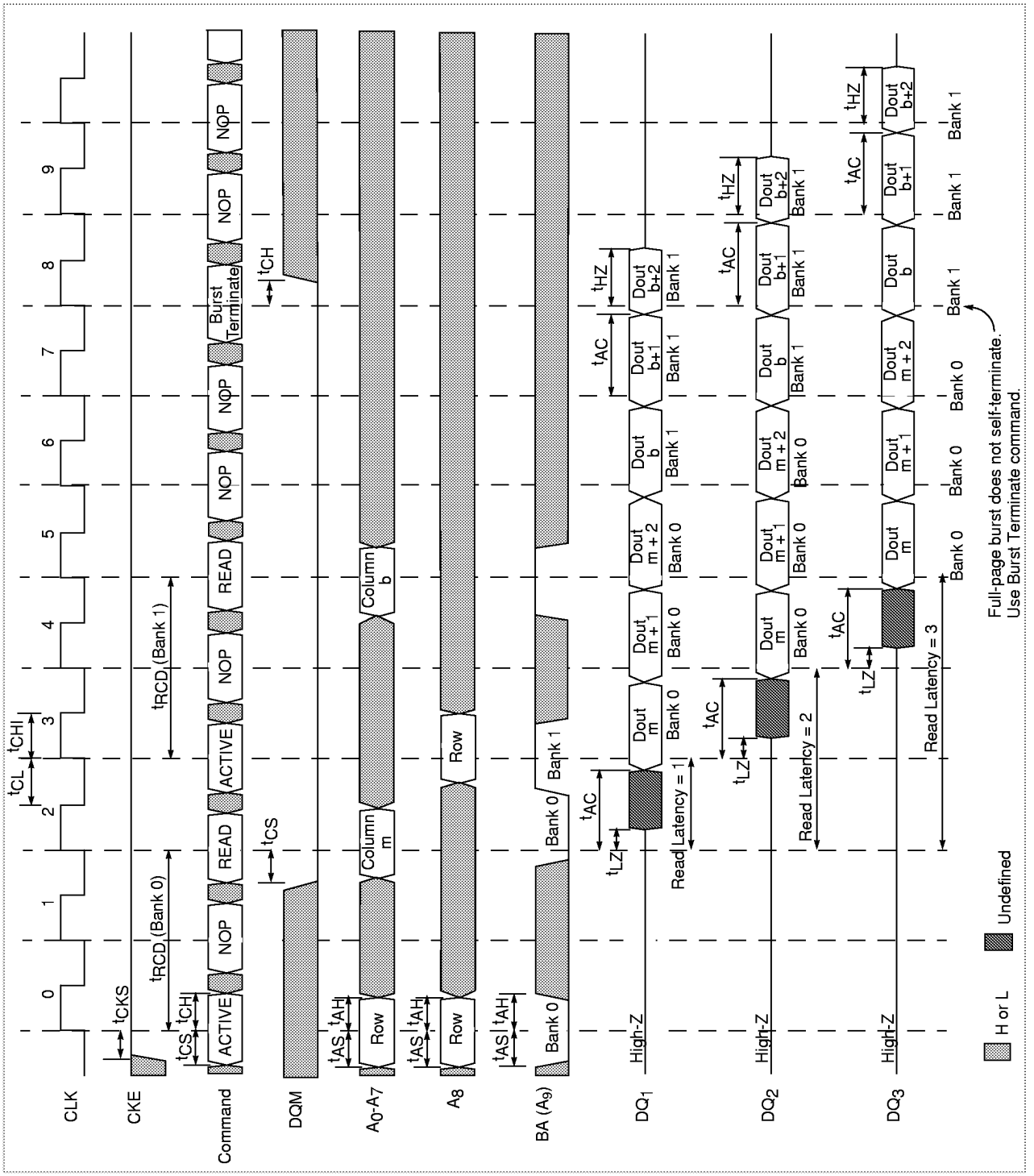
Read without Auto Precharge - Clock Suspension



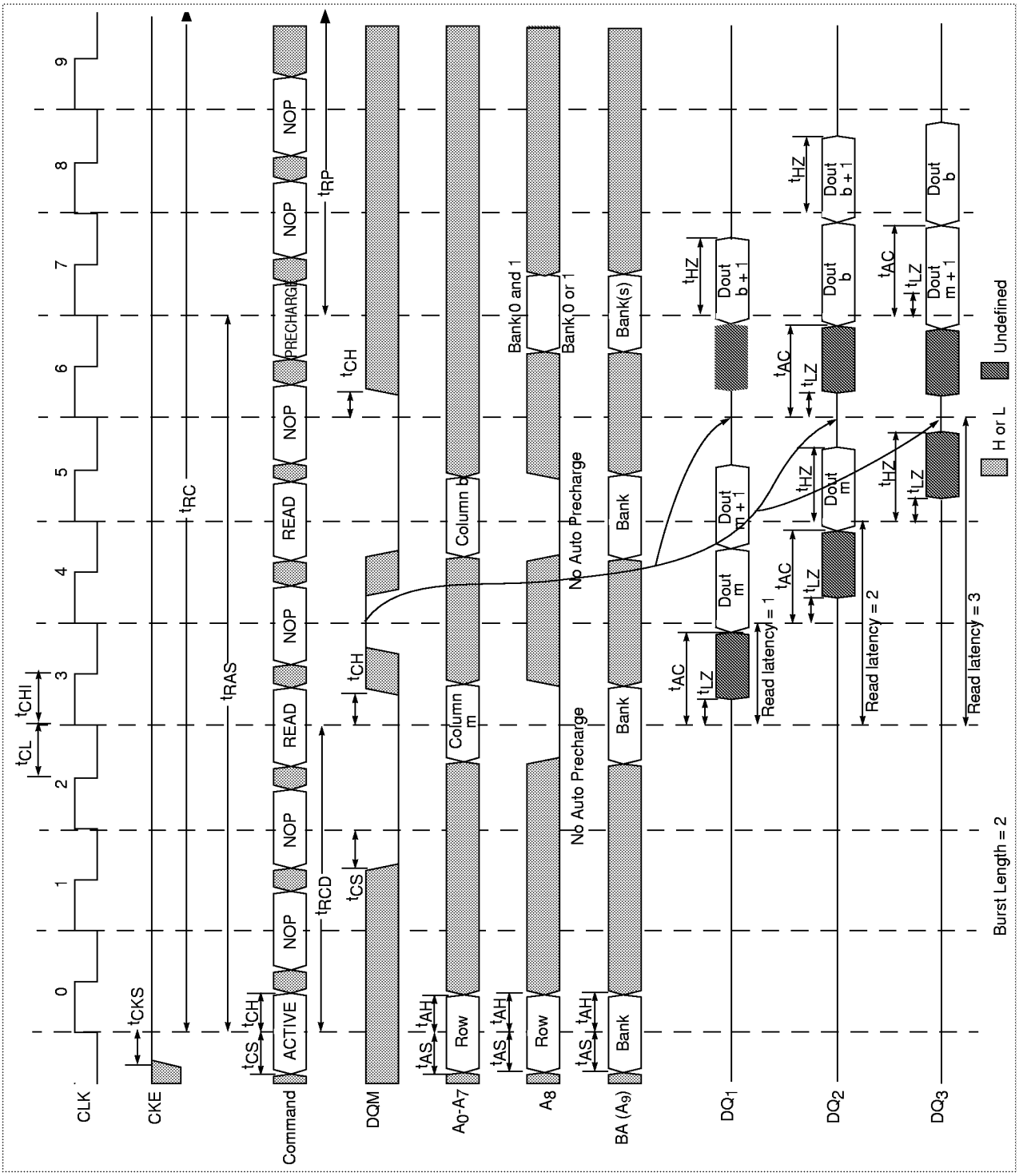
Read Full Page Burst



Read Full Page Burst (Interleaving two banks)



Read DQM Operation



Write Command (WR)

The following pages illustrate the Write operations for various cases with the help of timing diagrams.

Logic Table for Write Command

Mnemonic	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	BA (A_9)	A_8	A_7-A_0
WR	H	L	H	L	L	L	0	BS	L	Column
WRA	H	L	H	L	L	L	0	BS	H	Column
BW	H	L	H	L	L	H	0	BS	L	Column
BWA	H	L	H	L	L	H	0	BS	H	Column

Note: Input data at DQ pins at Block Write command time is registered as a column mask for that block of columns.

Write bursts are initiated with a Write command. The starting column and bank address is provided with the Write command, normal or Block Write is selected, and Auto Precharge is either enabled or disabled for that access. If Auto Precharge is enabled, the row being accessed is precharged automatically at the completion of the burst.

During Write bursts, the first valid data-in element will be registered coincident with the Write command. Subsequent data elements will be registered on successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z, and any additional data will be ignored. A full-page burst will continue until terminated (at the end of the page, it will wrap to column 0 and continue).

A fixed-length Write burst may be followed by, or truncated with a subsequent Write burst or Block Write command (provided that Auto Precharge was not activated) and a full page Write burst can be truncated with a subsequent Write burst or Block Write command. The new Write or Block Write command can be issued on any clock following the previous Write command, and the data provided coincident with the new command applies to the new command.

A fixed-length Write burst may be followed by, or truncated with a subsequent Read burst (provided that Auto Precharge was not activated) and a full-page Write burst can be truncated with a subsequent Read burst. Once the Read command is registered, the data inputs will be ignored, and writes will not be executed.

A fixed-length Write burst may be followed by, or truncated with a Precharge command to the same bank (provided that Auto Precharge was not activated) and a full-page Write burst may be truncated with a Precharge command to the same bank. ***The Precharge command should be issued x cycles (x = t_{WR}/t_{CK} rounded up to the next whole number) after the clock edge at which the last desired input data element is registered.*** In addition, the DQM signals must be used to mask input data, starting with the clock edge following the last desired data element and ending with the clock edge on which the Precharge command is entered. A Precharge command issued at the optimum time provides the same operation that would result from the same fixed-length Burst with Auto Precharge.

Disadvantages of Write command with Auto Precharge

1. Back to back Read/Write bursts can not be initiated. The Read/Write command with Auto Precharge will automatically initiate a precharge of the row in the selected bank. Most of the applications require subsequent Read/Write bursts in the same page.
2. The Auto Precharge command does not allow truncation of fixed-length bursts. It also does not apply to Full Page bursts.

Terminating a Write burst

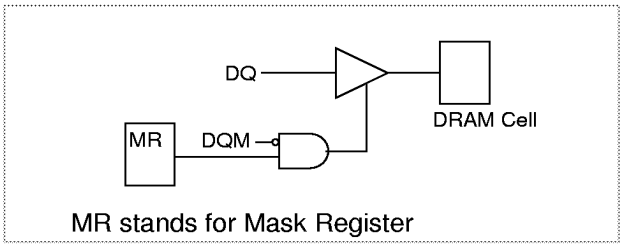
The fixed-length or Full-Page Write bursts can be truncated with the Burst Terminate command. When truncating a Write burst, the input data applied one clock edge prior to the Burst Terminate command will be the last data written.

Masked Writes

Any Write performed to a row that was activated via an Active with WPB command is a Write-per-Bit-Mask (WPBM). Data is written to the 32 cells at the selected column location subject to the mask stored in the WPB mask register. The data to be written in the DRAM cell will be according to the following logic.

DQM	MR	DRAM Cell
0	0	Mask
1	0	Mask
1	1	Mask
0	1	Write

Write Masking Functional Representation



If a particular bit in the WPB mask register is a “0”, the data appearing on the corresponding DQ input will be ignored, and the existing data in the corresponding DRAM cell will remain unchanged. If a mask data is a “1”, the data appearing on the corresponding DQ input will be written to the corresponding DRAM cell. ***The overall Write mask consists of a combination of the DQM inputs, which will mask on a per-byte basis, and the WPB mask register, which masks on a per-bit basis***. If a particular DQM signal was registered high, the corresponding byte will be masked. A given bit is written if the corresponding DQM signal registered is “0” and the corresponding WPB mask register bit is “1”. Note that the DQM Latency for Write is zero.

Block Write (BW)

Each Block Write cycle writes a single data value from the color register to the block of eight consecutive column locations addressed by A_7-A_3. The information on the DQs which is registered coincident with the Block Write command is used to mask specific column/byte combinations within the block. The masking of various DQ planes /column is according to the following functional logic.

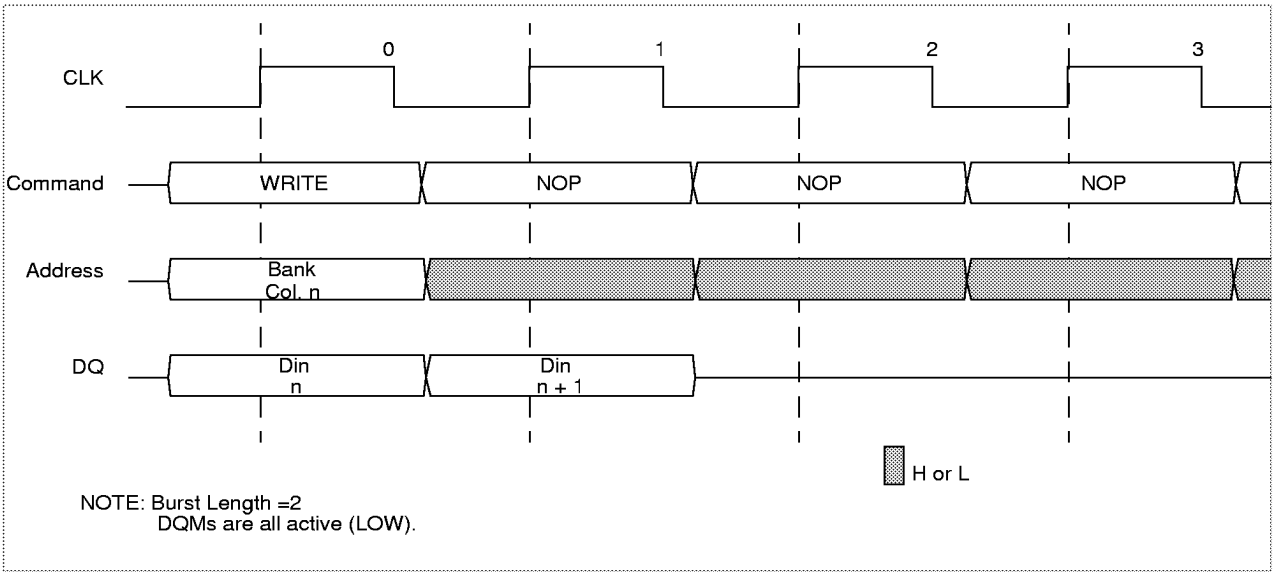
DQs	Column Address			DQ Planes Affected
	A_2	A_1	A_0	
DQ_0 - DQ_7	X	Y	Z	P_0 - P_7
DQ_8 - DQ_{15}	X	Y	Z	P_8 - P_{15}
DQ_{16} - DQ_{23}	X	Y	Z	P_{16} - P_{23}
DQ_{24} - DQ_{31}	X	Y	Z	P_{24} - P_{31}

For example, if DQ_0 is “0”, then {X,Y,Z} becomes {0,0,0} and the column 0 with its planes 0-7 is masked from the selected block of columns. If DQ_{14} is “0”, then {X,Y,Z} becomes {1,1,0} and the column with address 6 with its planes 8-15 is masked from the selected block of columns. When a “0” is registered in a particular DQ signal coincident with a Block Write command, the write to the corresponding column/byte combination is masked. When a “1” is registered, the Color Register data will be written to the corresponding DRAM cells, subject to the DQM and the WPB masking. The overall Block Write mask consists of a combination of the DQM signals, the WPB mask register and the column/byte mask information.

Block Write Timing Considerations.

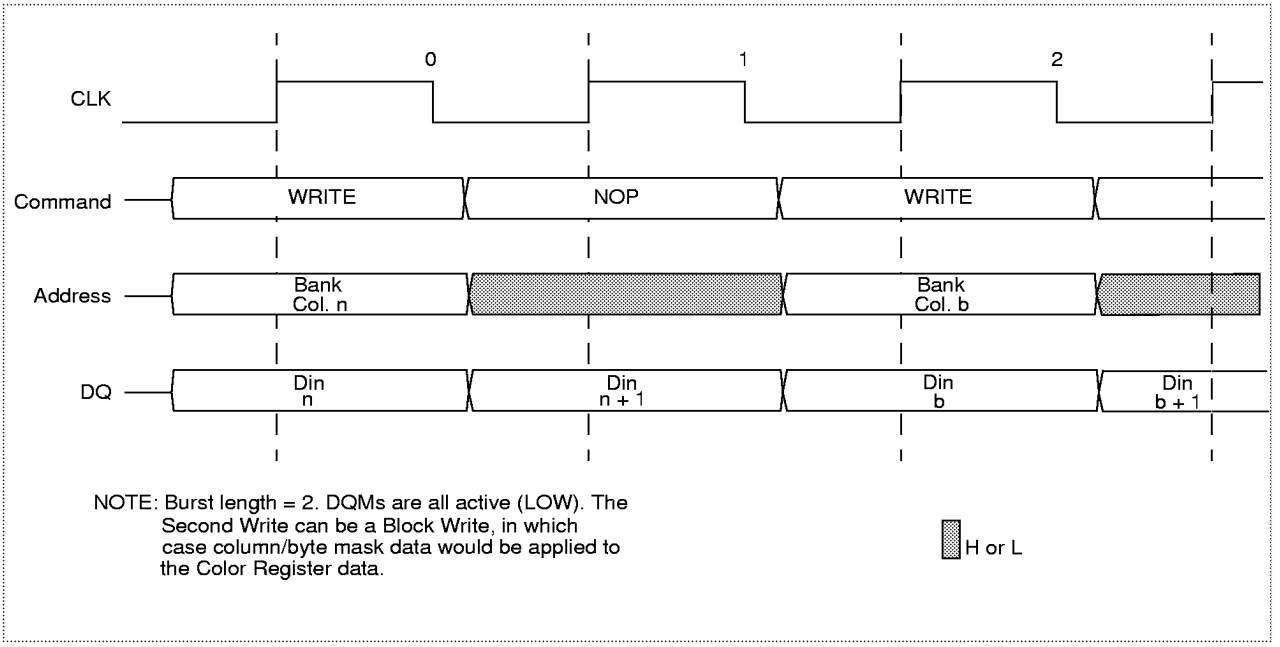
A Block Write access requires a time period of t_{BWC} to execute. When following a Block Write with a Precharge command to the same bank, t_{BPL} must be met.

Write Burst



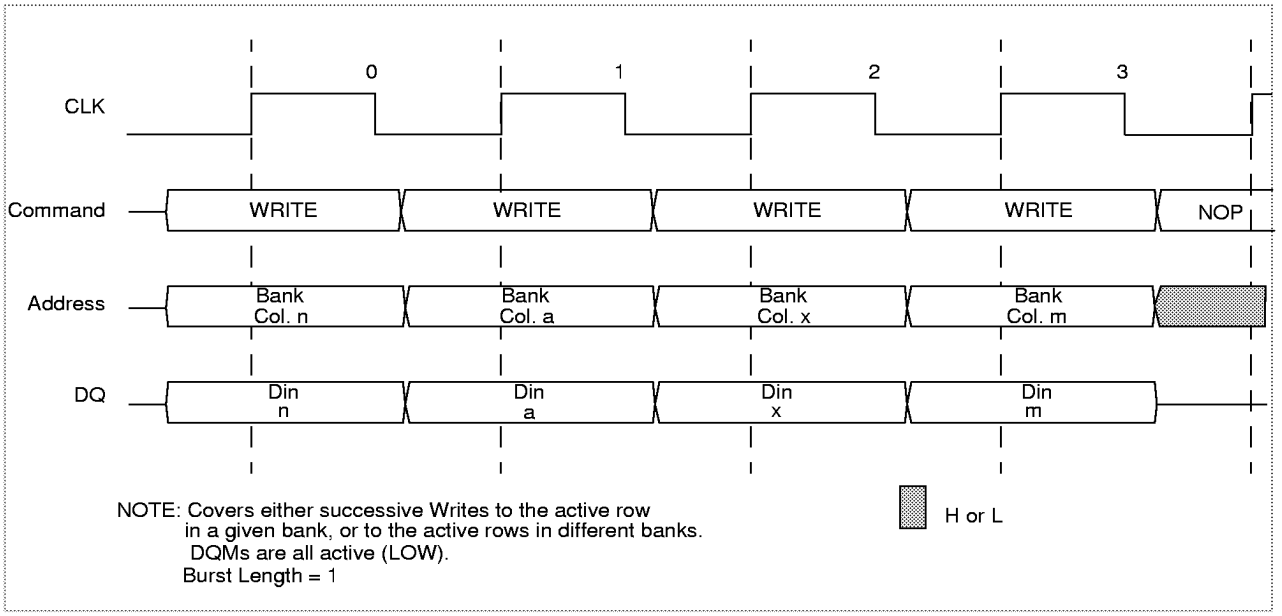
NOTE: Burst Length =2
DQMs are all active (LOW).

Write to Write (or Block Write)



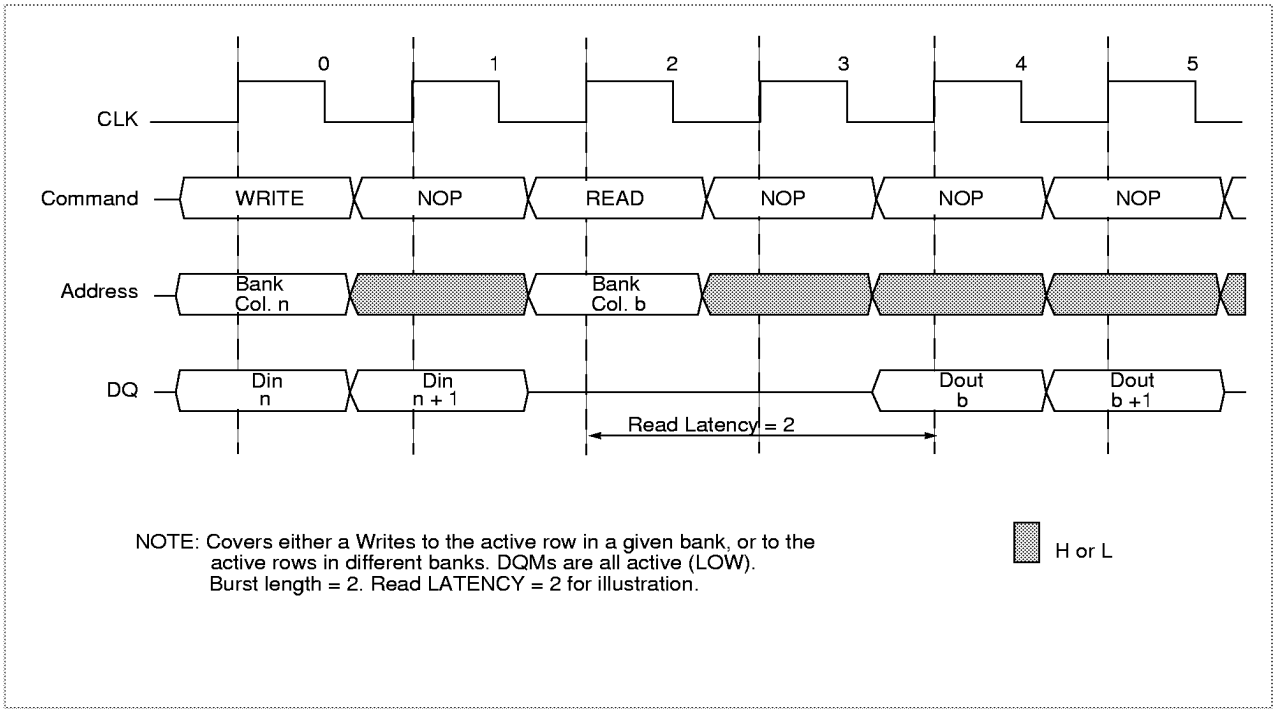
NOTE: Burst length = 2. DQMs are all active (LOW). The Second Write can be a Block Write, in which case column/byte mask data would be applied to the Color Register data.

Random Write (or Block Write) Cycles within a Page



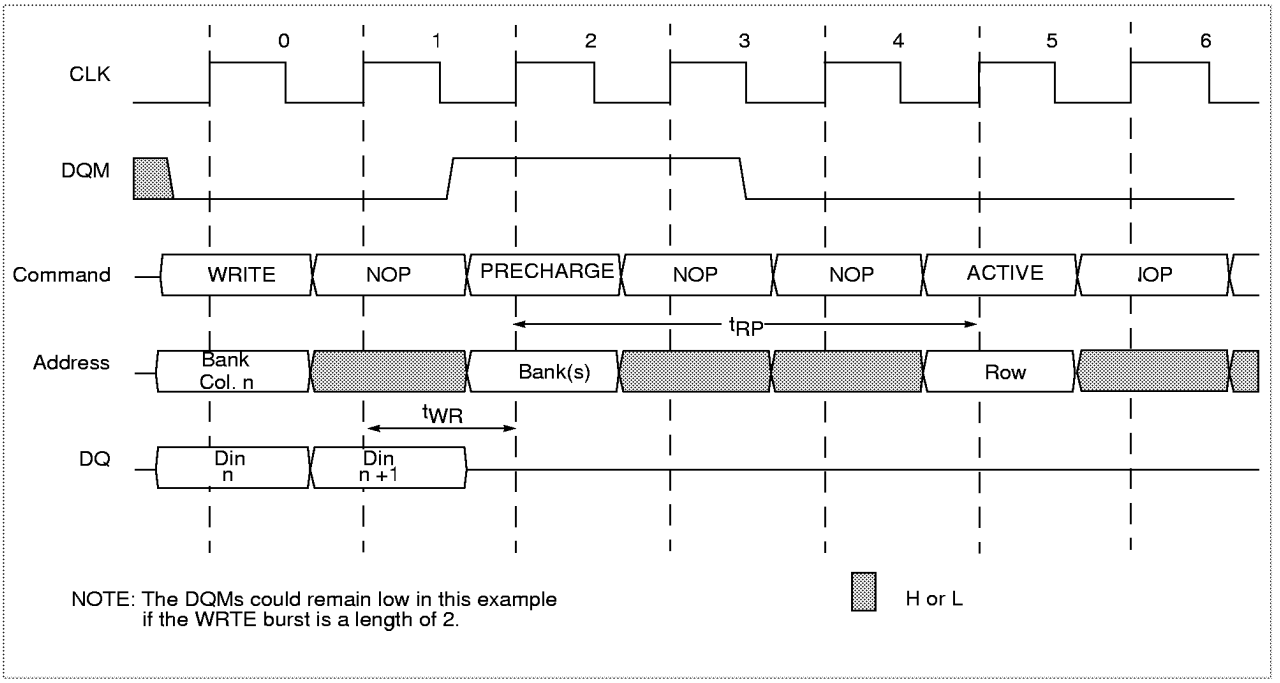
NOTE: Covers either successive Writes to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW). Burst Length = 1

Write to Read

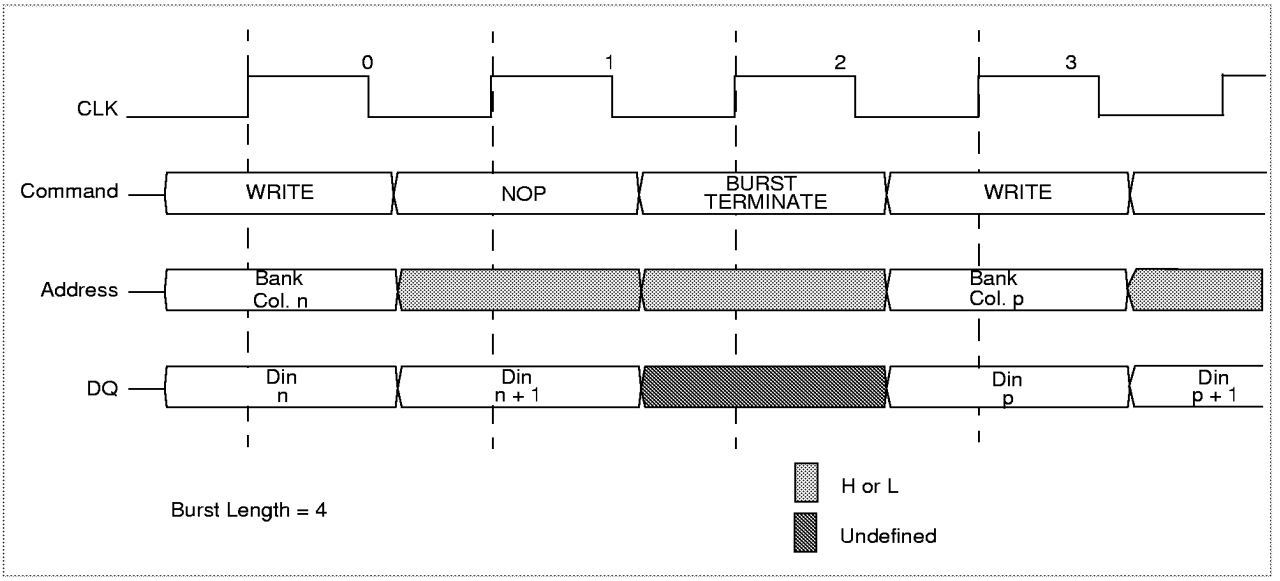


NOTE: Covers either a Writes to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW). Burst length = 2. Read LATENCY = 2 for illustration.

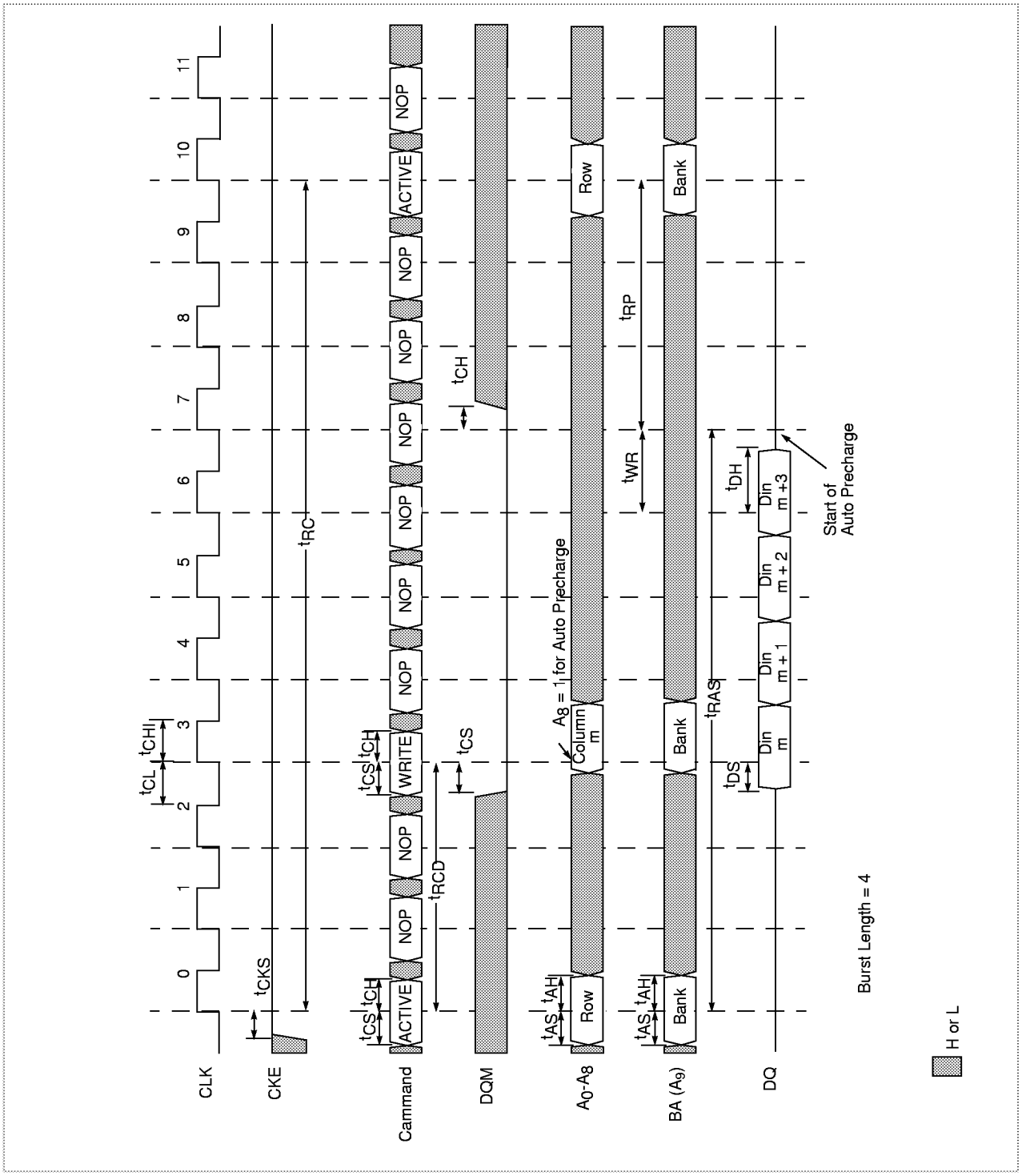
Write to Precharge



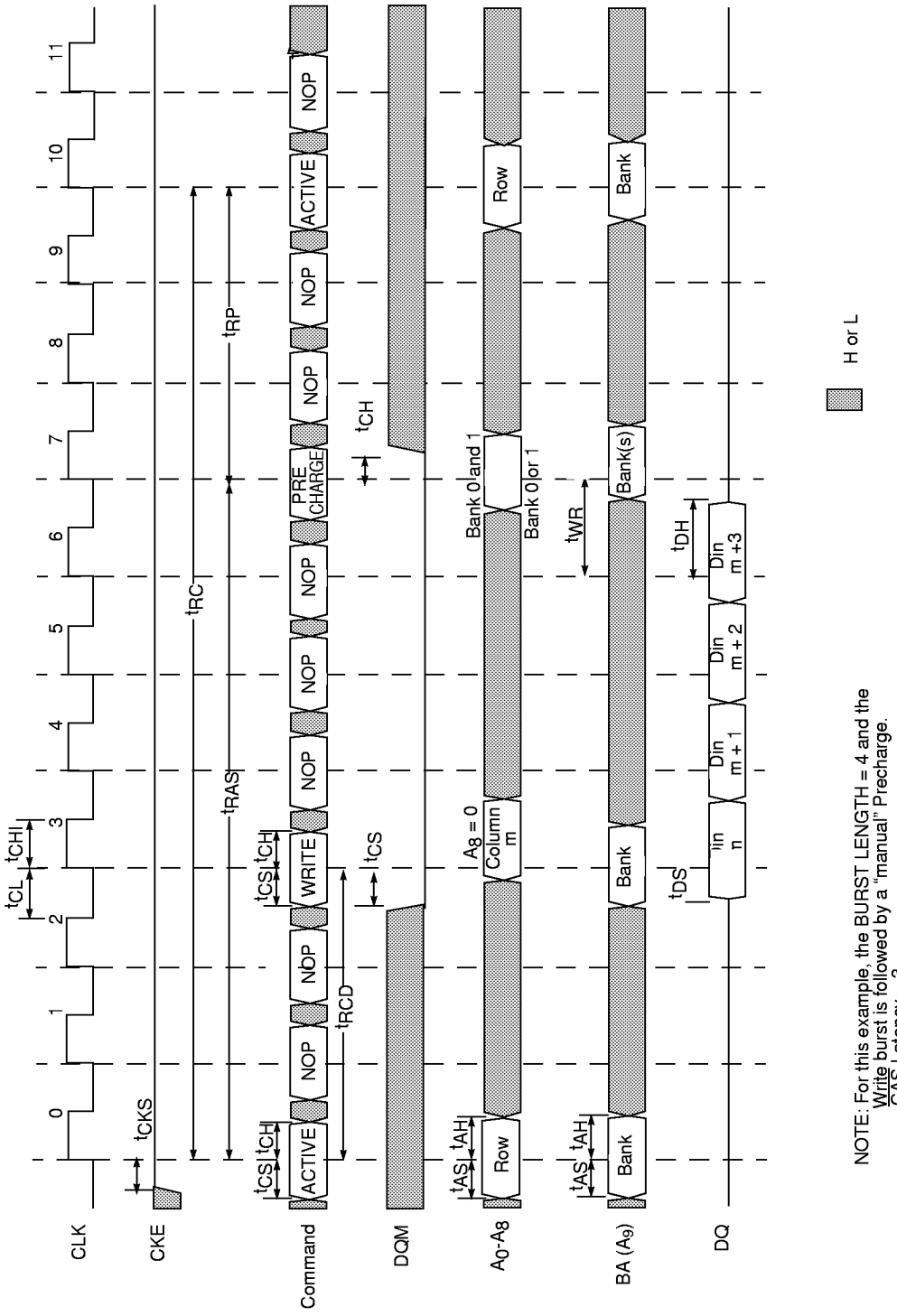
Terminating a Write Burst



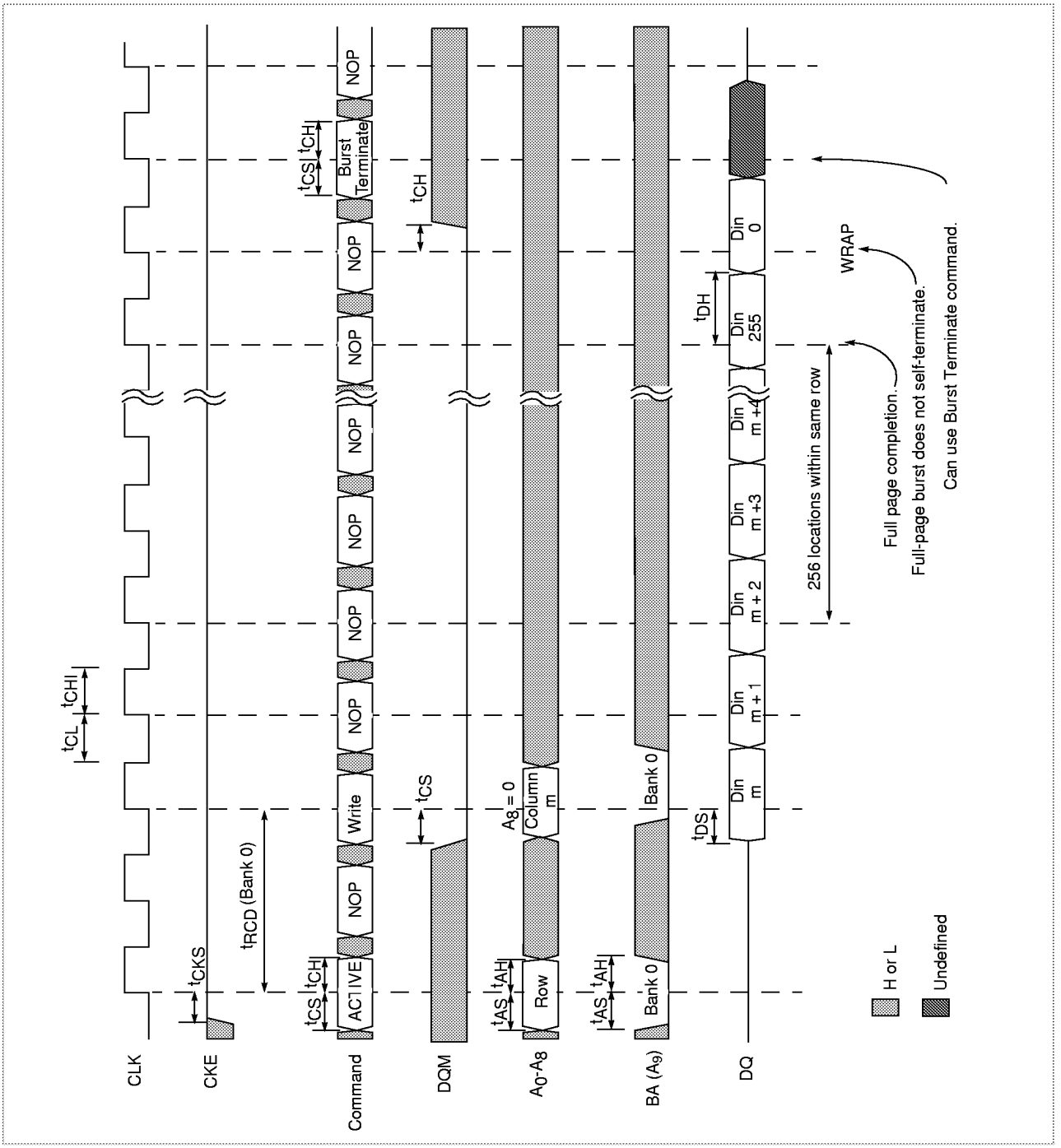
Write with Auto Precharge



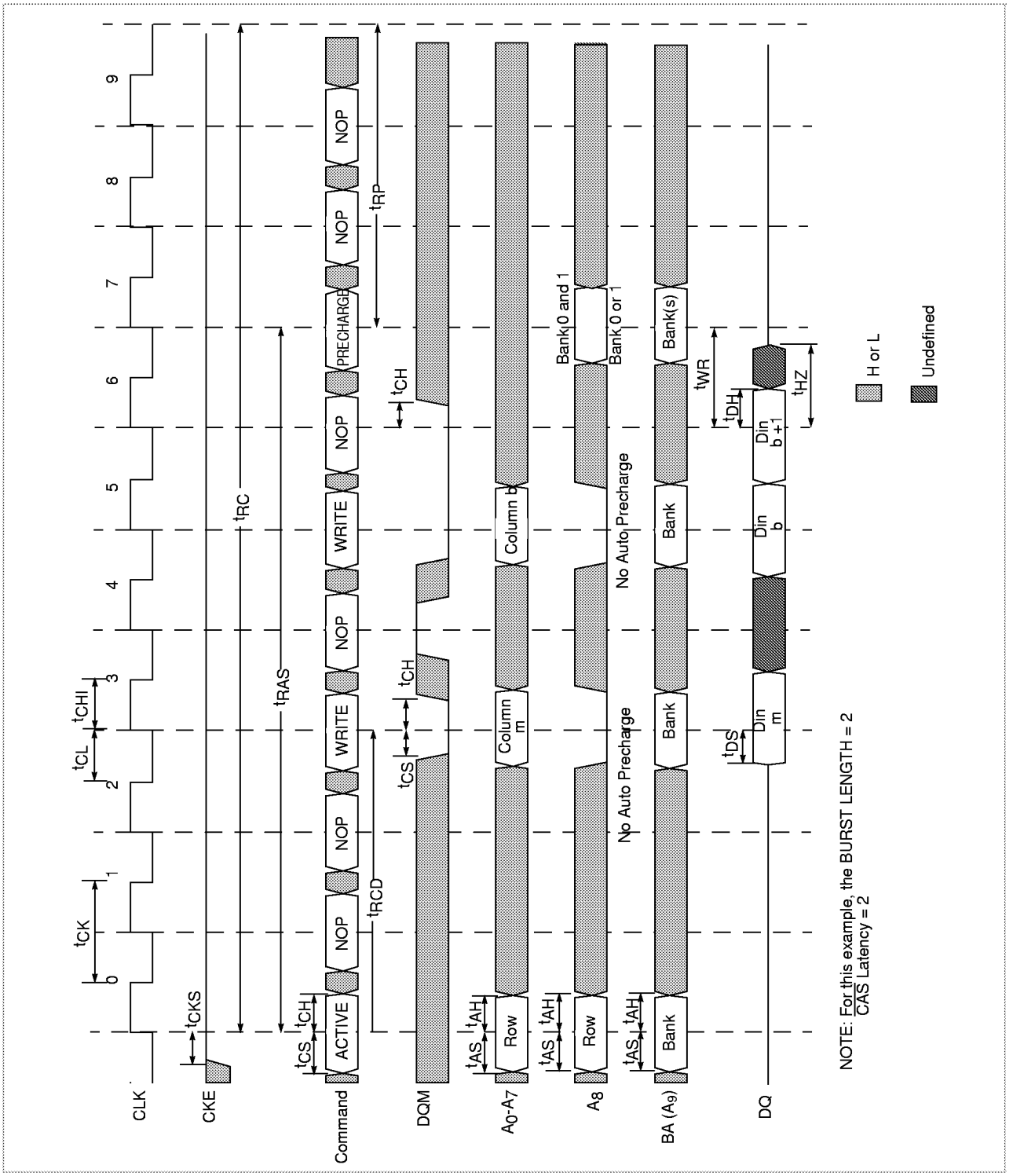
Write without Auto Precharge



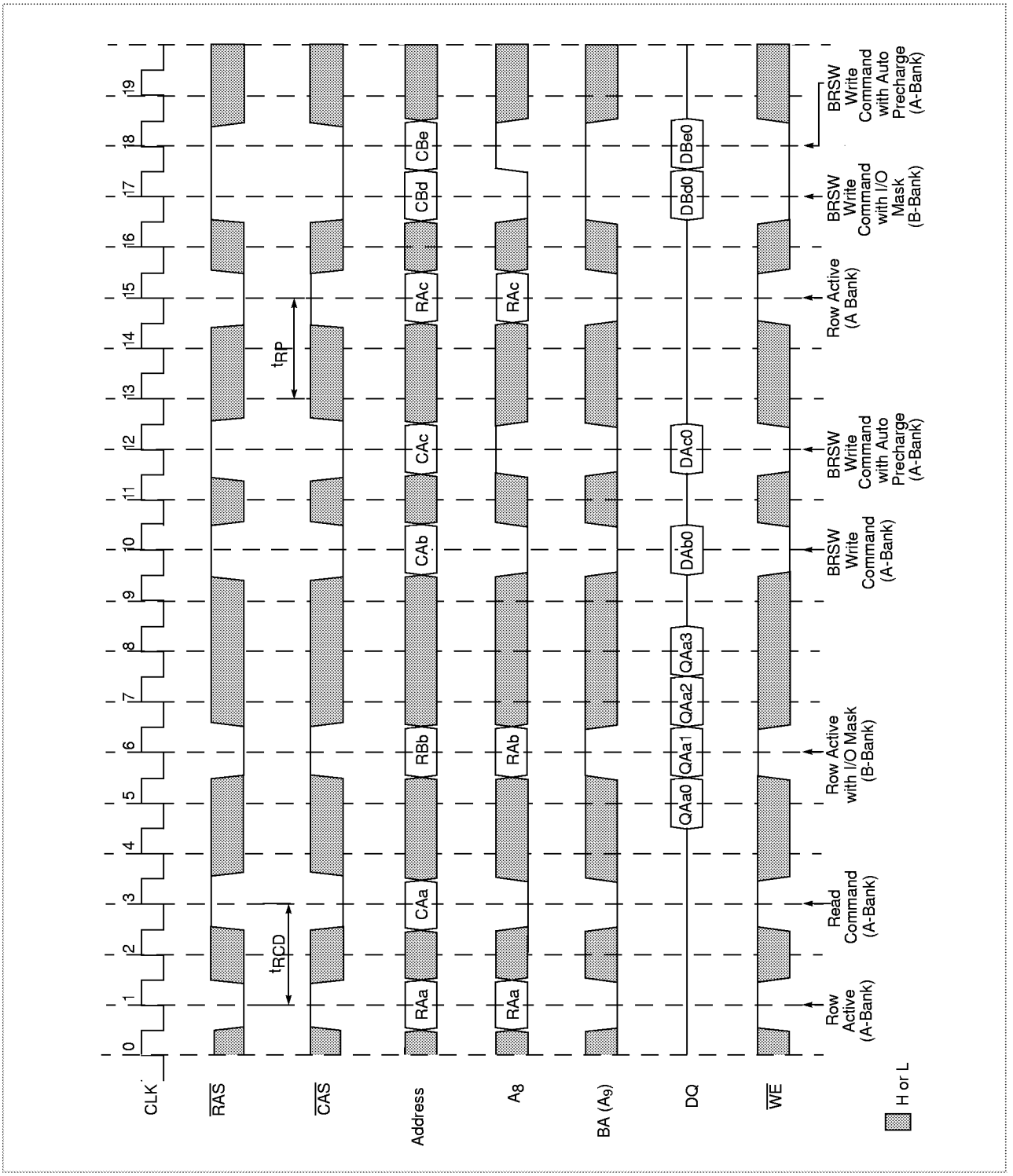
Write Full Page Burst



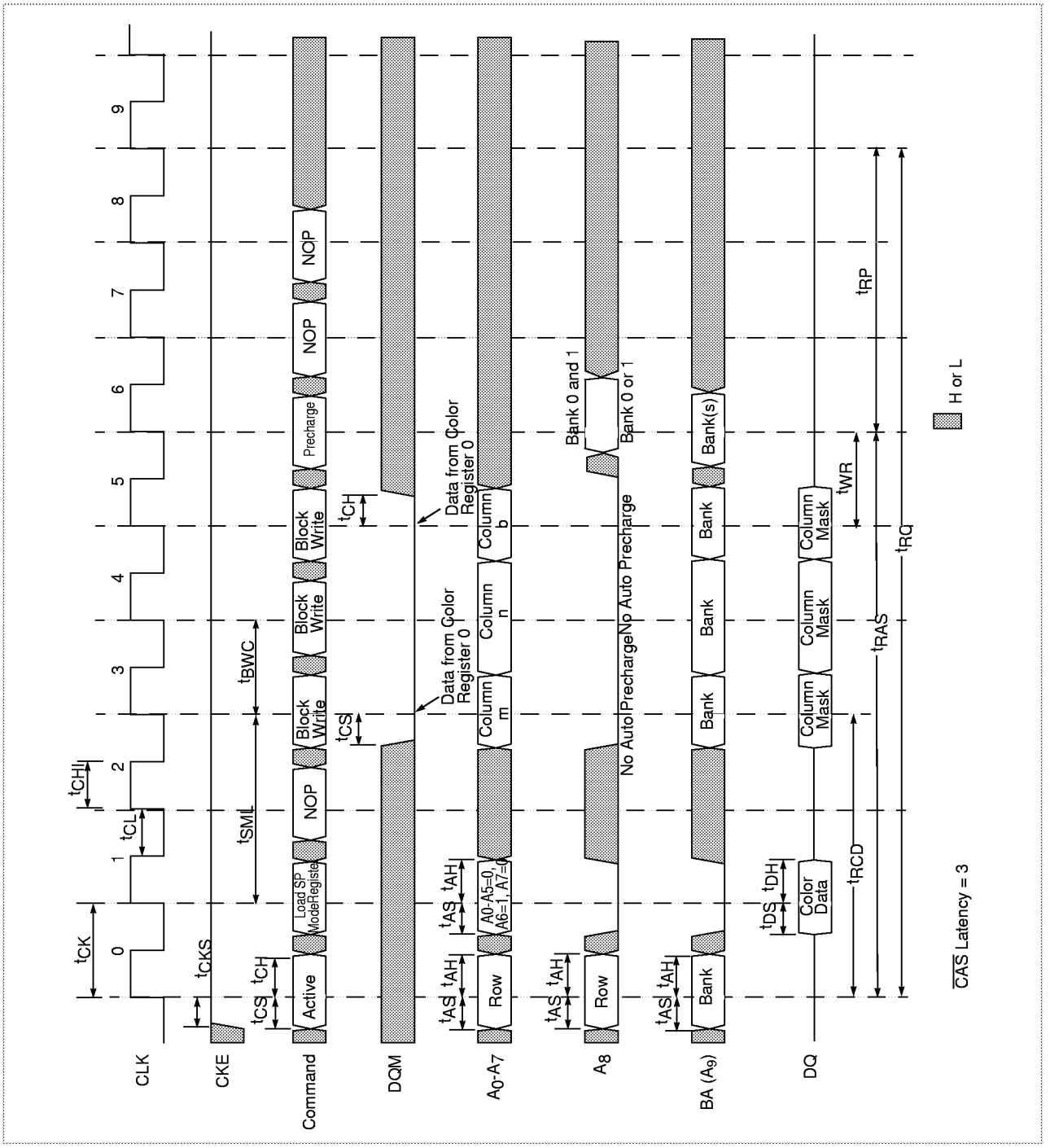
Write DQM Operation



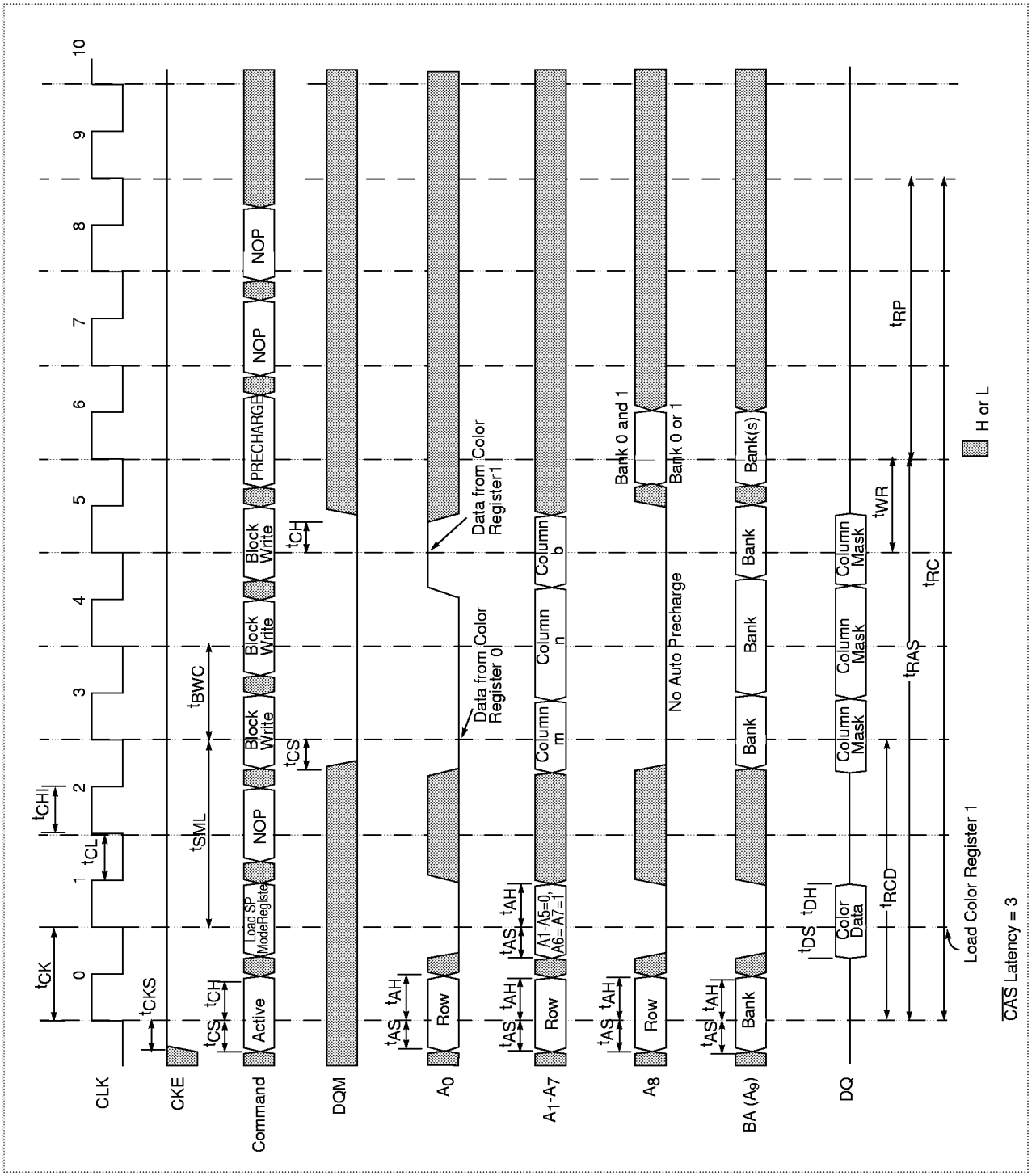
Burst Read Single Write Cycle (Burst Length = 4, CAS Latency = 2)



Block Write (1 Color Register)



Block Write (Multiple Color Registers)



Precharge Command

The Precharge command is used to deactivate the open row in a particular bank, or the open row in both banks. Whenever, a user wants to activate or open another row in the same bank, he must initiate the Precharge command. This process causes a significant latency known as Row Latency.

Logic Table for Precharge Command

Mnemonic	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	BA (A_9)	A_8	A_7-A_0
PRE	H	L	L	L	L	L	X	BS	L	X
PREAL	H	L	L	L	L	L	X	X	H	X

The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the Precharge command is issued. Once a bank has been precharged, it is in idle state and must be activated prior to any Read, Write, or Block Write commands being issued to the same bank.

Power Down

Logic Table for Power Down

Mnemonic	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	BA (A_9)	A_8	A_7-A_0
	n-1	n									
PDN (ENT)	H	L	X	X	X	X	X	X	X	X	X
PDN (EXT)	L	H	X	X	X	X	X	X	X	X	X

Power Down occurs when both banks are in idle state (precharged) and CKE is registered low. Entering Power Down deactivates the input and output buffers, excluding CKE for maximum power savings while in standby. In this mode the internal clock is suspended to save power. The device should be refreshed every 16ms to keep the DRAMs cells alive by initiating Auto Refresh command cycles. Note that in Power Down Mode no internal refresh operations are being performed..

The Power Down state is exited by taking CKE back high. CKE must go High, t_{CKS} before a positive clock edge, after meeting t_{CKH} from the previous clock edge. The first command after exiting Power Down will be registered on the clock edge following t_{CKS}. Exiting Power Down at clock edge n will put the device in the “all banks idle” state in time for clock edge n+1.

Self Refresh Mode (SREF)

The Self Refresh Mode is used to keep the device refreshed during its sleep mode for battery powered systems to conserve power.

SREF (ENT) command will put the device in Self Refresh mode and the information in the memory cells will be kept alive by refreshing the DRAM cells internally by initiating 1024 cycles every 64ms or 128ms or 256ms depending on the device used.

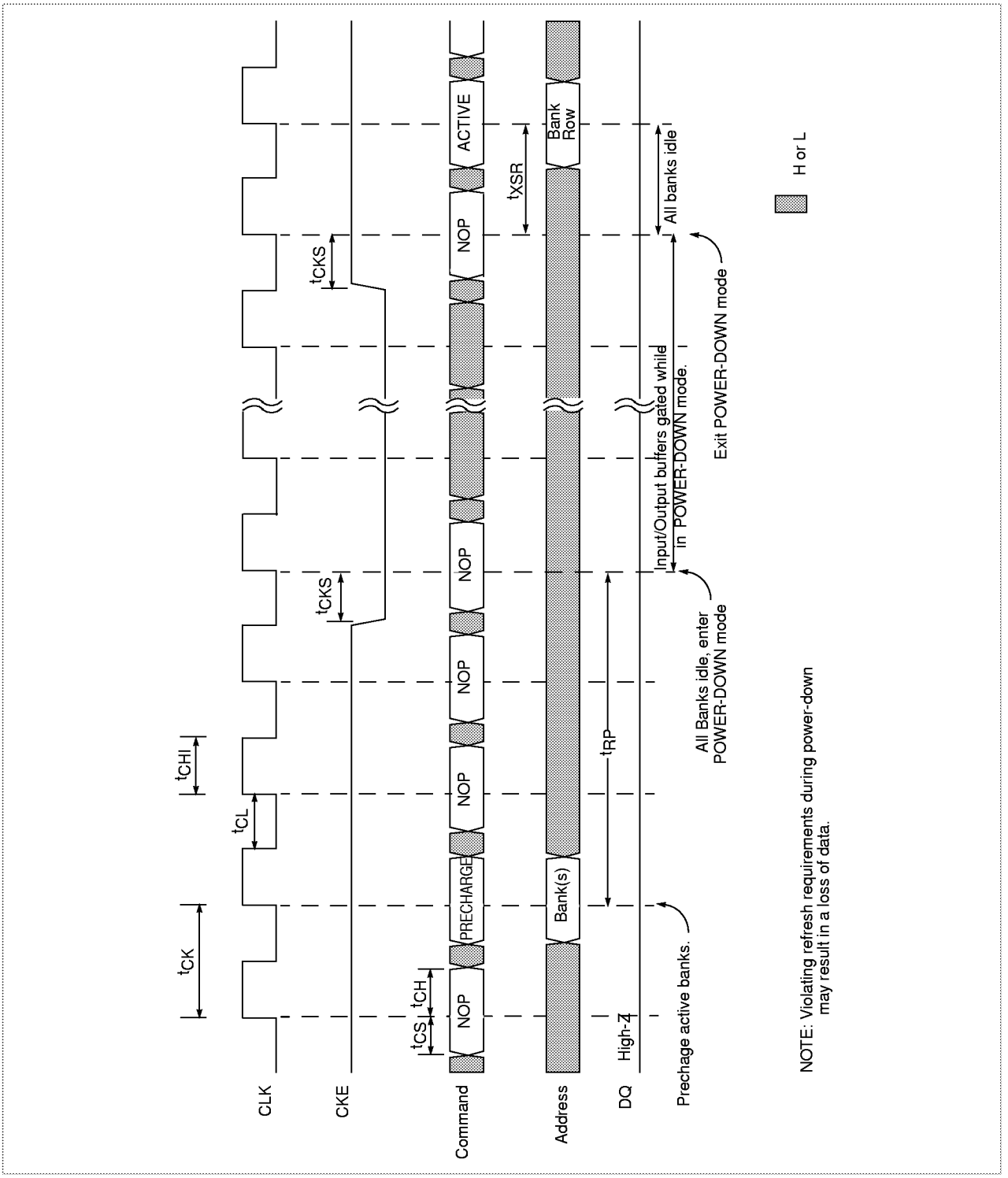
Exiting Self Refresh at clock edge n will put the device in the “all banks idle” state once t_{XSR} is met. NOP commands should be issued on any clock edges occurring during the t_{XSR} period.

Logic Table for Self Refresh

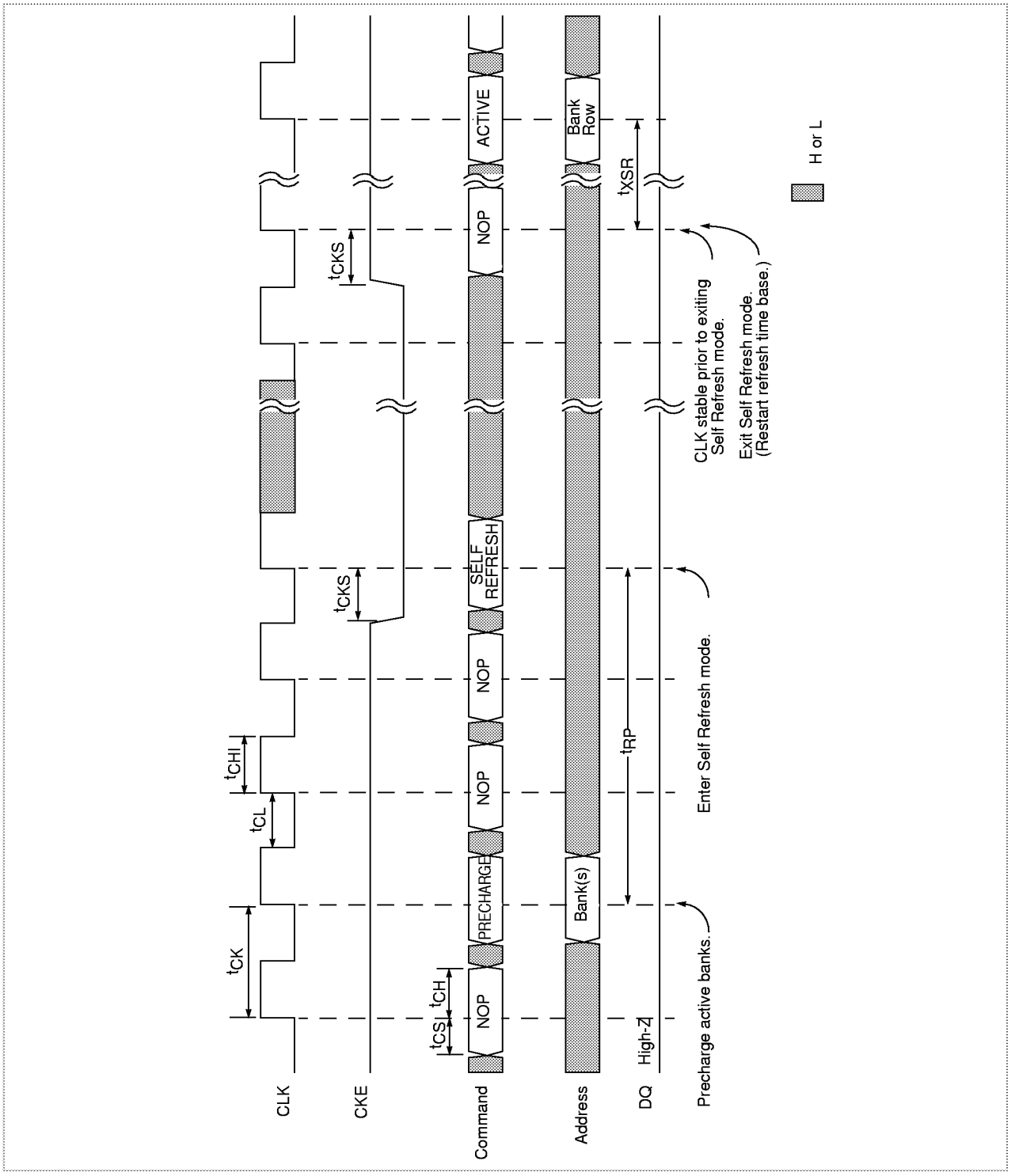
Mnemonic	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	BA (A_9)	A_8	A_7-A_0
	n-1	n									
SREF (ENT)	H	L	L	L	L	H	L	X	X	X	X
SREF (EXT)	L	H	H	X	X	X	X	X	X	X	X
	L	H	L	H	H	H	X	X	X	X	X

The following page shows the timing diagrams for the Power Down mode and the Self Refresh mode. Entry into these modes and exit from these modes are also illustrated.

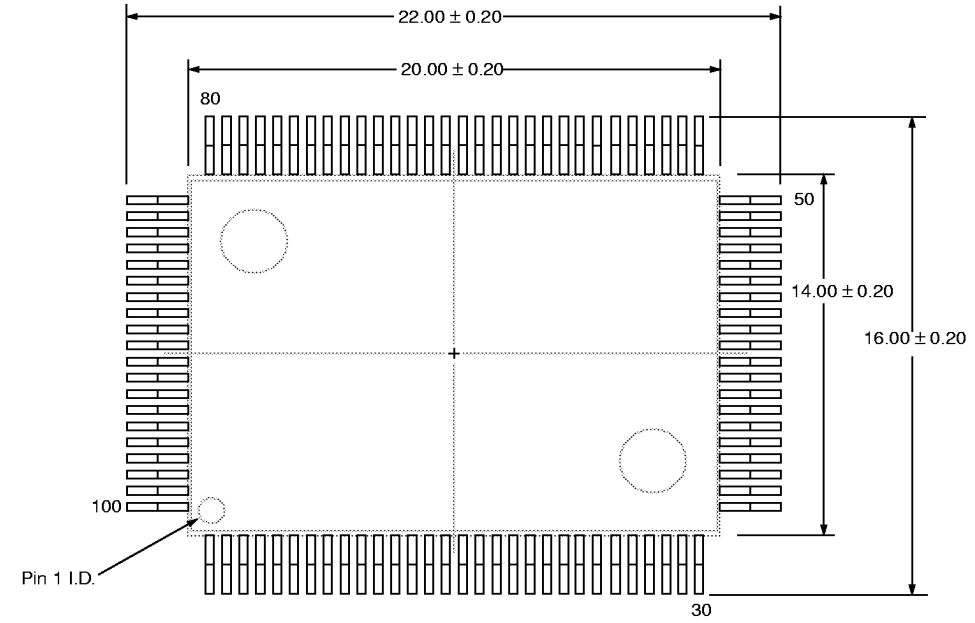
Power Down Mode

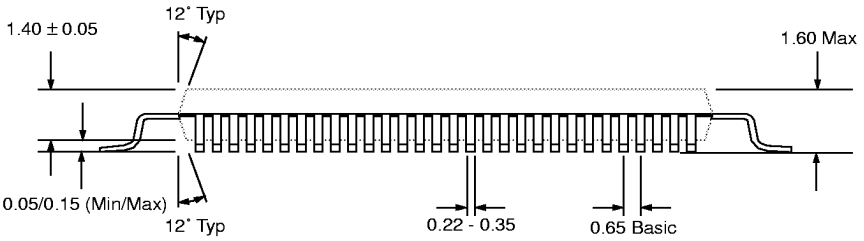


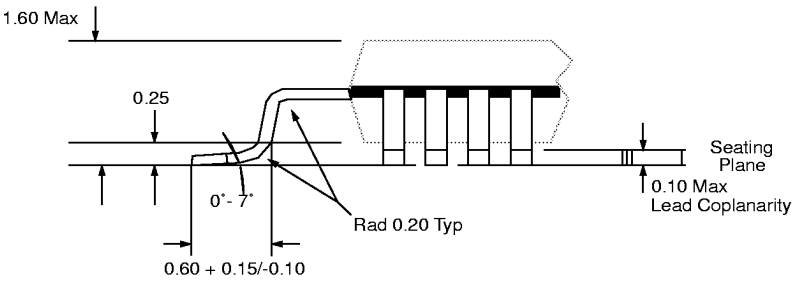
Self Refresh Mode



Package Diagram







All dimensions in Millimeters
Conforms to JEDEC MS-026/Variation BHA

Revision Log

Rev	Contents of Modification
7/95	Initial release.
1/96	Updates for databook.
9/96	Added 125 MHz specification: -8 part. Added Burst Read Single Write Cycle.
11/96	Updated minimum times in Timing Specifications table and maximum values in I_{CC} Specifications table. Changed -8 part to -7R5 part.
1/97	Assigned V_{REF} signal to pin #58. Added SSTL description after Commands section. Updated timing diagram of DQM Read operation. Changed T_{CKH} values in Timing Specifications table.
2/97	Corrected 133Mhz timing values. Corrected DQM timing and LSMR mode action. In Register Definition of Burst Type, changed “WT” to “BT” to match Mode Register Functions figure. Changed labeling of A_9 to BA to match JEDEC 8Mb nomenclature. Updated currents for -7R5 in I_{CC} Specifications table.