Features

- 200-Pin JEDEC Standard, Registered 8-Byte Dual In-line Memory Module
- 32M x 72 Synchronous DRAM DIMM
- Performance:

$\overline{CAS}$ Latency = 2*		-10	Units
f_{CK}	Clock Frequency	66	MHz
t_{CK2}	Clock Cycle	15	ns
t_{AC2}	Clock Access Time	11.3	ns
* SDRAM $\overline{CAS}$ latency = 2; DIMM $\overline{CAS}$ Latency = 3			

- Inputs and outputs are LVTTL (3.3V) compatible
- Single 3.3V to 3.6V Power Supply
- Single Pulsed $\overline{RAS}$ interface
- Fully Synchronous to positive Clock Edge
- Data Mask control
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge Commands
- Programmable Operation:
  - -SDRAM $\overline{CAS}$ Latency: 2
  - -Burst Type: Sequential or Interleave
  - -Burst Length: 2
  - -Operation: Burst Read and Write or Multiple Burst Read with Single Write
- Suspend Mode and Power Down Mode
- 12/10/2 Addressing (Row/Column/Bank)
- 4096 Refresh cycles distributed across 64ms
- Parallel Presence Detect
- Card size: 6.05" x 1.50" x 0.320"
- Gold contacts
- SDRAMs in TSOJ Type II, 2-High, Stacked Package

Description

IBM13Q32734BCA is a registered 200-pin Synchronous DRAM Dual In-line Memory Module (DIMM) which is organized as a 32Mx72 high-speed memory array. The DIMM uses eighteen x4 SDRAMs in 400mil TSOJ II stacked packages. The DIMM achieves high speed data transfer rates of up to 66MHz by employing a prefetch/pipeline hybrid architecture that supports the JEDEC 1N rule while allowing very low burst power.

The DIMM is intended to comply with all non-optional JEDEC standards set for the 200-pin registered SDRAM DIMMs.

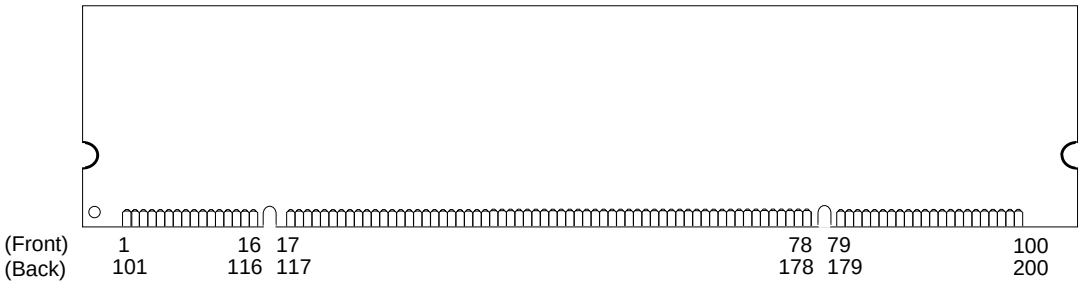
All control and address signals are synchronized with the positive edge of an externally supplied clock. They are latched in an on-DIMM pipeline register and presented to the SDRAMs on the following clock.

Prior to any Access operation, the $\overline{CAS}$ latency, burst type, burst length, and burst operation type must be programmed into the DIMM by address inputs A0-A13 using the Mode Register Set cycle.

The DIMM uses parallel presence detects implemented according to the JEDEC standard.

All IBM 200-pin DIMMs provide a high performance, flexible 8-byte interface in a 6.05” long high-performance footprint. Related products include both EDO DRAM and SDRAM unbuffered DIMMs in both non-parity x64 and ECC-Optimized x72 configurations in the 168 pin form factor.

Card Outline



Pin Description

CK0	Clock Input (Buffered through PLL)	DQM	Data Mask (Registered)
CKE0	Clock Enables (Registered)	V_{DD}	Power (3.3V)
$\overline{RAS}$	Row Address Strobe (Registered)	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe (Registered)	NC	No Connect
$\overline{WE}$	Write Enable (Registered)	PD1 - PD8	Presence Detect (Buffered)
$\overline{S}0$, $\overline{S}1$	Chip Selects (Registered)	PDE	Presence Detect Enable
A0 - A9, A11	Address Inputs (Registered)	ID1 - ID3	ID Bits
A10/AP	Address Input/Auto Precharge (Reg)	A12/BS1, A13/BS0	SDRAM Bank Selects (Registered)
DQ0 - DQ71	Data Input/Output	IN, OUT	Physical Detect (Direct short)

Pinout x72 DIMM

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{DD}	101	NC	26	V_{DD}	126	DQ53	51	V_{SS}	151	CK0	76	DQ16	176	V_{DD}
2	NC	102	NC	27	DQ51	127	DQ52	52	$\overline{RAS}$	152	V_{DD}	77	V_{SS}	177	NC
3	NC	103	V_{SS}	28	DQ50	128	V_{DD}	53	V_{SS}	153	$\overline{S}1$	78	NC	178	V_{SS}
4	IN	104	NC	29	V_{SS}	129	DQ47	54	NC	154	$\overline{S}0$	79	NC	179	V_{SS}
5	OUT	105	NC	30	DQ49	130	DQ46	55	A13/BS0	155	V_{SS}	80	V_{DD}	180	NC
6	ID1	106	NC	31	DQ48	131	V_{SS}	56	V_{DD}	156	A12/BS1	81	DQ15	181	NC
7	ID2	107	ID3	32	V_{DD}	132	DQ45	57	A0	157	A10/AP	82	DQ14	182	V_{DD}
8	V_{SS}	108	DQ71	33	DQ43	133	DQ44	58	A1	158	V_{DD}	83	V_{SS}	183	DQ11
9	DQ67	109	DQ70	34	DQ42	134	V_{DD}	59	V_{SS}	159	A2	84	DQ13	184	DQ10
10	DQ66	110	V_{SS}	35	V_{SS}	135	DQ39	60	DQ35	160	A3	85	DQ12	185	V_{SS}
11	V_{DD}	111	DQ69	36	DQ41	136	DQ38	61	DQ34	161	V_{SS}	86	V_{DD}	186	DQ9
12	DQ65	112	DQ68	37	DQ40	137	V_{SS}	62	V_{DD}	162	DQ31	87	DQ7	187	DQ8
13	DQ64	113	V_{DD}	38	V_{DD}	138	DQ37	63	DQ33	163	DQ30	88	DQ6	188	V_{DD}
14	V_{SS}	114	NC	39	A4	139	DQ36	64	DQ32	164	V_{DD}	89	V_{SS}	189	DQ3
15	DQ63	115	V_{SS}	40	A5	140	V_{DD}	65	V_{SS}	165	DQ29	90	DQ5	190	DQ2
16	DQ62	116	NC	41	V_{SS}	141	A6	66	DQ27	166	DQ28	91	DQ4	191	V_{SS}
17	NC	117	DQ59	42	A8	142	A7	67	DQ26	167	V_{SS}	92	V_{DD}	192	DQ1
18	DQ61	118	DQ58	43	A9	143	V_{SS}	68	V_{DD}	168	DQ23	93	$\overline{PDE}$	193	DQ0
19	DQ60	119	V_{SS}	44	V_{DD}	144	A11	69	DQ25	169	DQ22	94	PD1	194	PD5
20	V_{DD}	120	DQ57	45	CKE1	145	NC	70	DQ24	170	V_{DD}	95	PD2	195	PD6
21	NC	121	DQ56	46	CKE0	146	V_{DD}	71	V_{SS}	171	DQ21	96	PD3	196	PD7
22	NC	122	V_{DD}	47	V_{SS}	147	DQM	72	DQ19	172	DQ20	97	PD4	197	PD8
23	V_{SS}	123	DQ55	48	$\overline{CAS}$	148	$\overline{WE}$	73	DQ18	173	V_{SS}	98	SCL	198	V_{DD}
24	NC	124	DQ54	49	NC	149	V_{SS}	74	V_{DD}	174	NC	99	NC	199	NC
25	NC	125	V_{SS}	50	V_{DD}	150	NC	75	DQ17	175	NC	100	V_{SS}	200	NC

Ordering Information

Part Number	Organization	Clock Cycle	Leads	Dimension	Power
IBM13Q32734BCA-10Y	32Mx72	66MHz	Gold	6.05" x 1.50" x 0.320"	3.3V

Input/Output Functional Description

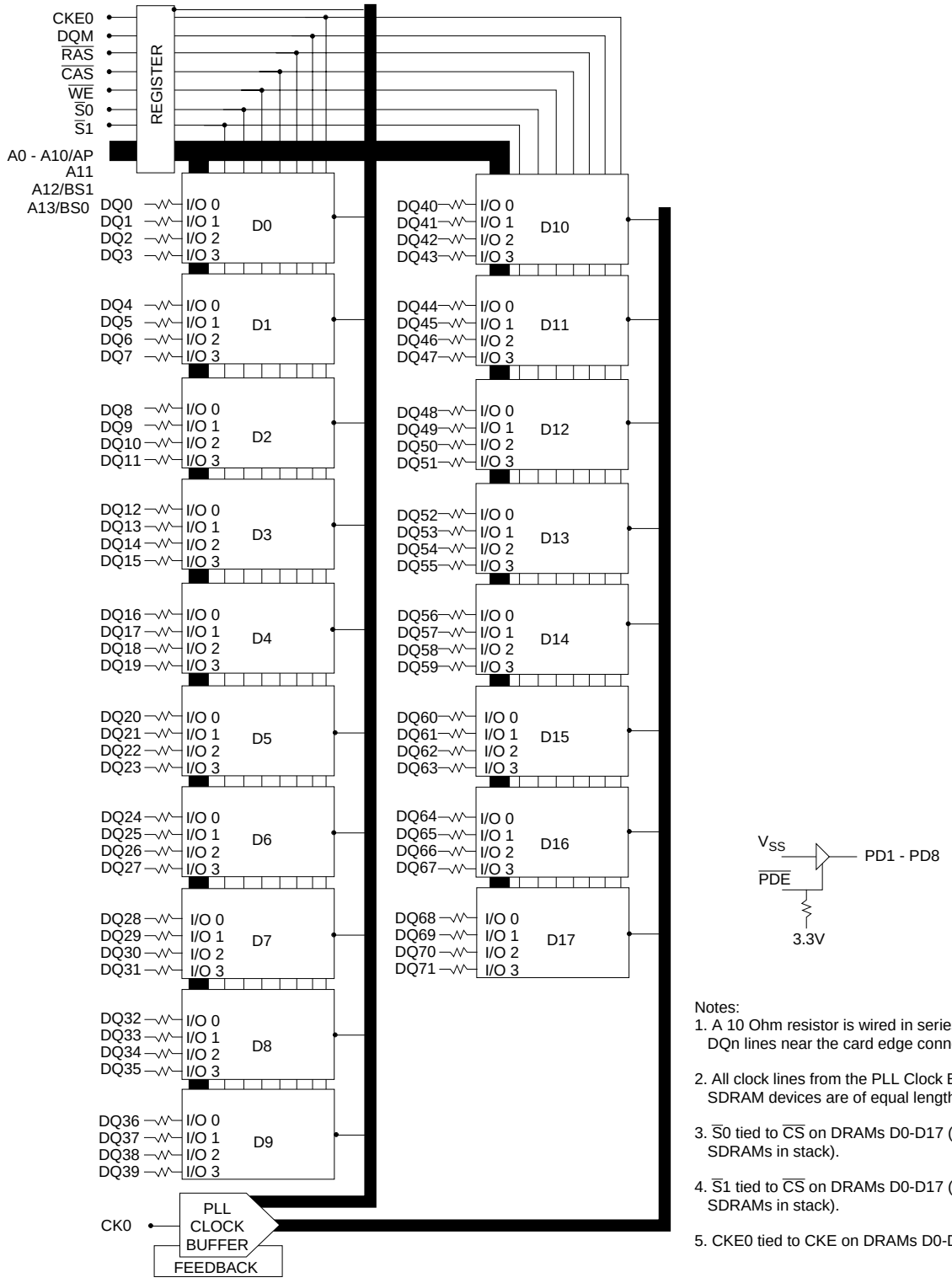
Symbol	Type	Signal	Polarity	Function
CK0	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE0	Input	Level	Active High	Activates the CK0 signal when high and deactivates the CK0 signal when low. By deactivating the clock, CKE0 low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{S}0$, $\overline{S}1$	Input	Pulse	Active Low	$\overline{S}0$, $\overline{S}1$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
A12/BS1 A13/BS0	Input	Level	—	Select which SDRAM bank is to be active (Bank 0 - Bank3)
A0 - A9, A11 A10/AP A12/BS1 A13/BS0	Input	Level	—	During a Bank Activate command cycle, A0-A10/AP and A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A8 defines the column address (CA0-CA8) when sampled at the rising clock edge. In addition to the column address, A10/AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If A10/AP is high, autoprecharge is selected and BS0,BS1 defines the bank to be precharged. If A10/AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BS0,BS1 to control which bank(s) to precharge. If A10/AP is high, all banks will be precharged regardless of the state of BS. If A10/AP is low, then BS0,BS1 is used to define which bank to precharge.
DQ0 - DQ71	Input Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAM DIMMs.
DQM	Input	Pulse	Mask Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of three clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of one and operates as a word mask by allowing input data to be written if it is low but blocks the Write operation if DQM is high.
V_{DD}, V_{SS}	Supply			Power and ground for the module.

Presence Detect

Pin	Value	Notes
PD1	0	1
PD2	0	1
PD3	1	1
PD4	0	1
PD5	1	1
PD6	0	1
PD7	1	1
PD8	1	1
ID1	1	2
ID2	0	2
ID3	0	2

1. 0 = driven to V_{OL}, 1 = open
2. 0 = ground, 1 = open

Block Diagram: Buffered 32Mx72 ECC SDRAM DIMM



Notes:
1. A 10 Ohm resistor is wired in series with all DQn lines near the card edge connector.
2. All clock lines from the PLL Clock Buffer to the SDRAM devices are of equal length.
3. $\overline{S0}$ tied to $\overline{CS}$ on DRAMs D0-D17 (lower SDRAMs in stack).
4. $\overline{S1}$ tied to $\overline{CS}$ on DRAMs D0-D17 (upper SDRAMs in stack).
5. CKE0 tied to CKE on DRAMs D0-D17

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Power Supply Voltage	-0.3 to +4.6	V	1
V_{IN}	Input Voltage	-0.3 to +4.6	V	1
V_{OUT}	Output Voltage	-0.3 to +4.6	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	16	W	1,2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power is calcuated assuming both physical banks on the DIMM are in Auto Refresh mode.

Recommended DC Operating Conditions (T_A= 0 to 70°C)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	3.3	—	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 0.3	V	1
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1

1. All voltages referenced to V_{SS} and VSSQ.

Capacitance (T_A= 25°C, f=1MHz, V_{DD}= 3.3V to 3.6V)

Symbol	Parameter	Max.	Units
C_{I1}	Input Capacitance (A0 - A9, A10/AP, A11)	15	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM, $\overline{PDE}$)	25	pF
C_{I3}	Input Capacitance ($\overline{S}$0, $\overline{S}$1, CKE0)	40	pF
C_{I4}	Input Capacitance (CK0)	10	pF
C_{I01}	Input/Output Capacitance (DQ0 - DQ71)	25	pF
C_{01}	Output Capacitance (PD1- PD8)	12	pF

Output Characteristics (T_A= 0 to +70°C, V_{DD}= 3.3V to 3.6V)

Symbol	Parameter	Min.	Max.	Units
$I_{I(L)}$	Input Leakage Current, any input (0.0V ≤ V_{IN} ≤ 3.6V), All Other Pins Not Under Test = 0V	-20	+20	µA
$I_{O(L)}$	Output Leakage Current (DQ) (D_{OUT} is disabled, 0.0V ≤ V_{OUT} ≤ 3.6V)	-2	+2	µA
V_{OH}	Output Level (TTL) Output "H" Level Voltage (I_{OUT} = -2.0mA)	2.4	V_{DD}	V
V_{OL}	Output Level (TTL) Output "L" Level Voltage (I_{OUT} = +2.0mA)	0.0	0.4	V
$I_{O(L)}$	Output Leakage Current (PD1 - PD8)	-10	+10	µA

Operating, Standby, and Refresh Currents (T_A = 0 to +70°C, V_{DD} = 3.3V to 3.6V)

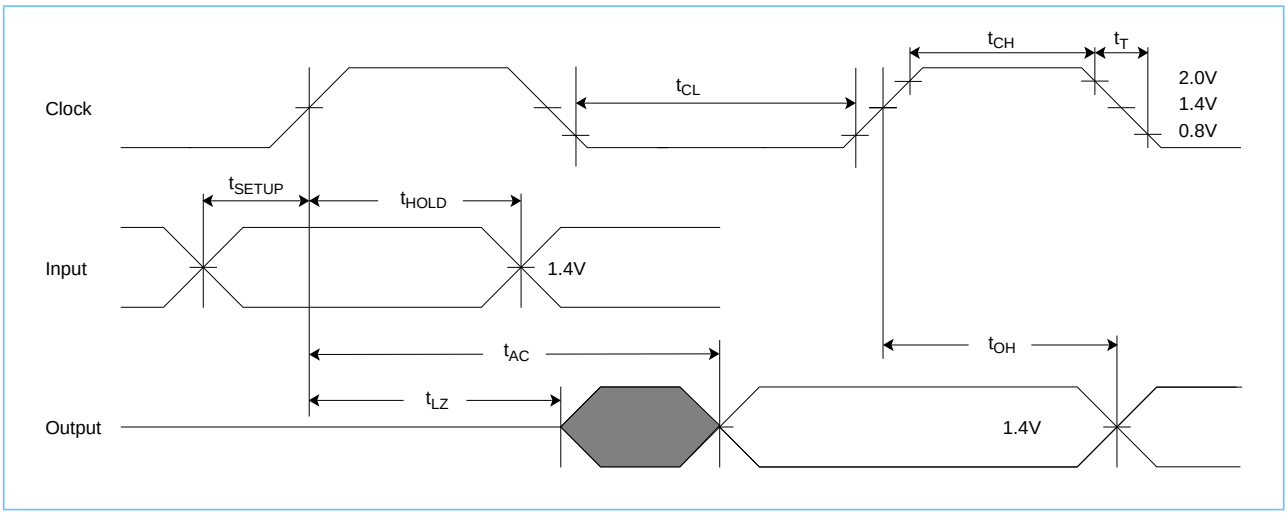
Parameter	Symbol	Test Condition	Value	Units	Notes
Operating Current	I_{CC1}	1 bank operation t_{RC} = t_{RC}(min), t_{CK} = min Active-Precharge command cycling without burst operation	2026	mA	1, 3, 4
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CK} = min, $\overline{CS}$ =V_{IH}(min)	532	mA	2
	I_{CC2PS}	CKE ≤ V_{IL}(max), t_{CK} = Infinity, $\overline{CS}$ =V_{IH}(min)	61	mA	2
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{CS}$ =V_{IH} (min)	1396	mA	2, 5
	I_{CC2NS}	CKE ≥ V_{IH}(min), t_{CK} = Infinity,	241	mA	2, 6
No Operating Current (Active state: 4 bank)	I_{CC3N}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{CS}$ =V_{IH} (min)	1576	mA	2, 5
	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CK} = min,	604	mA	2, 7
Operating Current (Burst Mode)	I_{CC4}	t_{CK} = min, Read/ Write command cycling, Multiple banks active, gapless data,BL=4	2656	mA	1, 4, 8
Auto (CBR) Refresh Current	I_{CC5}	t_{CK} = min, t_{RC} = t_{RC}(min) CBR command cycling	4456	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	61	mA	2, 8

1. The specified values are for one DIMM bank in the specified mode, and the other DIMM bank in Active Standby (I_{CC3N}).
2. The specified values are for both DIMM banks operating in the specified mode.
3. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}. Input signals are changed up to three times during t_{RC}(min).
4. The specified values are obtained with the output open.
5. Input signals are changed once during three clock cycles.
6. Input signals are stable.
7. Active Standby current will be higher if clock suspend is entered during a Burst Read cycle (add 1mA per DQ).
8. Input signals are changed once during $t_{CK(min)}$.

AC Characteristics (T_A= 0 to +70°C, V_{DD}= 3.3V to 3.6V)

1. An initial pause of 200µs is required after power-up, then a Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before or after the Mode Register Set operation can begin.
2. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with the timing referenced to the 1.40V crossover point.
3. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
4. AC measurements assume t_T=1ns.
5. In addition to meeting the transition rate specification, the clock and CKE0 must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

AC Characteristics Diagram



Clock and Clock Enable Parameters

Symbol	Parameter	Value		Units	Notes
		Min.	Max.		
t_{CK2}	Clock Cycle Time	15	66MHz	ns	
t_{AC2}	Clock Access Time	—	11.3	ns	1, 2
t_{CH}	Clock High Pulse Width	6.0	—	ns	
t_{CL}	Clock Low Pulse Width	6.0	—	ns	
t_{CKS}	Clock Enable Setup Time	2.3	—	ns	
t_{CKH}	Clock Enable Hold Time	1.3	—	ns	
t_{CKSP}	CKE0 Setup Time (Power down mode)	2.3	—	ns	
t_T	Transition Time (Rise and Fall)	1.4	10	ns	
t_{STAB}	PLL Stabilization Time	1	—	ms	

1. $\overline{CAS}$ latency defined at SDRAMs; DIMM actually has $\overline{CAS}$ latency of 3.
2. 50pF Load.

Common Parameters

Symbol	Parameter	Value		Units
		Min.	Max.	
t_{S0}	Command Setup Time	2.3	—	ns
t_{CH}	Command Hold Time	1.3	—	ns
t_{AS}	Address and Bank Select Setup Time	2.3	—	ns
t_{AH}	Address and Bank Select Hold Time	1.3	—	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	30	—	ns
t_{RC}	Bank Cycle Time	90	—	ns
t_{RAS}	Active Command Period	60	100000	ns
t_{RP}	Precharge Time	30	—	ns
t_{RRD}	Bank to Bank Delay Time	20	—	ns
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	—	CLK

Mode Register Set Cycle

Symbol	Parameter	Value		Units	Notes
		Min.	Max.		
t_{RSC}	Mode Register Set Cycle Time	20	—	ns	1

1. These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Read Cycle

Symbol	Parameter	Value		Units	Notes
		Min.	Max.		
t_{OH}	Data Out Hold Time	3.3	—	ns	
t_{LZ}	Data Out to Low Impedance Time	0.3	—	ns	
t_{HZ2}	Data Out to High Impedance Time	3.3	10.8	ns	1
t_{DQZ}	DQM Data Out Disable Latency	3	—	CLK	

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

Refresh Cycle

Symbol	Parameter	Value		Units	Notes
		Min.	Max.		
t_{REF}	Refresh Period	—	64	ms	1
t_{SREX}	Self Refresh Exit Time	10	—	ns	

1. 4096 cycles.

Write Cycle

Symbol	Parameter	Value		Units
		Min.	Max.	
t_{DS}	Data In Setup Time	3.3	—	ns
t_{DH}	Data In Hold Time	2.3	—	ns
t_{DPL2}	Data input to Precharge	1	—	CLK
t_{DQW}	DQM Write Mask Latency	1	—	CLK

Clock Frequency and Latency

Symbol	Parameter	Value	Units	Notes
f_{CK}	Clock Frequency	66.667	MHz	
t_{CK}	Clock Cycle Time	15	ns	
t_{AA}	$\overline{CAS}$ Latency	3	t_{CK}	1
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	2	t_{CK}	
t_{RC}	Bank Cycle Time	6	t_{CK}	
t_{RAS}	Minimum Bank Active Time	4	t_{CK}	
t_{RP}	Precharge Time	2	t_{CK}	
t_{DPL}	Data In to Precharge	1	t_{CK}	
t_{DAL}	Data In to Active/Refresh	3	t_{CK}	
t_{RRD}	Bank to Bank Delay Time	2	t_{CK}	
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	t_{CK}	
t_{WL}	Write Latency	1	t_{CK}	
t_{DQW}	DQM Write Mask Latency	1	t_{CK}	
t_{DQZ}	DQM Data Disable Latency	3	t_{CK}	
t_{CSL}	Clock Suspend Latency	1	t_{CK}	

1. SDRAMs have t_{AA}=2, but on-board DIMM register adds one clock cycle

Presence Detect Read Cycle

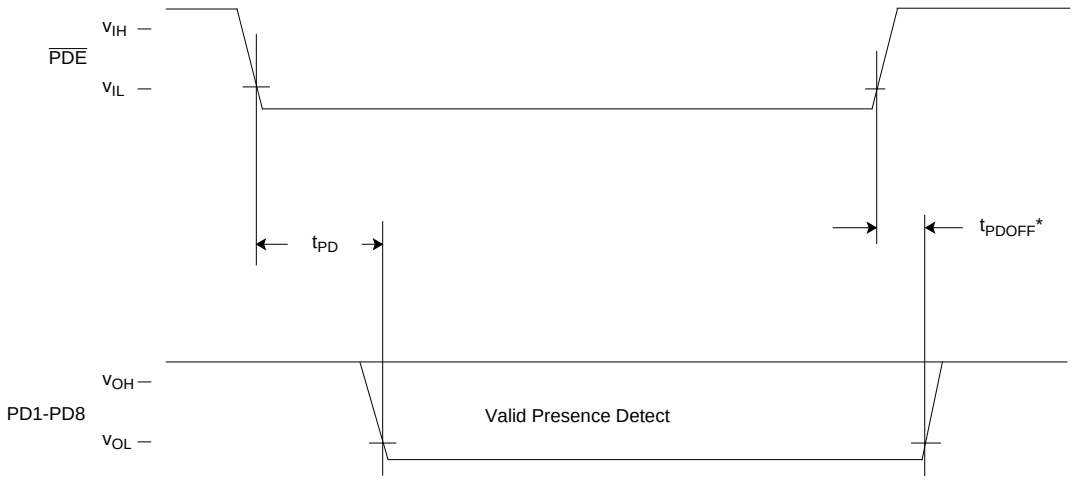
Symbol	Parameter	Value		Unit	Notes
		Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Functional Description and Timing Diagram

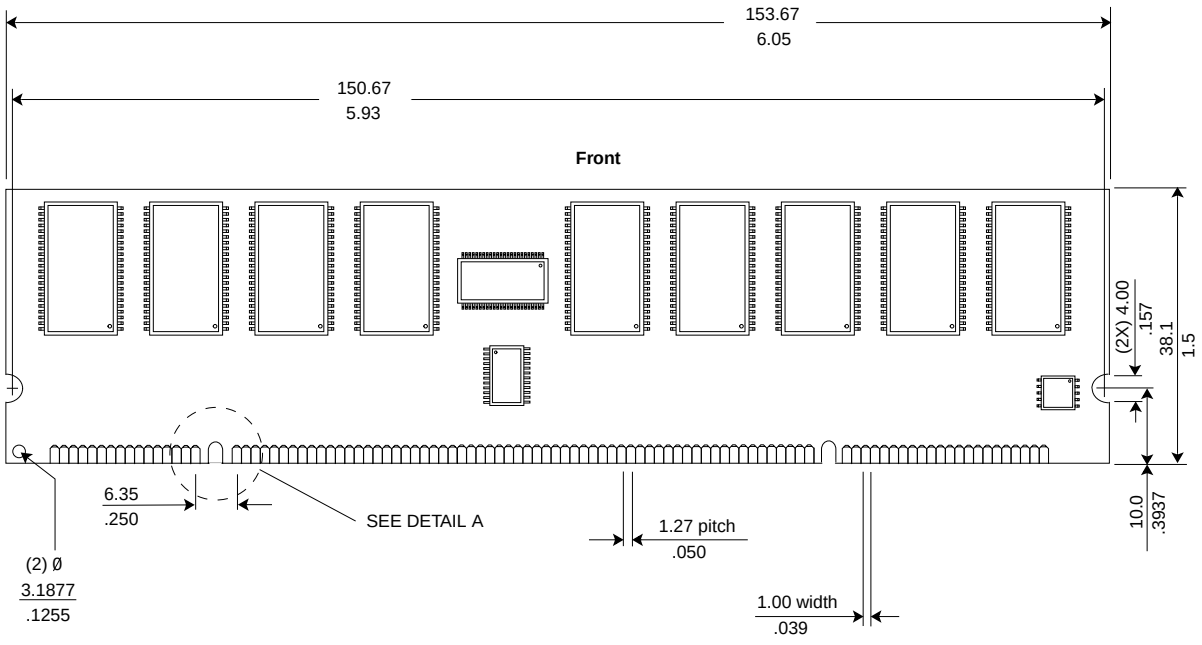
Refer to IBM 200-pin SDRAM Registered DIMM Functional Description and Timing Diagram (Document 04K8917.C75644C, for SDRAM operation).

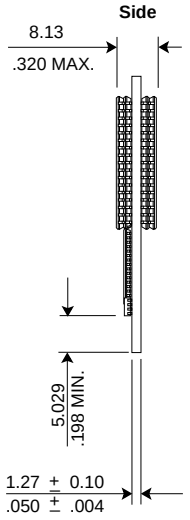
Presence Detect Read Cycle

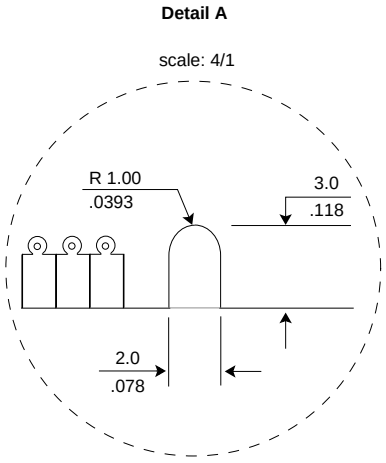


*PD pins must be pulled high at next level of assembly

Layout Drawing (200 Pin DIMM)







Note: All dimensions are typical unless otherwise stated.

Millimeters
Inches

Revision Log

Revision	Contents Of Modification
6/99	Initial release.
6/18/99	Updated notch dimensions line in layout drawing.

For more information contact your IBM Microelectronics sales representative or
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IBM Microelectronics manufacturing is ISO 9000 compliant.