

# NL74VCXH16373

## Low-Voltage 1.8/2.5/3.3V 16-Bit Transparent Latch With 3.6V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The NL74VCXH16373 is an advanced performance, non-inverting 16-bit transparent latch. It is designed for very high-speed, very low-power operation in 1.8V, 2.5V or 3.3V systems. The VCX16373 is byte controlled, with each byte functioning identically, but independently. Each byte has separate Output Enable and Latch Enable inputs. These control pins can be tied together for full 16-bit operation.

When operating at 2.5V (or 1.8V) the part is designed to tolerate voltages it may encounter on either inputs or outputs when interfacing to 3.3V busses. It is guaranteed to be over-voltage tolerant to 3.6V.

The NL74VCXH16373 contains 16 D-type latches with 3-state 3.6V-tolerant outputs. When the Latch Enable (LEn) inputs are HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, (a latch output will change state each time its D input changes). When LE is LOW, the latch stores the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state outputs are controlled by the Output Enable ( $\overline{OE_n}$ ) inputs. When  $\overline{OE}$  is LOW, the outputs are enabled. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches. The data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating inputs at a valid logic state.

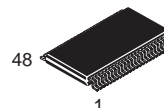
- Designed for Low Voltage Operation:  $V_{CC} = 1.65\text{--}3.6\text{V}$
- 3.6V Tolerant Inputs and Outputs
- High Speed Operation: 3.0ns max for 3.0 to 3.6V  
3.9ns max for 2.3 to 2.7V  
6.8ns max for 1.65 to 1.95V
- Static Drive:  $\pm 24\text{mA}$  Drive at 3.0V  
 $\pm 18\text{mA}$  Drive at 2.3V  
 $\pm 6\text{mA}$  Drive at 1.65V
- Supports Live Insertion and Withdrawal
- Includes Active Bushold to Hold Unused or Floating Inputs at a Valid Logic State
- I<sub>OFF</sub> Specification Guarantees High Impedance When  $V_{CC} = 0\text{V}^\dagger$
- Near Zero Static Supply Current in All Three Logic States (20 $\mu\text{A}$ ) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds  $\pm 300\text{mA}$  @ 125°C
- ESD Performance: Human Body Model >2000V; Machine Model >200V

$^\dagger$ NOTE: To ensure the outputs activate in the 3-state condition, the output enable pins should be connected to  $V_{CC}$  through a pull-up resistor. The value of the resistor is determined by the current sinking capability of the output connected to the OE pin.



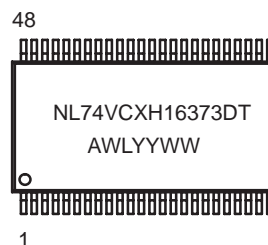
ON Semiconductor

<http://onsemi.com>



TSSOP-48  
DT SUFFIX  
CASE 1201

### MARKING DIAGRAM



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

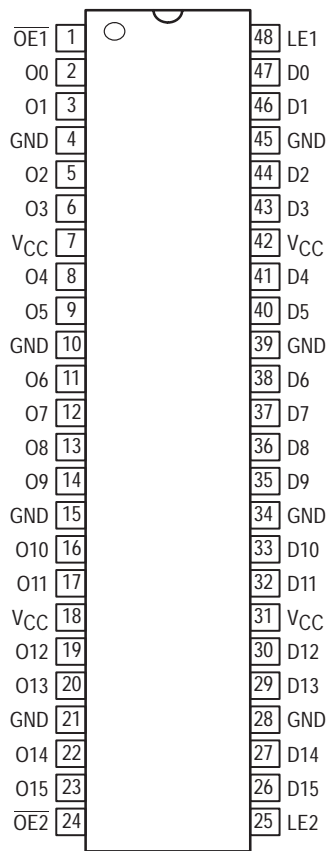
### PIN NAMES

Pins	Function
$\overline{OE_n}$	Output Enable Inputs
LEn	Latch Enable Inputs
D0–D15	Inputs
O0–O15	Outputs

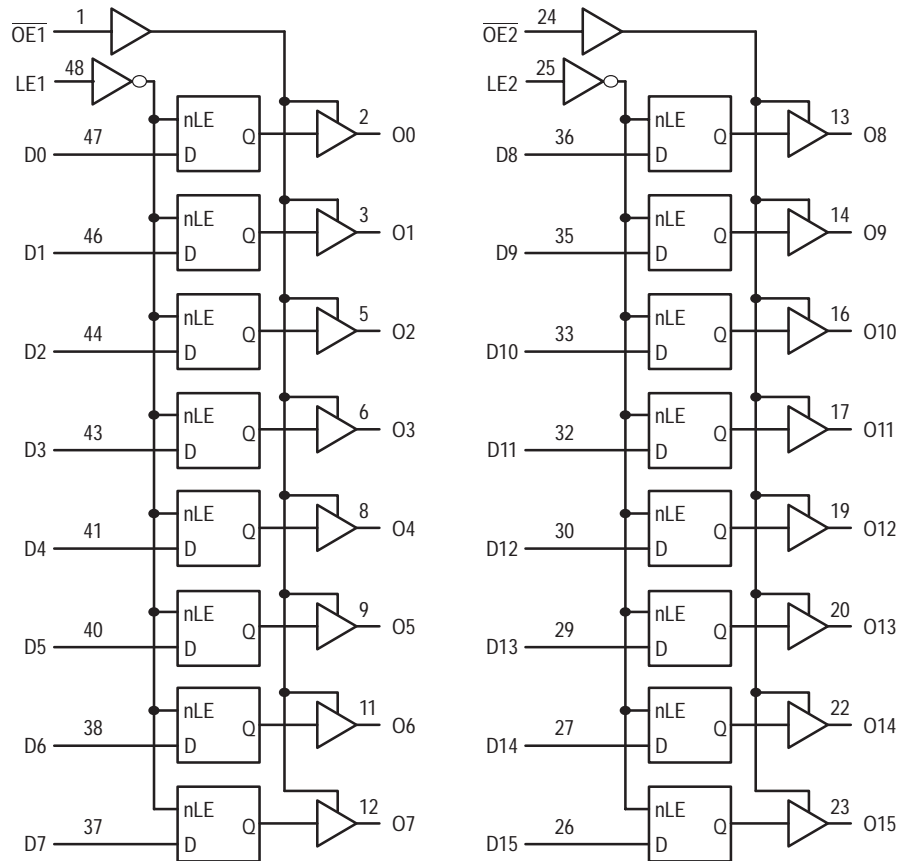
### ORDERING INFORMATION

Device	Package	Shipping
NL74VCXH16373DT	TSSOP	39 / Rail
NL74VCXH16373DTR	TSSOP	2500 / Reel

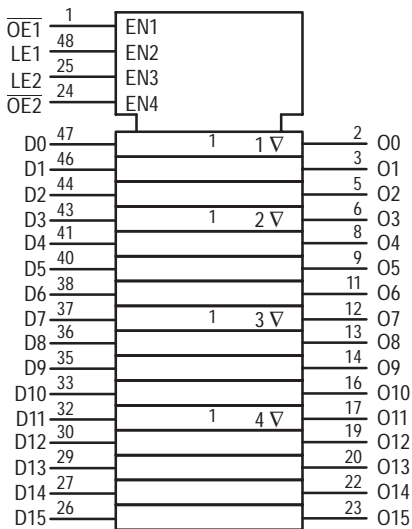
# NL74VCXH16373



**Figure 1. 48-Lead Pinout**  
(Top View)



**Figure 2. Logic Diagram**



Inputs			Outputs	Inputs			Outputs
LE1	OE1	D0:7	O0:7	LE2	OE2	D8:15	O8:15
X	H	X	Z	X	H	X	Z
H	L	L	L	H	L	L	L
H	L	H	H	H	L	H	H
L	L	X	O0	L	L	X	O0

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for ICC reasons, DO NOT FLOAT Inputs. O0 = No Change.

**ABSOLUTE MAXIMUM RATINGS\***

Symbol	Parameter	Value	Condition	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +4.6		V
$V_I$	DC Input Voltage	$-0.5 \leq V_I \leq +4.6$		V
$V_O$	DC Output Voltage	$-0.5 \leq V_O \leq +4.6$	Output in 3-State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$	Note 1.; Outputs Active	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current Per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature Range	-65 to +150		°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1.  $I_O$  absolute maximum rating must be observed.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	1.65	3.3	3.6	V
	Operating Data Retention Only	1.2	3.3	3.6	
V <sub>I</sub>	Input Voltage	−0.3		3.6	V
V <sub>O</sub>	Output Voltage	0		V <sub>CC</sub>	V
	(Active State) (3-State)	0		3.6	
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			−24	mA
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			24	mA
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 2.3V – 2.7V			−18	mA
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 2.3V – 2.7V			18	mA
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 1.65 – 1.95V			−6	mA
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 1.65 – 1.95V			6	mA
T <sub>A</sub>	Operating Free-Air Temperature	−40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8V to 2.0V, V <sub>CC</sub> = 3.0V	0		10	ns/V

# NL74VCXH16373

## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2.)	1.65V ≤ V <sub>CC</sub> < 2.3V	0.65 x V <sub>CC</sub>		V
		2.3V ≤ V <sub>CC</sub> ≤ 2.7V	1.6		
		2.7V < V <sub>CC</sub> ≤ 3.6V	2.0		
V <sub>IL</sub>	LOW Level Input Voltage (Note 2.)	1.65V ≤ V <sub>CC</sub> < 2.3V		0.35 x V <sub>CC</sub>	V
		2.3V ≤ V <sub>CC</sub> ≤ 2.7V		0.7	
		2.7V < V <sub>CC</sub> ≤ 3.6V		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	1.65V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 1.65V; I <sub>OH</sub> = -6mA	1.25		
		V <sub>CC</sub> = 2.3V; I <sub>OH</sub> = -6mA	2.0		
		V <sub>CC</sub> = 2.3V; I <sub>OH</sub> = -12mA	1.8		
		V <sub>CC</sub> = 2.3V; I <sub>OH</sub> = -18mA	1.7		
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -12mA	2.2		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -18mA	2.4		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -24mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	1.65V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OL</sub> = 100μA		0.2	V
		V <sub>CC</sub> = 1.65V; I <sub>OL</sub> = 6mA		0.3	
		V <sub>CC</sub> = 2.3V; I <sub>OL</sub> = 12mA		0.4	
		V <sub>CC</sub> = 2.3V; I <sub>OL</sub> = 18mA		0.6	
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 12mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 18mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 24mA		0.55	
I <sub>I</sub>	Input Leakage Current	1.65V ≤ V <sub>CC</sub> ≤ 3.6V; 0V ≤ V <sub>I</sub> ≤ 3.6V		±5.0	μA
I <sub>I</sub> (HOLD)	Minimum Bushold Input Current	V <sub>CC</sub> = 3.0V, V <sub>IN</sub> = 0.8V	75		μA
		V <sub>CC</sub> = 3.0V, V <sub>IN</sub> = 2.0V	-75		
		V <sub>CC</sub> = 2.3V, V <sub>IN</sub> = 0.7V	45		
		V <sub>CC</sub> = 2.3V, V <sub>IN</sub> = 1.6V	-45		
		V <sub>CC</sub> = 1.65V, V <sub>IN</sub> = 0.57V	25		
		V <sub>CC</sub> = 1.65V, V <sub>IN</sub> = 1.07V	-25		
I <sub>I</sub> (OD)	Minimum Bushold Over-Drive Current Needed to Change State	V <sub>CC</sub> = 3.6V, (Note 3.)	450		μA
		V <sub>CC</sub> = 3.6V, (Note 4.)	-450		
		V <sub>CC</sub> = 2.7V, (Note 3.)	300		
		V <sub>CC</sub> = 2.7V, (Note 4.)	-300		
		V <sub>CC</sub> = 1.95V, (Note 3.)	200		
		V <sub>CC</sub> = 1.95V, (Note 4.)	-200		
I <sub>OZ</sub>	3-State Output Current	1.65V ≤ V <sub>CC</sub> ≤ 3.6V; 0V ≤ V <sub>O</sub> ≤ 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		±10	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 3.6V		10	μA
I <sub>CC</sub>	Quiescent Supply Current (Note 5.)	1.65V ≤ V <sub>CC</sub> ≤ 3.6V; V <sub>I</sub> = GND or V <sub>CC</sub>		20	μA
		1.65V ≤ V <sub>CC</sub> ≤ 3.6V; 3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 3.6V		±20	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.7V < V <sub>CC</sub> ≤ 3.6V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		750	μA

2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

3. An external driver must source at least the specified current to switch from LOW-to-HIGH

4. An external driver must source at least the specified current to switch from HIGH-to-LOW

5. Outputs disabled or 3-state only.

# NL74VCXH16373

## AC CHARACTERISTICS (Note 6.; $t_R = t_F = 2.0\text{ns}$ ; $C_L = 30\text{pF}$ ; $R_L = 500\Omega$ )

Symbol	Parameter	Waveform	Limits						Unit
			T <sub>A</sub> = −40°C to +85°C						
			V <sub>CC</sub> = 3.0V to 3.6V		V <sub>CC</sub> = 2.3V to 2.7V		V <sub>CC</sub> = 1.65 to 1.95V		
			Min	Max	Min	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Dn to On	1	0.8 0.8	3.0 3.0	1.0 1.0	3.4 3.4	1.5 1.5	6.8 6.8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LE to On	1	0.8 0.8	3.0 3.0	1.0 1.0	3.9 3.9	1.5 1.5	7.8 7.8	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to High and Low Level	2	0.8 0.8	3.5 3.5	1.0 1.0	4.6 4.6	1.5 1.5	9.2 9.2	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time From High and Low Level	2	0.8 0.8	3.5 3.5	1.0 1.0	3.8 3.8	1.5 1.5	6.8 6.8	ns
t <sub>s</sub>	Setup Time, High or Low Dn to LE	3	1.5		1.5		2.5		ns
t <sub>h</sub>	Hold Time, High or Low Dn to LE	3	1.0		1.0		1.0		ns
t <sub>w</sub>	LE Pulse Width, High	3	1.5		1.5		4.0		ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 7.)			0.5 0.5		0.5 0.5		0.75 0.75	ns

6. For  $C_L = 50\text{pF}$ , add approximately 300ps to the AC maximum specification.

7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$	Unit
			Typ	
$V_{OLP}$	Dynamic LOW Peak Voltage (Note 8.)	$V_{CC} = 1.8\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	0.25	V
		$V_{CC} = 2.5\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	0.6	
		$V_{CC} = 3.3\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	0.8	
$V_{OLV}$	Dynamic LOW Valley Voltage (Note 8.)	$V_{CC} = 1.8\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	-0.25	V
		$V_{CC} = 2.5\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	-0.6	
		$V_{CC} = 3.3\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	-0.8	
$V_{OHV}$	Dynamic HIGH Valley Voltage (Note 9.)	$V_{CC} = 1.8\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.5	V
		$V_{CC} = 2.5\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.9	
		$V_{CC} = 3.3\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	2.2	

8. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

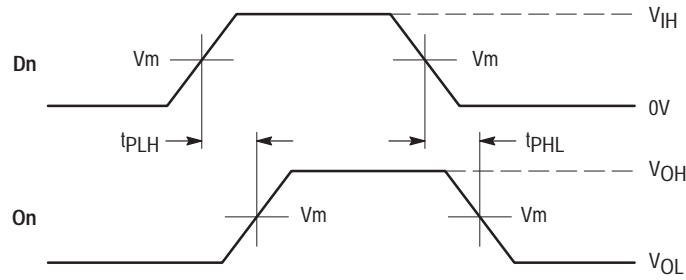
9. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the HIGH state.

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance	Note 10.	6	pF
$C_{OUT}$	Output Capacitance	Note 10.	7	pF
$C_{PD}$	Power Dissipation Capacitance	Note 10., 10MHz	20	pF

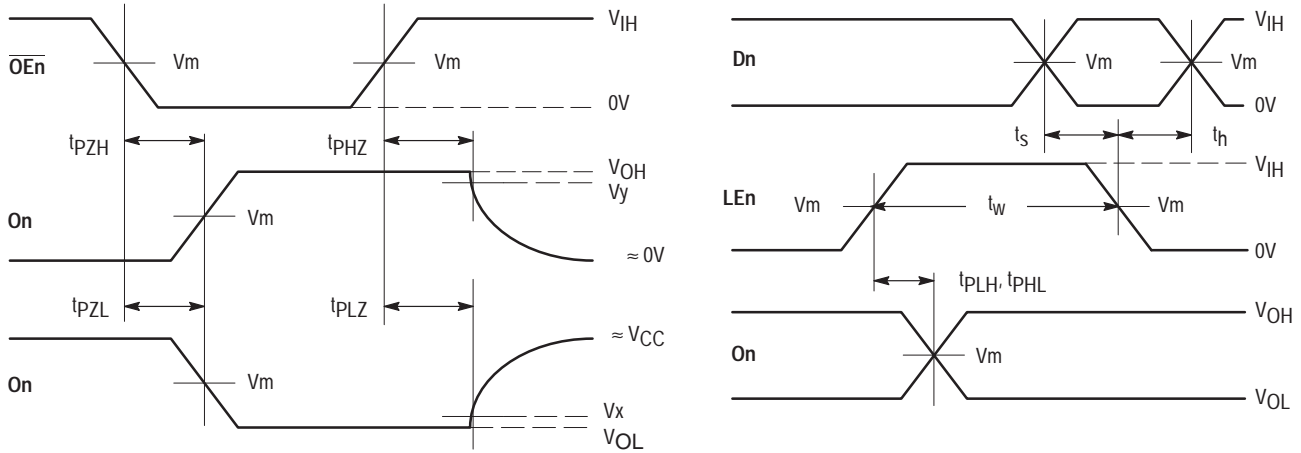
10.  $V_{CC} = 1.8, 2.5$  or  $3.3\text{V}$ ;  $V_I = 0\text{V}$  or  $V_{CC}$ .

# NL74VCXH16373



**WAVEFORM 1 – PROPAGATION DELAYS**  
 $t_R = t_F = 2.0\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

**Figure 3. AC Waveforms**

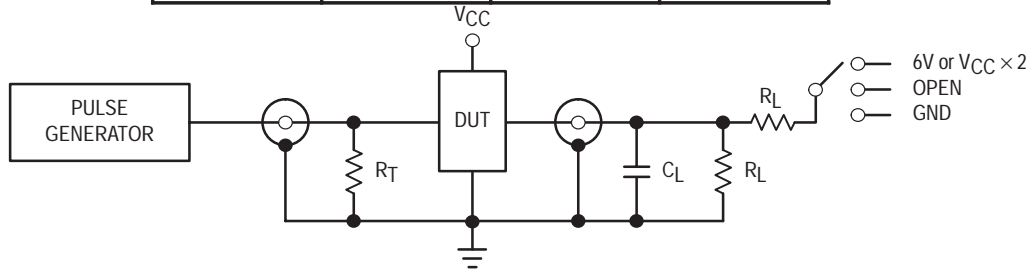


**WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES**  
 $t_R = t_F = 2.0\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

**WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES**  
 $t_R = t_F = 2.0\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$  except when noted

**Figure 4. AC Waveforms**

Symbol	V <sub>CC</sub>		
	3.3V ±0.3V	2.5V ±0.2V	1.8V ±0.15V
V <sub>IH</sub>	2.7V	V <sub>CC</sub>	V <sub>CC</sub>
V <sub>m</sub>	1.5V	V <sub>CC</sub> /2	V <sub>CC</sub> /2
V <sub>x</sub>	V <sub>OL</sub> + 0.3V	V <sub>OL</sub> + 0.15V	V <sub>OL</sub> + 0.15V
V <sub>y</sub>	V <sub>OH</sub> - 0.3V	V <sub>OH</sub> - 0.15V	V <sub>OH</sub> - 0.15V

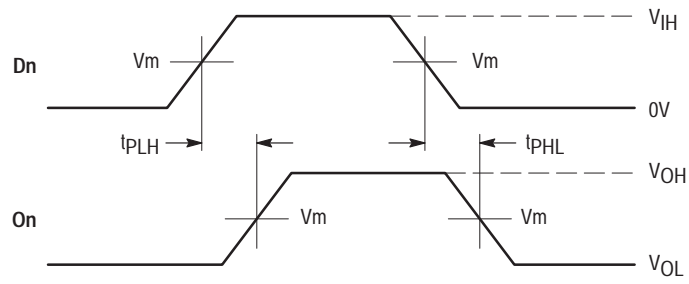


TEST	SWITCH
t <sub>PLH</sub> , t <sub>PHL</sub>	Open
t <sub>PZL</sub> , t <sub>PLZ</sub>	6V at V <sub>CC</sub> = 3.3 ±0.3V; V <sub>CC</sub> × 2 at V <sub>CC</sub> = 2.5 ±0.2V; 1.8V ±0.15V
t <sub>PZH</sub> , t <sub>PHZ</sub>	GND

$C_L = 30\text{pF}$  or equivalent (Includes jig and probe capacitance)  
 $R_L = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically 50Ω)

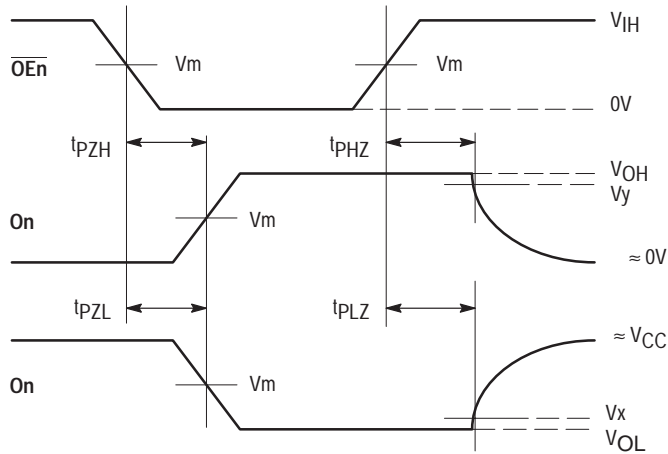
**Figure 5. Test Circuit**

# NL74VCXH16373

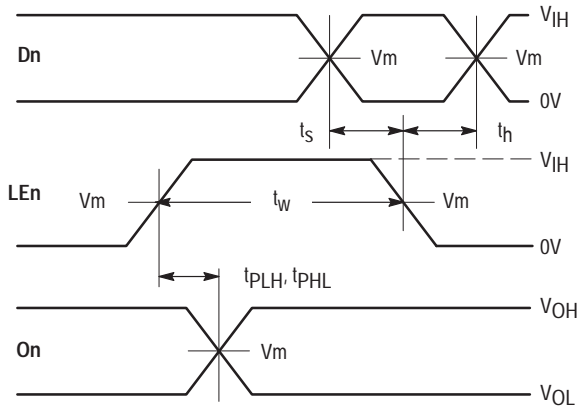


**WAVEFORM 4 – PROPAGATION DELAYS**  
 $t_R = t_F = 2.0\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

**Figure 6. AC Waveforms**



**WAVEFORM 5 – OUTPUT ENABLE AND DISABLE TIMES**  
 $t_R = t_F = 2.0\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$



**WAVEFORM 6 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES**  
 $t_R = t_F = 2.0\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$  except when noted

**Figure 7. AC Waveforms**

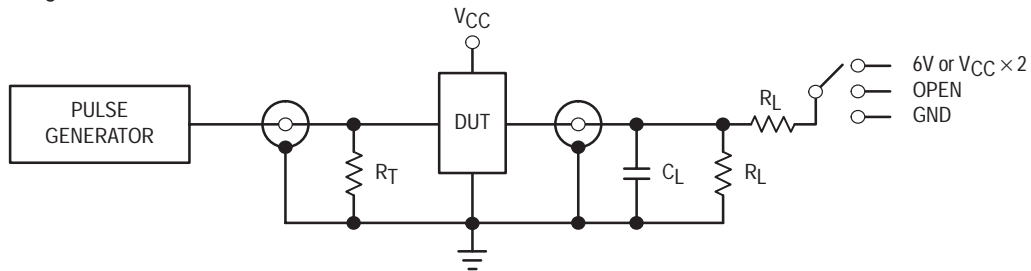
Symbol	VCC	
	3.3V ±0.3V	2.7V
VIH	2.7V	2.7V
Vm	1.5V	1.5V
Vx	VOL + 0.3V	VOL + 0.3V
Vy	VOH – 0.3V	VOH – 0.3V

# NL74VCXH16373

**AC CHARACTERISTICS** ( $t_R = t_F = 2.0\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ )

Symbol	Parameter	Waveform	Limits				Unit
			T <sub>A</sub> = −40°C to +85°C				
			V <sub>CC</sub> = 3.0V to 3.6V		V <sub>CC</sub> = 2.7V		
			Min	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Dn to On	4	1.0 1.0	3.6 3.6		4.3 4.3	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LE to On	4	1.0 1.0	3.9 3.9		4.6 4.6	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to High and Low Level	5	1.0 1.0	4.7 4.7		5.7 5.7	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time From High and Low Level	5	1.0 1.0	4.1 4.1		4.5 4.5	ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 11.)			0.5 0.5		0.5 0.5	ns

11. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.



TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3\text{V}$ ; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2\text{V}$ ; $1.8\text{V} \pm 0.15\text{V}$
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 50\text{pF}$  or equivalent (Includes jig and probe capacitance)

$R_L = 500\Omega$  or equivalent

$R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

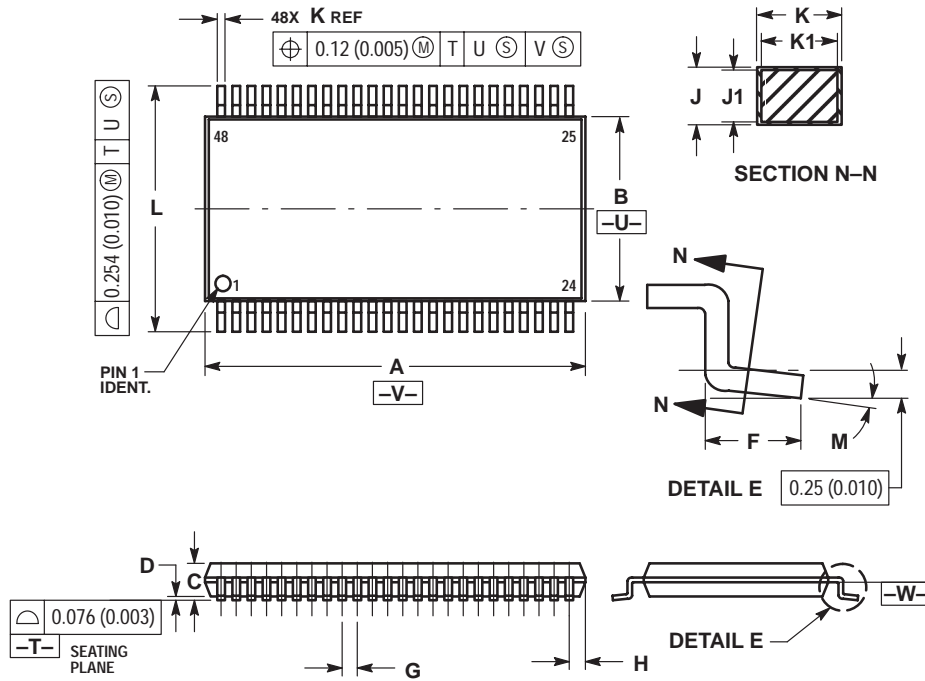
**Figure 8. Test Circuit**



# NL74VCXH16373

## PACKAGE DIMENSIONS

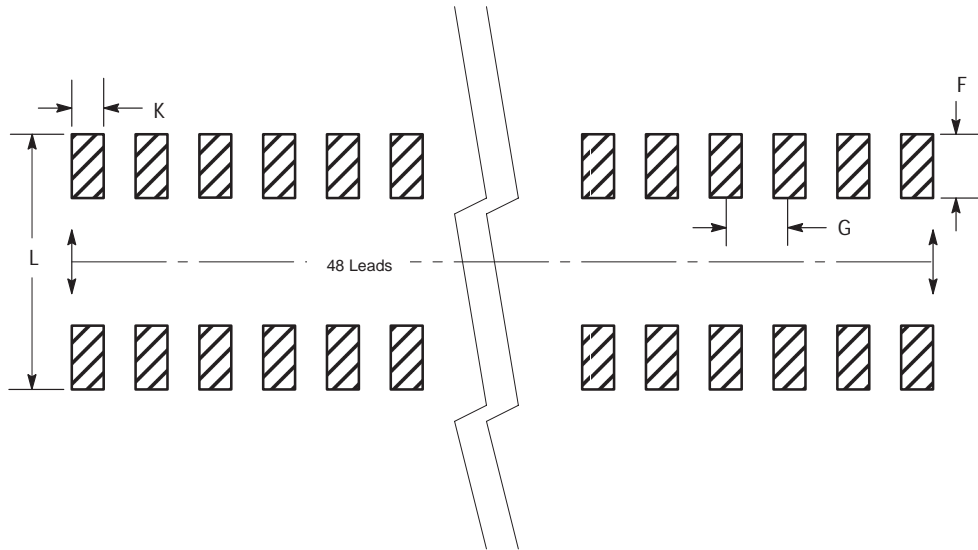
TSSOP  
DT SUFFIX  
CASE 1201-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	—	1.10	—	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	—	0.015	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8 °	0 °	8 °



Package Footprint

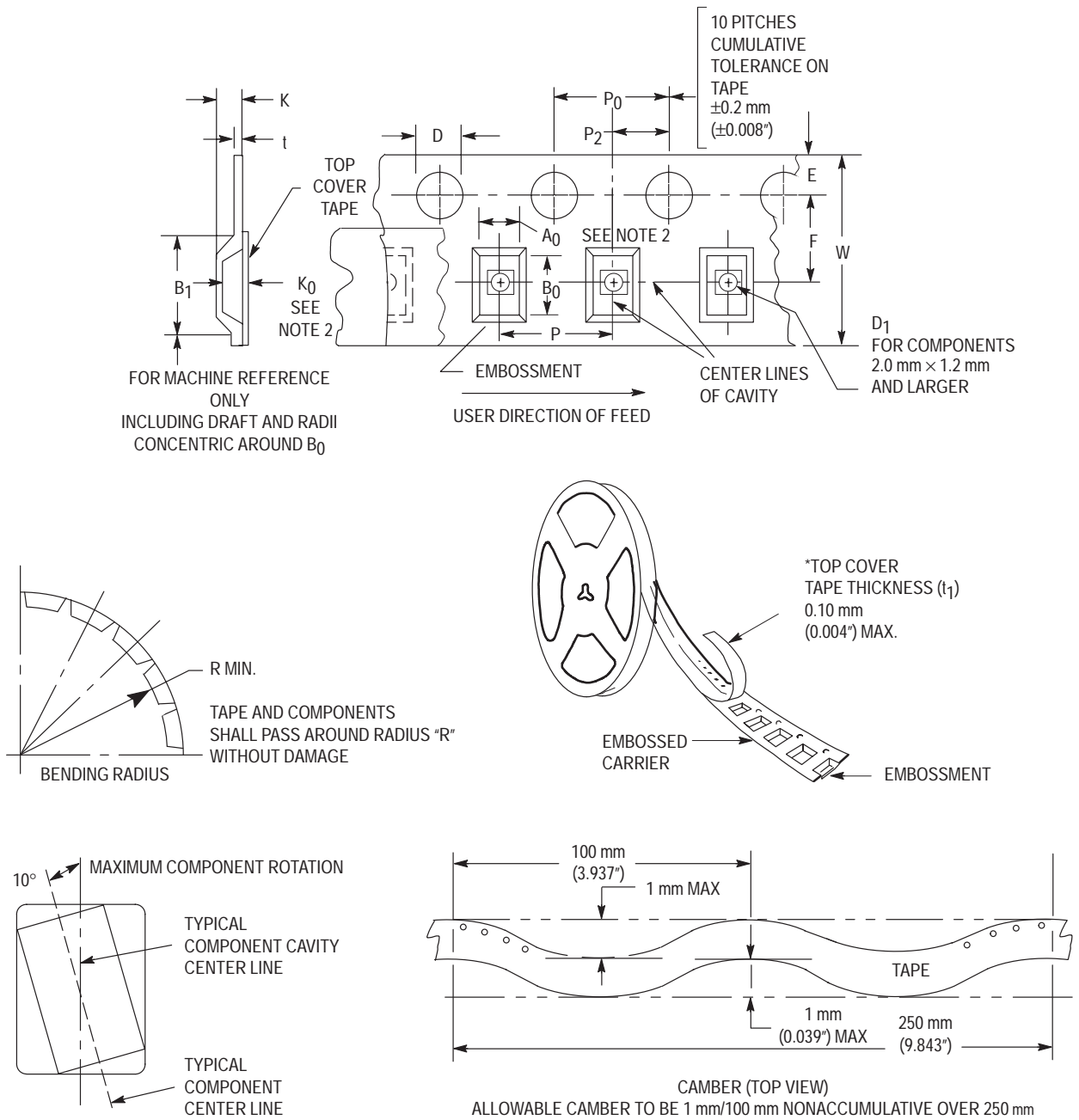


Figure 9. Carrier Tape Specifications

**EMBOSSED CARRIER DIMENSIONS** (See Notes 1 and 2)

Tape Size	$B_1$ Max	D	$D_1$	E	F	K	P	$P_0$	$P_2$	R	T	W
24mm	20.1mm (0.791")	1.5 + 0.1mm - 0.0 (0.059 +0.004" - 0.0)	1.5mm Min (0.060")	1.75 $\pm 0.1$ mm (0.069 $\pm 0.004$ ")	11.5 $\pm 0.10$ mm (0.453 $\pm 0.004$ ")	11.9 mm Max (0.468")	16.0 $\pm 0.1$ mm (0.63 $\pm 0.004$ ")	4.0 $\pm 0.1$ mm (0.157 $\pm 0.004$ ")	2.0 $\pm 0.1$ mm (0.079 $\pm 0.004$ ")	30 mm (1.18")	0.6 mm (0.024")	24.3 mm (0.957")

1. Metric Dimensions Govern—English are in parentheses for reference only.
2.  $A_0$ ,  $B_0$ , and  $K_0$  are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

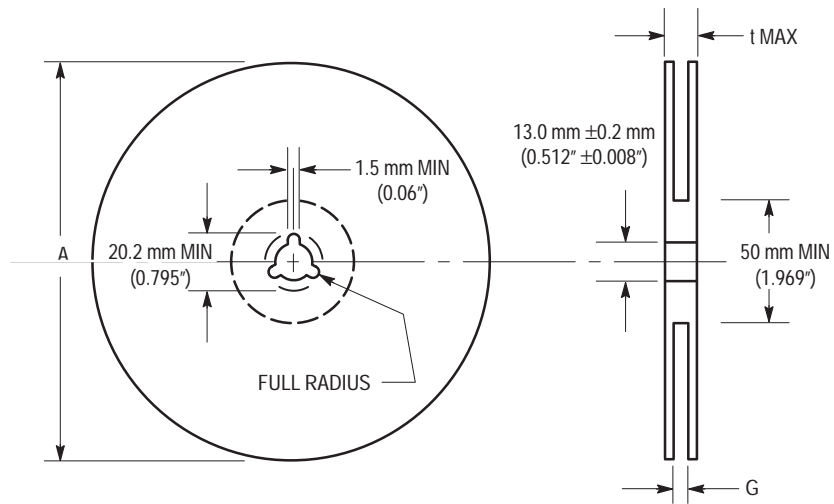


Figure 10. Reel Dimensions

REEL DIMENSIONS

Tape Size	A Max	G	t Max
24 mm	360 mm (14.173")	24.4 mm + 2.0 mm, -0.0 (0.961" + 0.078", -0.00)	30.4 mm (1.197")

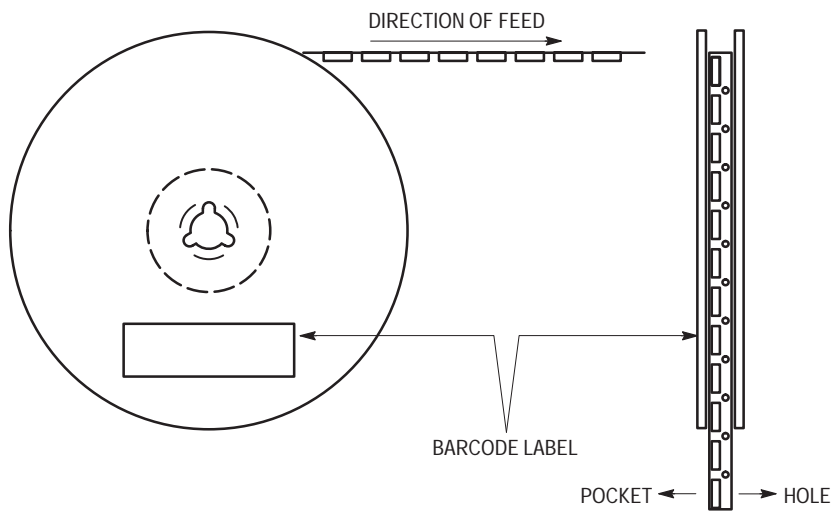


Figure 11. Reel Winding Direction

## NL74VCXH16373

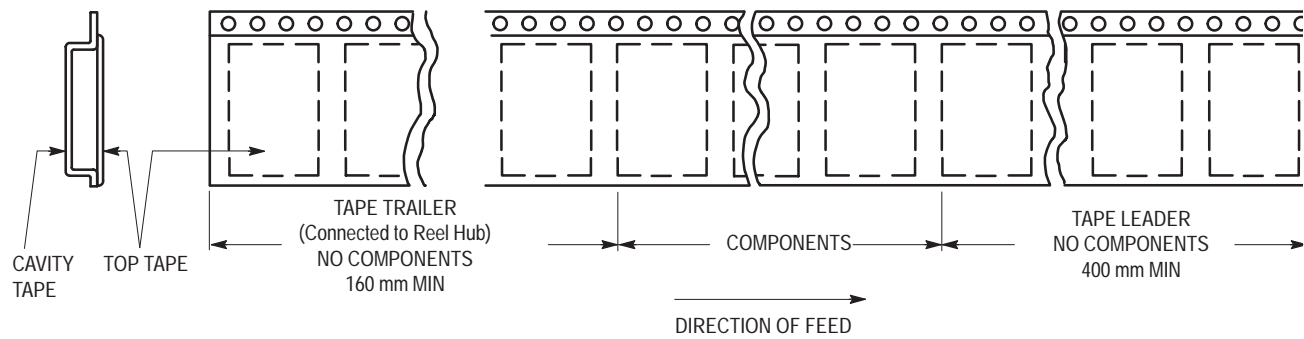


Figure 12. Tape Ends for Finished Goods

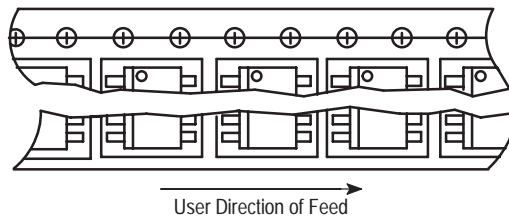



Figure 13. Reel Configuration

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

### PUBLICATION ORDERING INFORMATION

#### NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com  
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

#### N. American Technical Support: 800-282-9855 Toll Free USA/Canada

#### EUROPE: LDC for ON Semiconductor – European Support

**German Phone:** (+1) 303-308-7140 (M–F 1:00pm to 5:00pm Munich Time)  
**Email:** ONlit-german@hibbertco.com  
**French Phone:** (+1) 303-308-7141 (M–F 1:00pm to 5:00pm Toulouse Time)  
**Email:** ONlit-french@hibbertco.com  
**English Phone:** (+1) 303-308-7142 (M–F 12:00pm to 5:00pm UK Time)  
**Email:** ONlit@hibbertco.com

#### EUROPEAN TOLL-FREE ACCESS\*: 00-800-4422-3781

\*Available from Germany, France, Italy, England, Ireland

#### CENTRAL/SOUTH AMERICA:

**Spanish Phone:** 303-308-7143 (Mon–Fri 8:00am to 5:00pm MST)  
**Email:** ONlit-spanish@hibbertco.com

#### ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

**Phone:** 303-675-2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)  
Toll Free from Hong Kong & Singapore:  
**001-800-4422-3781**  
**Email:** ONlit-asia@hibbertco.com

#### JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549  
**Phone:** 81-3-5740-2745  
**Email:** r14525@onsemi.com

#### ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.