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SSI 78Q8360
Ethernet Controller/ ENDEC Combo

Preliminary Data

December 1992

DESCRIPTION

The SSI 78Q8360 is a combination Media Access Controller (MAC) and 10 Mbit/s Manchester encoder/ decoder (ENDEC) with Attachment Unit Interface (AUI) for IEEE 802.3 applications. It is connected to the transmission medium through the AUI with a transceiver circuit such as the SSI 78Q8330 Ethernet Coax Transceiver or the 78Q902 10BaseT Transceiver. Connection to the host is accomplished via external bus decoding logic.

An intelligent Buffer Manager is controlled by the host read, host write, receive and transmit pointers, and the 8360 manages the pointers internally without any host intervention. The 8360 interleaves access to the buffer memory so that accesses from the host and from the network media seem to operate concurrently.

The 8360 has a sophisticated power management capability with three different operating modes allowing the user to maximize power savings. Interface with the host can be accomplished in several different ways: memory mapping, I/O mapping, programmable DMA or a combination of these. Big and little endian byte orderings make for simple bus interface to all standard microprocessors. The 78Q8360 is packaged in a 100-pin QFP or TQFP and uses a single 5V supply.

FEATURES

- IEEE 802.3 and Ethernet 2.0 compliant
- Power management options include:
  - Intelligent power mode automatically shuts off unused circuitry
  - Standby mode reduces power while not in operation
  - Full power-down mode offers maximum power savings
- Advanced Buffer Manager architecture:
  - Automatic management of all pointers
  - Allows "simultaneous" access to data in buffer memory by both the network and host
  - High-speed received packet skip
- Configurable Buffer Memory for design flexibility:
  - Two-bank transmit buffer in 2, 4, 8, or 16 Kbyte sizes
  - Ring-structure receive buffer from 4 to 62 Kbytes
- Software-configurable system bus structure:
  - Compatible with major microprocessors
  - 8- or 16-bit wide data path
  - Supports single and programmable burst DMA, I/O and interrupt operations
- Three different loopback modes
- Multicast address filtering via 64-element hash table

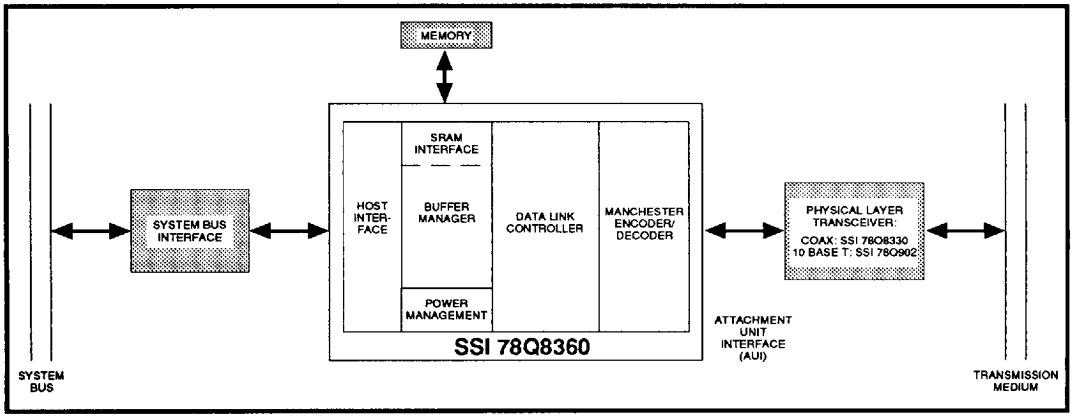

FIGURE 1: System Diagram

SSI 78Q8360 Ethernet Controller/ ENDEC Combo

FUNCTIONAL DESCRIPTION

The 78Q8360 consists of five major blocks:

- Buffer Manager (and SRAM Interface)
- Data Link Controller
- Host Interface
- Manchester ENDEC
- Power Management

A block diagram of the 78Q8360 is shown in Figure 2.

BUFFER MANAGER

The Buffer Manager manages all accesses to the buffer memory through the SRAM interface. The buffer memory is connected directly to the Data Link Controller (DLC), thus eliminating the need for a local microprocessor. The Buffer Manager also keeps track of all buffer memory pointers automatically, simplifying the software driver task. Together with intelligent arbitration, this makes the 8360 a high performance LAN controller.

The buffer memory is divided into two portions: transmit memory portion and receive memory portion. The transmit memory portion can be partitioned into 2K, 4K, 8K or 16 Kbyte buffer sizes. There is only one transmit bank if a 2 KB transmit buffer size is selected. If the transmit buffer size is greater than 2 KB, then the transmit buffer is configured into two banks of equal size. With the two bank configuration, one transmit bank may be tied up during transmission but the host can still continue to load data packets into the second transmit bank to be transmitted later. The receive buffer has a ring architecture which can be configured from 4K to 62 KB depending on the buffer memory configuration which has a range of 8K to 64 KB.

A central arbitrator inside the Buffer Manager prioritizes and services requests for access to the buffer memory from 4 sources: the Transmitter, the Receiver, Host Read and Host Write. If necessary, the 8360 will assert a 'not ready' handshake to the host while servicing the Transmitter and/or Receiver. The 8360 arbitration mechanism provides packet management by interleaving packet data accesses to the buffer memory such that the operation appears to be simultaneous.

For instance, in the situation where 2 transmit banks are configured, the host can load the first transmit bank and initiate a transmission. While the first transmit bank is being transmitted, the host can continue to load packets in the second transmit bank. At this stage, the 8360 can potentially be receiving data from the medium and loading it into the receive buffer (if the 8360 is in a loop back mode or if self-reception occurs).

DATA LINK CONTROLLER

The Data Link Controller (DLC) implements the ISO/ ANSI/IEEE 8802-3 CSMA/CD protocol. It consists of a Transmitter, a Receiver and CRC logic (which is shared by both transmit and receive operations). Automatic generation and stripping of the 64-bit preamble and the 32-bit CRC code are provided on-chip.

HOST INTERFACE

The Host Interface (HIF) provides connection to the host system. It consists of the various registers, DMA circuits and ready logic. Both word and byte interfaces are supported as well as big endian and little endian data ordering. Host access to the buffer memory is through BMR8 (and BMR9). Reading from BMR8 will read a byte or word from the receive buffer and writing to BMR8 will write a byte or word to the transmit buffer. The ready logic is capable of delaying host access to the buffer memory with a time-out mechanism. Both single and burst DMA transfer modes are supported.

MANCHESTER ENDEC

This block implements Manchester encoding and decoding. Serial NRZ data from the DLC is converted to Manchester encoded data and sent to TDP and TDN outputs through the Attachment Unit Interface (AUI) driver. The decoder section performs three functions on the data received at RDP and RDN: clock recovery, carrier detection and Manchester decoding. The recovered receive clock will be low at the end of reception and during idle to save power. Jitter of up to 20 nsec can be tolerated by the decoder. Collisions detected at the transceiver are presented as a 10 MHz signal at CDP and CDN and are then converted to a logic level signal and passed to the DLC.

POWER MANAGEMENT

One very useful and important feature that the 8360 offers is intelligent power management. It supports three different power saving modes: Intelligent, Standby, and Full Shutdown. All modes are configurable through registers. In the Intelligent mode, clocks are active only when they are needed. For example, when not transmitting, the clock supplied to the transmitter circuit in the DLC block is not active while host read from buffer memory may be active. In Standby mode, the oscillator clock is disconnected from the rest of the circuits, so that only the oscillator circuits draw power. Full Shutdown turns off the oscillator, resulting in maximum power savings. Note that this mode is not available when using an external clock source.

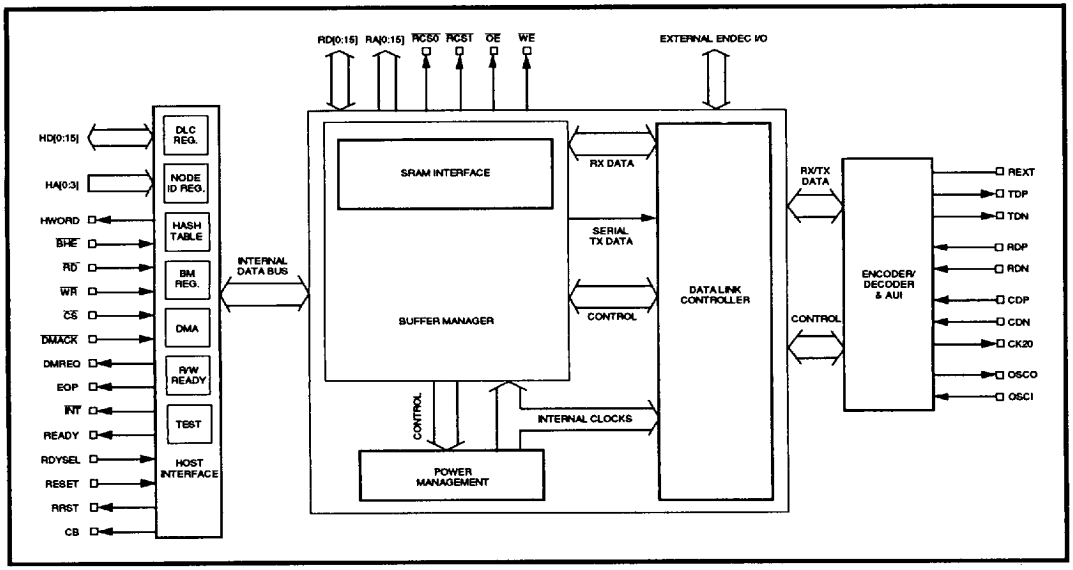

FIGURE 2: 78Q8360 Block Diagram

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PIN ASSIGNMENT TABLE – 100-Pin QFP

PIN #	PIN NAME	TYPE	PIN #	PIN NAME	TYPE	PIN #	PIN NAME	TYPE	PIN #	PIN NAME	TYPE
1	HD11	IO8U	26	DMREQ	O16	51	$\overline{RCS0}$	O4	76	OSCI	I[2]
2	HD10	IO8U	27	$\overline{DMACK}$	I	52	$\overline{RCS1}$	O4	77	OSCO	O[2]
3	VDD	P	28	VDD	P	53	VDD	P	78	AVDD	P
4	GND	P	29	$\overline{RD}$	I	54	RA0	O4	79	AGND	P
5	HD9	IO8U	30	$\overline{WR}$	I	55	RA1	O4	80	TXC	IO4U
6	HD8	IO8U	31	RESET	I[1]	56	RA2	O4	81	RDN	AI
7	$\overline{CS}$	I	32	RD0	IO4U	57	RA3	O4	82	RDP	AI
8	$\overline{BHE}$	I	33	RD1	IO4U	58	RA4	O4	83	CDN	AI
9	HWORD	O4	34	RD2	IO4U	59	RA5	O4	84	CDP	AI
10	HA0	I	35	RD3	IO4U	60	RA6	O4	85	VDD	P
11	HA1	I	36	RD4	IO4U	61	RA7	O4	86	LOOP	IO4U
12	HA2	I	37	RD5	IO4U	62	RA8	O4	87	REXT	-[3]
13	HA3	I	38	RD6	IO4U	63	RA9	O4	88	RXC	IO4U
14	READY	O4	39	RD7	IO4U	64	RA10	O4	89	CK20	O2
15	GND	P	40	GND	P	65	GND	P	90	GND	P
16	HD0	IO8	41	RD8	IO4U	66	RA11	O4	91	RXD	IO4U
17	HD1	IO8	42	RD9	IO4U	67	RA12	O4	92	COL	IO4U
18	HD2	IO8	43	RD10	IO4U	68	RA13	O4	93	CRS	IO4U
19	HD3	IO8	44	RD11	IO4U	69	RA14	O4	94	RDYSEL	I
20	HD4	IO8	45	RD12	IO4U	70	RA15	O4	95	CB	O4
21	HD5	IO8	46	RD13	IO4U	71	TXE	IO4U	96	RRST	O4
22	HD6	IO8	47	RD14	IO4U	72	TXD	IO4U	97	HD15	IO8U
23	HD7	IO8	48	RD15	IO4U	73	GND	P	98	HD14	IO8U
24	EOP	I	49	$\overline{OE}$	O4	74	TDN	AO	99	HD13	IO8U
25	$\overline{INT}$	O4	50	$\overline{WE}$	O4	75	TDP	AO	100	HD12	IO8U

Legend:

I: Input (TTL level)
On: Output with IOL = n mA
IOn: Input (TTL level) and Output with IOL = n mA
IOnU: IOn with "controlled" internal pull-up resistor
AI: Analog Input
AO: Analog Output
P: Power

Notes:

[1] RESET has a Schmitt trigger and a pull-down resistor.
[2] OSCI and OSCO have CMOS level.
[3] REXT is connected to a resistor and then to analog ground.

PIN ASSIGNMENT TABLE – 100-Pin TQFP

PIN #	PIN NAME	TYPE	PIN #	PIN NAME	TYPE	PIN #	PIN NAME	TYPE	PIN #	PIN NAME	TYPE
1	GND	P	26	$\overline{RD}$	I	51	RA0	O4	76	AGND	P
2	HD9	IO8U	27	$\overline{WR}$	I	52	RA1	O4	77	TXC	IO4U
3	HD8	IO8U	28	RESET	I[1]	53	RA2	O4	78	RDN	AI
4	$\overline{CS}$	I	29	RD0	IO4U	54	RA3	O4	79	RDP	AI
5	$\overline{BHE}$	I	30	RD1	IO4U	55	RA4	O4	80	CDN	AI
6	HWORD	O4	31	RD2	IO4U	56	RA5	O4	81	CDP	AI
7	HA0	I	32	RD3	IO4U	57	RA6	O4	82	VDD	P
8	HA1	I	33	RD4	IO4U	58	RA7	O4	83	LOOP	IO4U
9	HA2	I	34	RD5	IO4U	59	RA8	O4	84	REXT	-[3]
10	HA3	I	35	RD6	IO4U	60	RA9	O4	85	RXC	IO4U
11	READY	O4	36	RD7	IO4U	61	RA10	O4	86	CK20	O2
12	GND	P	37	GND	P	62	GND	P	87	GND	P
13	HD0	IO8	38	RD8	IO4U	63	RA11	O4	88	RXD	IO4U
14	HD1	IO8	39	RD9	IO4U	64	RA12	O4	89	COL	IO4U
15	HD2	IO8	40	RD10	IO4U	65	RA13	O4	90	CRS	IO4U
16	HD3	IO8	41	RD11	IO4U	66	RA14	O4	91	RDYSEL	I
17	HD4	IO8	42	RD12	IO4U	67	RA15	O4	92	CB	O4
18	HD5	IO8	43	RD13	IO4U	68	TXE	IO4U	93	RRST	O4
19	HD6	IO8	44	RD14	IO4U	69	TXD	IO4U	94	HD15	IO8U
20	HD7	IO8	45	RD15	IO4U	70	GND	P	95	HD14	IO8U
21	EOP	I	46	$\overline{OE}$	O4	71	TDN	AO	96	HD13	IO8U
22	$\overline{INT}$	O4	47	$\overline{WE}$	O4	72	TDP	AO	97	HD12	IO8U
23	DMREQ	O16	48	$\overline{RCS0}$	O4	73	OSCI	I[2]	98	HD11	IO8U
24	$\overline{DMACK}$	I	49	$\overline{RCS1}$	O4	74	OSCO	O[2]	99	HD10	IO8U
25	VDD	P	50	VDD	P	75	AVDD	P	100	VDD	P

Legend:
I: Input (TTL level)
On: Output with IOL = n mA
IOn: Input (TTL level) and Output with IOL = n mA
IOnU: IOn with "controlled" internal pull-up resistor
AI: Analog Input
AO: Analog Output
P: Power

Notes:
[1] RESET has a Schmitt trigger and a pull-down resistor.
[2] OSCI and OSCO have CMOS level.
[3] REXT is connected to a resistor and then to analog ground.

PIN DESCRIPTION

HOST BUS INTERFACE

NAME	TYPE	DESCRIPTION
RESET	I	HARDWARE RESET. Active high. A minimum pulse length of 200 ns is required. This pin resets the 8360's internal pointers and registers to their appropriate states. NB: the 8360 must be reset after power on before usage.
READY	O	READY. This output is asserted to indicate to the host that the 8360 is ready to complete the requested read or write operation. It will also be used if the device is unable to respond to read or write requests within 2.4 µs. In these situations, the 8360 will also assert $\overline{INT}$ and the host read error status bit (DLCR1 <6>) or host write error status bit (DLCR0 <0>). The polarity of the READY pin is determined by RDYSEL.
RDYSEL	I	READY POLARITY SELECT. Control input to select the polarity of the READY pin. When RDYSEL is a '1', READY will be active high. If RDYSEL is a '0', READY will be an active low signal.
$\overline{WR}$	I	WRITE. The $\overline{WR}$ pin is an active low input that enables a write operation from the host to the 8360's internal registers as selected by the host address inputs HA[0:3].
$\overline{RD}$	I	READ. The $\overline{RD}$ pin is an active low input that enables a read operation by the host from the 8360's internal registers as selected by the host address inputs HA[0:3].
$\overline{CS}$	I	CHIP SELECT. An active low input signal as the chip select for the 8360.
$\overline{BHE}$	I	BYTE HIGH ENABLE. This is an active low byte/word control pin used only when the 8360 is configured for word transfer by HBYTE bit (DLCR6 <5>). Combinations of $\overline{BHE}$ and HA0 are used to select word, upper byte only or lower byte only transfers.
$\overline{INT}$	O	INTERRUPT. This active low signal is asserted when the 8360 requires the intervention of the Host in the situations as depicted in DLCR0&1. The $\overline{INT}$ signal is masked by writing a '0' to the interrupt enable register.
EOP	I	END OF PROCESS. Asserted at the end of a DMA transfer by the Host DMA controller. Further DMA requests (DMREQ) will be discontinued after EOP is asserted. Polarity can be selected via register bit (DLCR7 <1>).
DMREQ	O	DMA REQUEST. The 8360 issues a DMREQ to the Host DMA controller to initiate a write to its transmit buffer or a read from its receive buffer.

HBYTE	$\overline{BHE}$	HA0	FUNCTION
0	0	0	Word transfer
0	0	1	Byte transfer on high bus HD[8:15].
0	1	0	Byte transfer on low bus HD[0:7].
0	1	1	Reserved
1	X	X	Byte transfer (HD[0:7])

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{DMACK}}$	I	DMA ACKNOWLEDGE. An active low signal issued by the Host DMA controller when it is ready to perform data transfers between the Host and the 8360's buffer memory via BMR8.
HA[0:3]	I	HOST ADDRESS. Selects the set of internal registers to be accessible by the 8360 for read or write operations.
HD[0:15]	I/O	HOST DATA BUS. A bi-directional, tri-state bus for data, command and status transfers between the Host and the 8360 with the direction being controlled by $\overline{\text{RD}}$ and $\overline{\text{WR}}$. The combinations of HBYTE, $\overline{\text{BHE}}$ and HA0 control the portion of the bus that is being utilized. HA[0:3] and RBNK <0:1> (DLCR7 <2:3>) select the set of internal registers for access.
HWORD	O	HOST WORD CONFIGURATION. This pin is the complement of the register bit HBYTE (DLCR6 <5>). If HBYTE is a '0', the Host interface is configured for word transfers. If HBYTE is a '1', the Host interface is configured for byte transfers on the lower bus, HD[0:7].

BUFFER MEMORY INTERFACE

$\overline{\text{RCS0}}$, $\overline{\text{RCS1}}$	O	RAM CHIP SELECT. $\overline{\text{RCS0}}$ and $\overline{\text{RCS1}}$ are active low chip select lines for the SRAM with $\overline{\text{RCS0}}$ as the least significant byte.
$\overline{\text{OE}}$	O	RAM OUTPUT ENABLE. Active low. This is the output enable asserted by the 8360 during buffer memory read cycles for the SRAM.
$\overline{\text{WE}}$	O	RAM WRITE ENABLE. Active low. This is the write enable asserted by the 8360 during buffer memory write cycles for the SRAM.
RD[0:15]	I/O	RAM DATA BUS. This is the data bus between the 8360 and the buffer memory. It can be configured for byte or word transfer depending on register bit RBYTE (DLCR6 <4>) RAM BYTE. For word transfers, the ordering of the most and least significant byte is defined by the register bit, INTLMOT (DLCR7 <0>).
RA[0:15]	O	RAM ADDRESS BUS. Addresses up to 64 KByte of SRAM buffer memory.

NETWORK INTERFACE

TDN, TDP	O	TRANSMIT DATA NEGATIVE and POSITIVE. Differential outputs to the transceiver for transmission.
RDN, RDP	I	RECEIVE DATA NEGATIVE and POSITIVE. Manchester differential inputs from the transceiver for reception.
CDN, CDP	I	COLLISION DETECT NEGATIVE and POSITIVE. When the transceiver detects a collision on the media, these differential inputs are driven by a 10 MHz signal.
REXT	-	EXTERNAL RESISTOR. External biasing resistor for the Attachment Unit Interface (AUI).

EXTERNAL ENCODER/DECODER INTERFACE

The following eight pins are provided for connection to an external encoder/decoder in the optional mode of using an external encoder/decoder with the 78Q8360. They are also used as monitor pins for test purposes. In normal network interface applications these pins are not used and are pulled-up internally. Optional modes of configuration are determined by the EEDCNTL <1:0> register bits DLCR7<7:6>.

CONTROLLER-ENCODER/DECODER INTERFACE

NAME	TYPE	DESCRIPTION
TXD	I/O	TRANSMIT DATA. Normally not used. (Non-Return to Zero) NRZ transmit serial data.
TXC	I/O	TRANSMIT CLOCK. Normally not used. A synchronous 10 MHz clock with the serially transmitted data, TXD.
TXE	I/O	TRANSMIT ENABLE. Normally not used. Enable for transmission.
COL	I/O	COLLISION. Normally not used. Active high collision signal.
LOOP	I/O	LOOP BACK. Normally not used. ENDEC loop back test signal.
RXD	I/O	RECEIVE DATA. Normally not used. NRZ serial receive data.
RXC	I/O	RECEIVE CLOCK. Normally not used. A synchronous 10 MHz recovered clock with the serially received data, RXD.
CRS	I/O	CARRIER SENSE. Normally not used. When asserted high, it signifies that a carrier is active in the media.

ENCODER/DECODER PIN INPUT/OUTPUT TABLE

EEDCNTL <1:0>	MODE	TXD	TXC	TXE	LOOP	RXD	RXC	CRS	COL
00	Normal	On-chip internal ENDEC is used with the 8360							
	78Q8360	ZU	ZU	ZU	ZU	ZU	ZU	ZU	ZU
01	78Q8360	On-chip internal ENDEC is used with the 8360							
	Monitor	O	O	O	O	O	O	O	O
10	External	External ENDEC is used with the 8360, internal ENDEC is off							
	ENDEC	O	I	O	O	I	I	I	I
11	ENDEC	On-chip internal ENDEC is used only, the 8360 controller is off							
	Test	I	O	I	I	O	O	O	O

ZU: High impedance with internal pull-up

PIN DESCRIPTION (continued)

DEVICE POWER

NAME	TYPE	DESCRIPTION
VDD	P	POWER SUPPLY. A +5V DC (±5%) supply is required.
GND	P	SYSTEM GROUND.
AVDD	P	ANALOG VDD. The analog VDD pin required by the internal encoder/decoder is to be connected to a different VDD path from the digital VDD. A +5V DC (±5%) supply is required.
AGND	P	ANALOG GROUND. The analog ground required by the internal encoder/ decoder is to be connected to a separate GND path from the digital GND.

CRYSTAL OSCILLATOR

OSCI	I	OSCILLATOR IN. Connection for one side of the 20 MHz crystal or an input for an external 20 MHz clock source.
OSCO	O	OSCILLATOR OUT. Connection for other side of the 20 MHz crystal. Left unconnected if an external clock is used.

MISCELLANEOUS

CB	O	CONTROL BIT. A complement of the internal register bit, DLCR4 <2>, which is used to activate any external hardware.
RRST	O	REMOTE RESET. This pin follows the RMTRST register bit (DLCR1 <4>). The RMTRST bit is '1' only if a packet with the pattern 0900H in the Type Field is detected and ENA_RMTRST (DLCR5 <2>) is activated. This feature can be used by the nodes on the network to remotely-control external hardware.
CK20	O	20 MHz CLOCK: A 20 MHz free-running buffered clock output provided by the crystal oscillator circuit.

SSI 78Q8360 Ethernet Controller/ ENDEC Combo

CONTROL AND STATUS REGISTERS

The registers in the 8360 can be divided into 5 groups: the Data Link Control Registers (DLCR0-7), Node ID registers (IDR8-13), Time Domain Reflectometry Registers (TDR14-15), Hash Table Registers (HTR8-15) and Buffer Memory Registers (BMR8-15).

The Data Link Control Registers contain the transmit and receive status information, interrupt enable, 8360 setup and software reset bit (DLCR6<7>). They are accessed through direct register addresses xxx0H through xxx7H. The Ethernet Node ID is stored in IDR 8-15. The TDR14-15 registers are used to provide the count value of the number of bits transmitted for each packet. This value can indicate whether a packet has completed its transmission or has encountered a collision. Both the Node ID and the Time Domain Reflectometry Registers can be accessed through direct register addresses xxx8H through xxxFH.

The Hash Table Registers (HTR8-15) provide a means for filtering incoming multicast packets. Any packet that does not match the hash table coding will be rejected. The HTR8-15 can be accessed by the bank-switching addresses RBNK<1:0> (DLCR7 <3:2>).

The final group of the registers belongs to the Buffer Memory Registers (BMR8-15). The tasks performed by these registers include transferring of packets between the host and the 8360 (via BMR8-9), collision control, DMA operations and activation of the transmit operation. A summary table of the registers and their addresses are tabulated below:

RBNK<1:0>	HA3	HA2	HA1	HA0	ADDRESS	DESCRIPTION
XX	0	0	0	0	DLCR0	Transmit Status
XX	0	0	0	1	DLCR1	Receive Status
XX	0	0	1	0	DLCR2	Transmit Interrupt Mask
XX	0	0	1	1	DLCR3	Receive Interrupt Mask
XX	0	1	0	0	DLCR4	Transmit Mode
XX	0	1	0	1	DLCR5	Receive Mode
XX	0	1	1	0	DLCR6	Configuration 1
XX	o	1	1	1	DLCR7	Configuration 2
00	1	0	0	0	IDR8	NODE ID 0
00	1	0	0	1	IDR9	NODE ID 1
00	1	0	1	0	IDR 10	NODE ID 2
00	1	0	1	1	IDR11	NODE ID 3
00	1	1	0	0	IDR12	NODE ID 4
00	1	1	0	1	IDR13	NODE ID 5
00	1	1	1	0	TDR14	TDR 0 (LSB)
00	1	1	1	1	TDR15	TDR 1 (MSB)

CONTROL AND STATUS REGISTERS (continued)

RBNK<1:0>	HA3	HA2	HA1	HA0	ADDRESS	DESCRIPTION
01	1	0	0	0	HTR8	Hash Table 0
01	1	0	0	1	HTR9	Hash Table 1
01	1	0	1	0	HTR10	Hash Table 2
01	1	0	1	1	HTR11	Hash Table 3
01	1	1	0	0	HTR12	Hash Table 4
01	1	1	0	1	HTR13	Hash Table 5
01	1	1	1	0	HTR14	Hash Table 6
01	1	1	1	1	HTR15	Hash Table 7
10	1	0	0	0	BMR8	Buffer Memory I/O Port
10	1	0	0	1	BMR9	Buffer Memory I/O Port (word mode)
10	1	0	1	0	BMR10	Transmit Start + Packet Count
10	1	0	1	1	BMR11	16 Collisions Control
10	1	1	0	0	BMR12	DMA Enable
10	1	1	0	1	BMR13	DMA Burst
10	1	1	1	0	BMR14	Skip Packet
10	1	1	1	1	BMR15	Reserved
11	X	X	X	X	-	RESERVED

Note: All registers are both word and byte accessible. In word mode, register bytes are paired up. IDR and HTR can only be accessed when $\overline{\text{ENADLC}}$ (DLCR 6<7>) is a '1'. In byte mode, only BMR8 will be used.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Supply voltage, V_{DD}	-0.5 to 6.0V
Input voltage, V_{IN}	-0.5 to V_{DD} + 0.5V
Output voltage, V_{OUT}	-0.5 to V_{DD} + 0.5V
Storage temperature, T_{STG}	-55 to 150°C
Lead temperature (max 10 sec soldering), T_L	250°C max

DC CHARACTERISTICS

(TA = 0°C to +70°C, V_{DD} = 5V ± 5%)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Low level input voltage	V_{IL}	TTL inputs	0		0.8	V
		OSCI pin	0		1.4	V
		RESET pin	0		1.2	V
High level input voltage	V_{IH}	TTL inputs	2.0		V_{DD}	V
		OSCI pin	3.2		V_{DD}	V
		RESET pin	1.8		V_{DD}	V
Low level output voltage	V_{OL}	Rated I_{OL}	0		0.4	V
		I_{OL} = 20 µA	0		0.1	V
High level output voltage	V_{OH}	Rated I_{OH}	2.4		V_{DD}	V
		I_{OH} = -20 µA	V_{DD} - 0.1		V_{DD}	V
Low level output current (1) (pin types On, IOn and IOnU)	I_{OL}	V_{OL} = 0.4V	n			mA
High level output current (1) (pin types On, IOn and IOnU)	I_{OH}	V_{OH} = 2.4V	-n			mA
Leakage current (input/output)	I_L		-10		10	µA
Supply current (2)	I_{DD}	Fully active			50	mA
		Idle			25	mA
Power down supply current (2)	I_{PWRDN}	Osc. on			5	mA
		Osc. off			1	mA

Note: (1) "n" refers to the rated output current and takes the value of 2, 4, 8, 16 depending on the pins.
(2) Inputs at VCC or GND. Fully active means 3 "simultaneous" operations: transmitting, receiving and either host write or read.

ELECTRICAL SPECIFICATIONS (continued)

AUI CHARACTERISITICS

(TA = 0 to 70 °C, VDD = 5V ±5%)
Input refers to RDP, N and CDP, N. Output refers to TDP, N.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
AC Common Mode Output Voltage V_{ACCM}				±40	mV
DC Common Mode Output Voltage V_{DCCM}		3.0	4.0	V_{DD}- 0.5	V
Differential Peak Output Voltage V_{OP}	R_{EXT} = 20 kΩ R_T = 78Ω	0.7	0.9	1.1	V
Output Current I_{OP}	R_{EXT} = 20 kΩ	9	11	13	mA
Input Squelch Threshold Voltage V_{SQ}		-140	-190	-260	mV
Open Circuit Input Bias Voltage V_{BIAS}		2.5	3.5	V_{DD}- 0.5	V

CAPACITANCE

Input pin capacitance	C_{IN}			10	pF
Output pin capacitance	C_{OUT}			10	pF
I/O pin capacitance	C_{IO}			10	pF

6

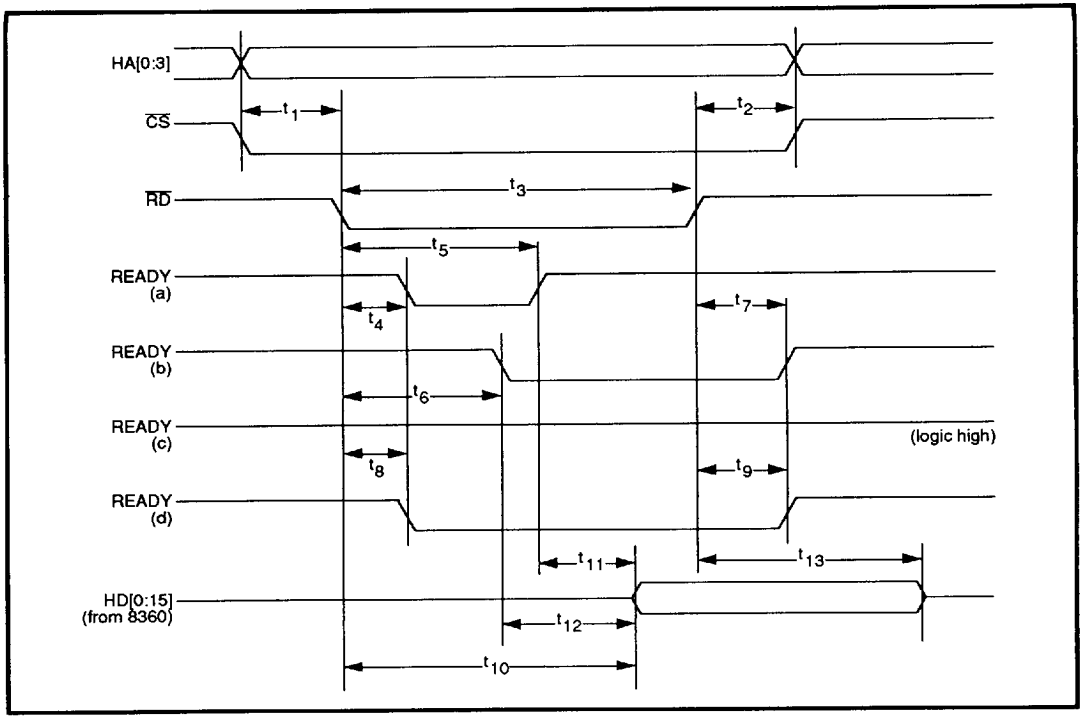

FIGURE 3: Read Cycle

TABLE 1: Read Cycle

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{CS}$ low to $\overline{RD}$ low; HA[0:3] valid to $\overline{RD}$ low	t_1		0			ns
$\overline{RD}$ high to $\overline{CS}$ high; $\overline{RD}$ high to HA[0:3] invalid	t_2		0			ns
$\overline{RD}$ low pulse width	t_3		30			ns
$\overline{RD}$ low to READY low	t_4	(a)	0		35	ns
$\overline{RD}$ low to READY high (1)	t_5	(a)			400	ns
$\overline{RD}$ low to READY low (1)	t_6	(b)	0		400	ns
$\overline{RD}$ high to READY high	t_7	(b)	0		25	ns
$\overline{RD}$ low to READY low	t_8	(d)	0		25	ns
$\overline{RD}$ high to READY high	t_9	(d)	0		25	ns
$\overline{RD}$ low to HD[0:15] valid	t_{10}	Register access			45	ns
READY high to HD[0:15] valid	t_{11}	Port access			0	ns
READY low to HD[0:15] valid	t_{12}	Port access			0	ns
$\overline{RD}$ high to HD[0:15] invalid (data hold)	t_{13}		10			ns

Note: (1) Maximum of 400 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active in "loopback" reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 µs max for host read error.
(a) For Buffer Memory Port when port is busy and RDYSEL = 1.
(b) For Buffer Memory Port when port is busy and RDYSEL = 0.
(c) For register or port is not busy and RDYSEL = 1.
(d) For register or port is not busy and RDYSEL = 0.

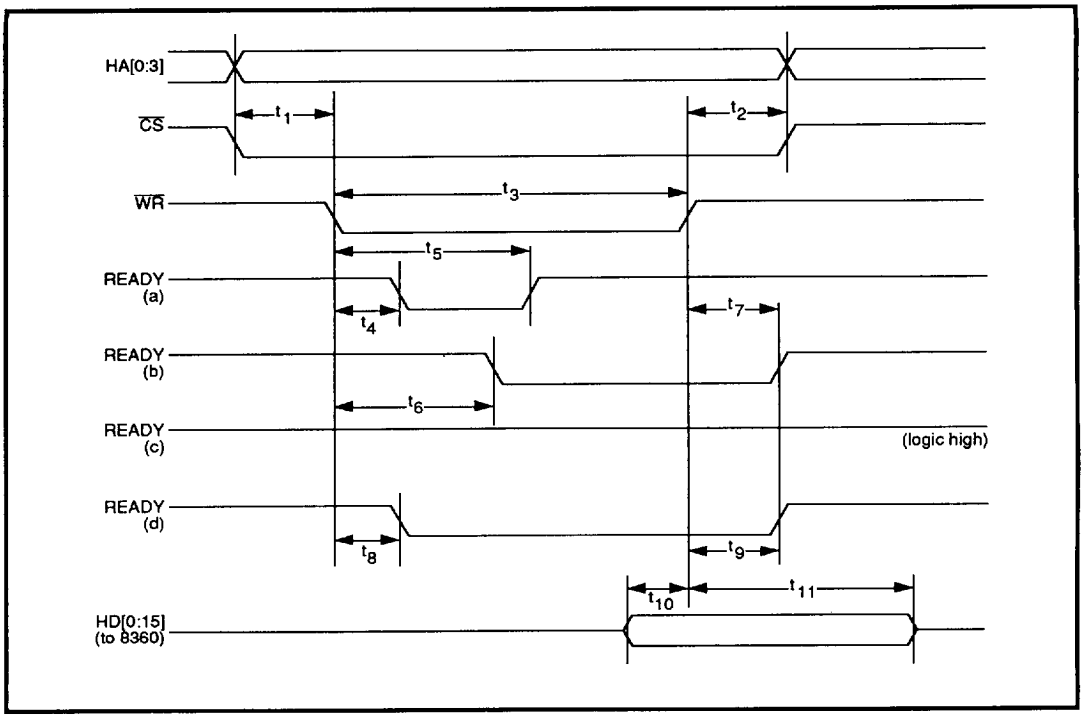

FIGURE 4: Write Cycle

TABLE 2: Write Cycle

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{CS}$ low to $\overline{WR}$ low; HA[0:3] valid to $\overline{WR}$ low	t_1		0			ns
$\overline{WR}$ high to $\overline{CS}$ high; $\overline{WR}$ high to HA[0:3] invalid	t_2		0			ns
$\overline{WR}$ low pulse width	t_3		30			ns
$\overline{WR}$ low to READY low	t_4	(a)	0		35	ns
$\overline{WR}$ low to READY high (1)	t_5	(a)			400	ns
$\overline{WR}$ low to READY low (1)	t_6	(b)	0		400	ns
$\overline{WR}$ high to READY high	t_7	(b)			25	ns
$\overline{WR}$ low to READY low	t_8	(d)	0		25	ns
$\overline{WR}$ high to READY high	t_9	(d)	0		25	ns
HD[0:15] valid to $\overline{WR}$ high (data setup)	t_{10}		15			ns
$\overline{WR}$ high to HD[0:15] invalid (data hold)	t_{11}		10			ns

Note: (1) Maximum of 400 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active on "loopback" reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 µs max for host write error.
(a) For Buffer Memory Port when port is busy and RDYSEL = 1.
(b) For Buffer Memory Port when port is busy and RDYSEL = 0.
(c) For register or port is not busy and RDYSEL = 1.
(d) For register or port is not busy and RDYSEL = 0.

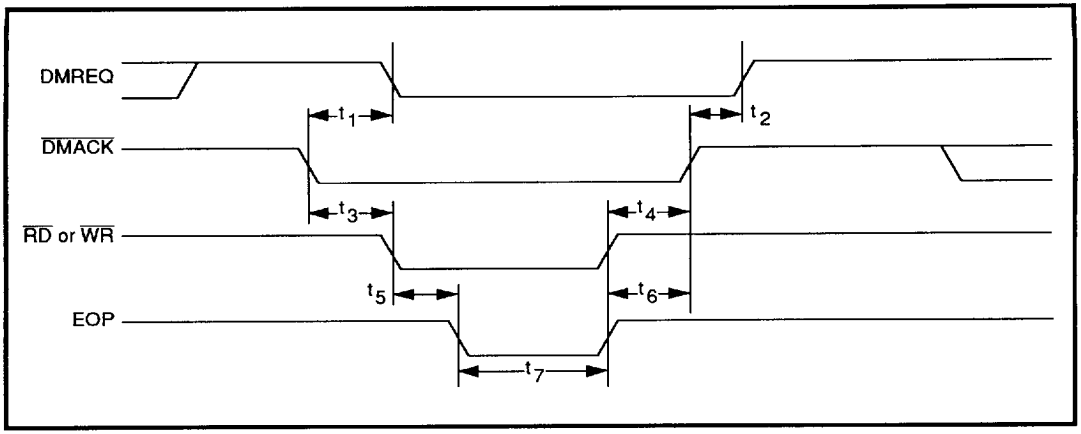

FIGURE 5: Single-Cycle DMA Timing

TABLE 3: Single-Cycle DMA Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{DMACK}$ low to DMREQ low	t_1		0		20	ns
$\overline{DMACK}$ high to DMREQ high	t_2		0		20	ns
$\overline{DMACK}$ low to $\overline{RD}$ or $\overline{WR}$ low	t_3		0			ns
$\overline{RD}$ or $\overline{WR}$ high to $\overline{DMACK}$ high	t_4		0			ns
$\overline{RD}$ or $\overline{WR}$ low to EOP low	t_5		0			ns
EOP high to $\overline{DMACK}$ high	t_6		0			ns
EOP low pulse width	t_7		10			ns

Note: (1) An asserted EOP terminates any further DMREQ after $\overline{DMACK}$ returns high.
(2) The DMA cycle uses $\overline{DMACK}$ as the chip select. $\overline{DMACK}$ overrides $\overline{CS}$ and HA[0:3] if they are both asserted at the same time, forcing selection of the Buffer Memory Port as in a DMA cycle.
(3) For READY timing and HD[0:15] timing, see Figure 3, t_4-t_{13}, and Figure 4, t_4-t_{11}.

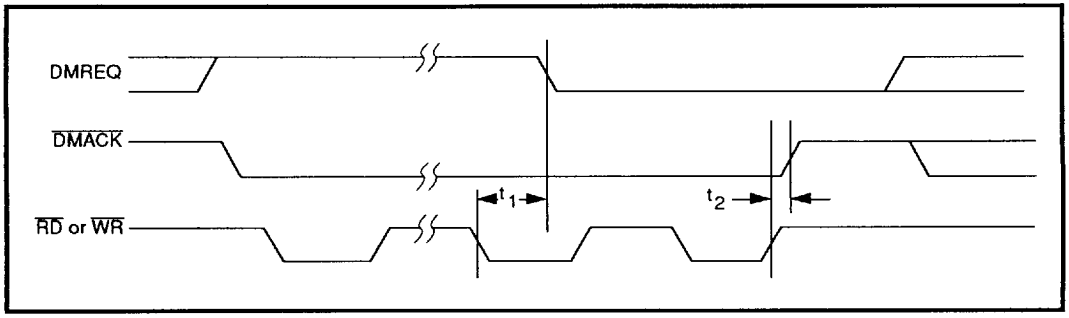

FIGURE 6: Burst DMA Timing

TABLE 4: Burst DMA Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{RD}$ or $\overline{WR}$ low to DMREQ low t_1				30	ns
$\overline{RD}$ or $\overline{WR}$ high to $\overline{DMACK}$ high t_2		0			ns

Note: (1) DMREQ goes low during the next-to-last transfer of the burst. $\overline{DMACK}$ should not go high until after the $\overline{RD}$ or $\overline{WR}$ pulse of the last transfer cycle goes high
(2) The DMA cycle uses $\overline{DMACK}$ as the chip select. $\overline{DMACK}$ overrides $\overline{CS}$ and HA[0:3] if they are both asserted at the same time, forcing selection of the Buffer Memory Port as in a DMA cycle.
(3) For READY timing and HD[0:15] timing, see Figure 3, t_4-t_{13}, and Figure 4, t_4-t_{11}.

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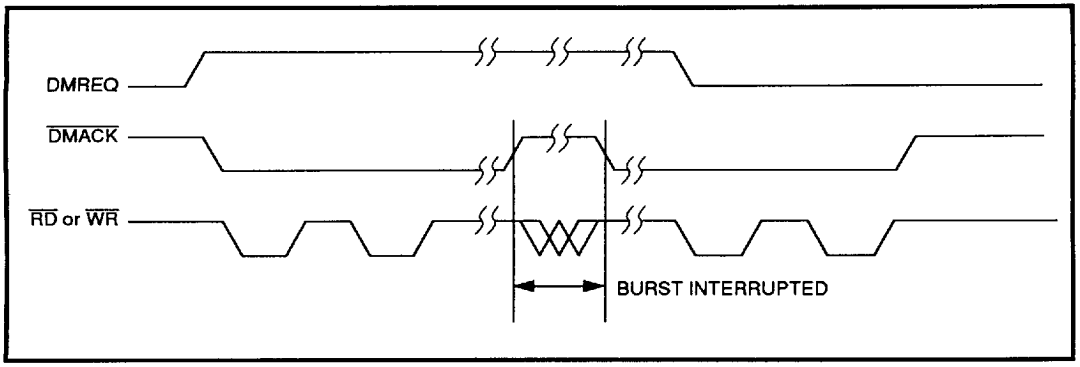

FIGURE 7: Burst DMA Interrupted by DMACK

Note: Burst can be interrupted by DMACK high-going pulse during the burst. Burst will resume when DMACK returns low.

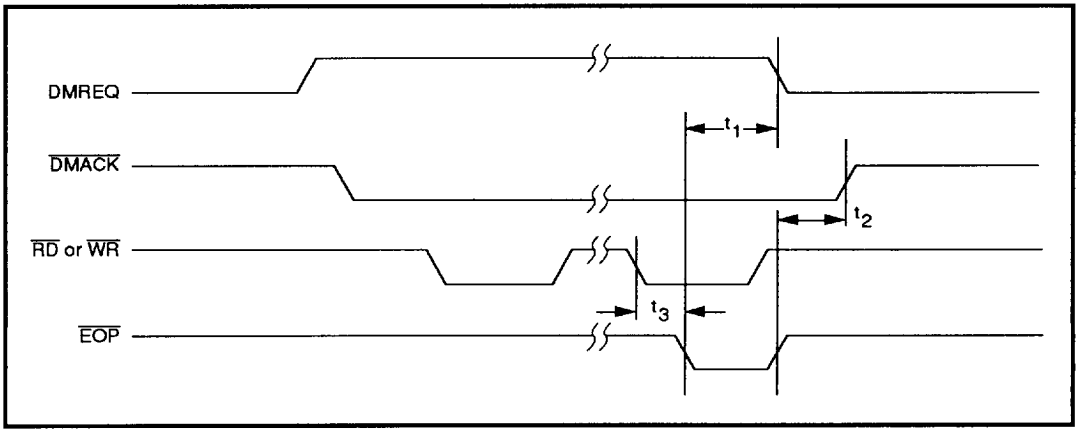

FIGURE 8: Burst DMA Terminated by EOP

TABLE 5: Burst DMA Terminated by EOP

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
EOP low to DMREQ low	t_1		4		28	ns
EOP high to DMACK high	t_2		3			ns
RD or WR low to EOP low	t_3		0			ns

Note: EOP can be asserted during any transfer of the burst to terminate the process following that transfer.

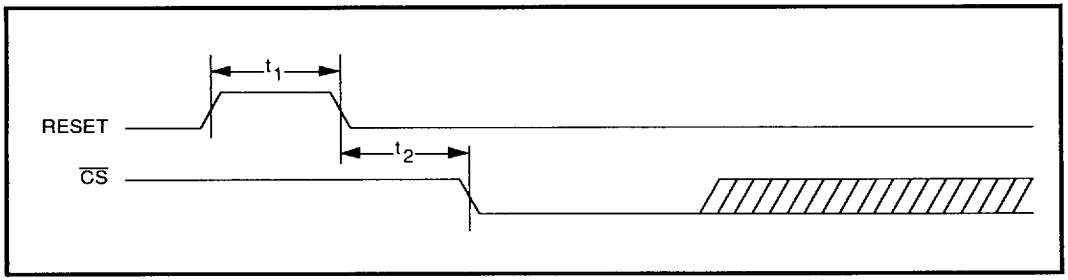

FIGURE 9: RESET Timing

TABLE 6: RESET Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
RESET pulse width	t_1		200			ns
RESET low to first $\overline{CS}$ low	t_2		300			ns

Note: Before enabling transmit and receive functions ($\overline{ENADLC}$), wait 10 µs after reset pulse for internal calibration of DPLL.

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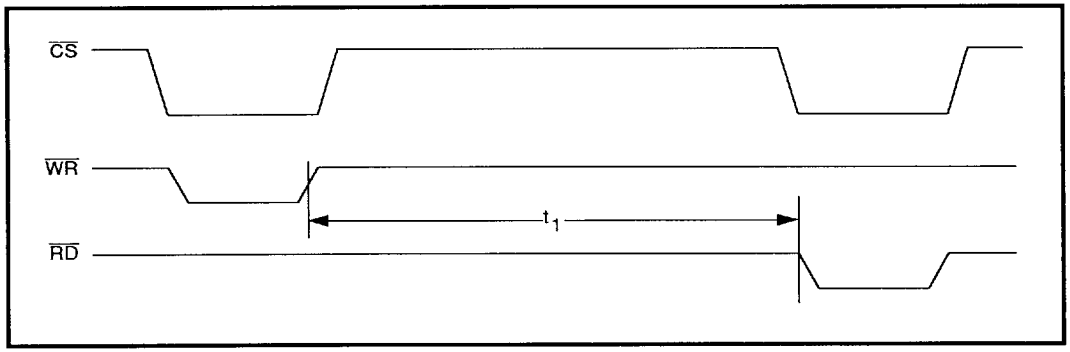

FIGURE 10: Skip Packet Timing

TABLE 7: Skip Packet Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Writing Skip Packet high to next Buffer Memory Port read t_1		200			ns

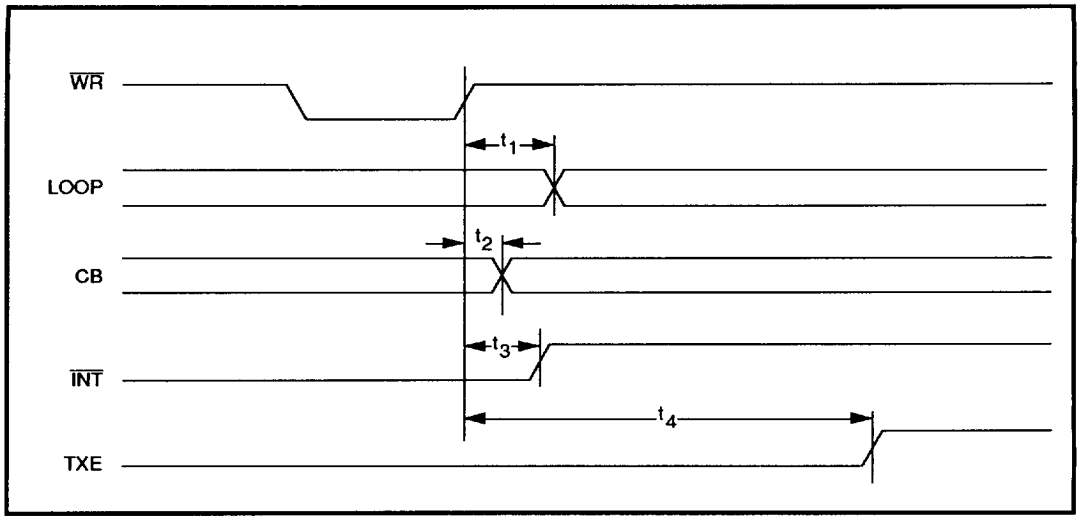

FIGURE 11: LOOP, CB and $\overline{INT}$ Timing

TABLE 8: LOOP, CB and $\overline{INT}$ Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Loopback Control (LOOP) delay	t_1		5		30	ns
CB delay	t_2		5		30	ns
$\overline{INT}$ signal clearing delay	t_3		7		40	ns
Transmit enable delay after setting TXST high	t_4	Network free and 8360 idle			1	µs

Note: TXST is BMR10<7>

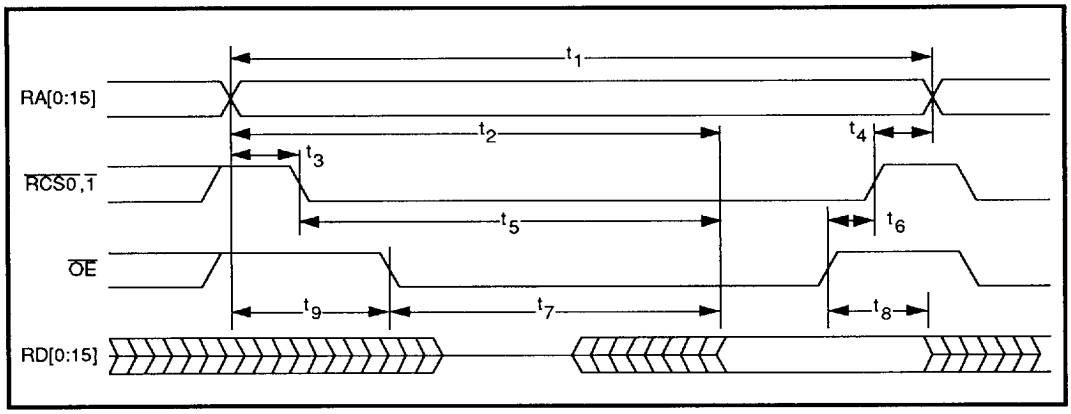

FIGURE 12: SRAM Read Timing

TABLE 9: SRAM Read Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Read cycle	t_1	RAMSP = 1	95			ns
		RAMSP = 0	145			ns
Address access time	t_2	RAMSP = 1			80	ns
		RAMSP = 0			130	ns
Address valid to $\overline{RCS0,1}$ low	t_3		0		5	ns
$\overline{RCS0,1}$ high to address invalid	t_4		0			ns
Chip select access time	t_5	RAMSP = 1			80	ns
		RAMSP = 0			130	ns
$\overline{OE}$ high to $\overline{RCS0,1}$ high	t_6		0		2	ns
Output enable access time	t_7				50	ns
Data hold time	t_8		0			ns
Address valid to $\overline{OE}$ low	t_9				30	ns

Note: Use SRAM with address access time of 80 ns or less for RAMSP = 1 and 130 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

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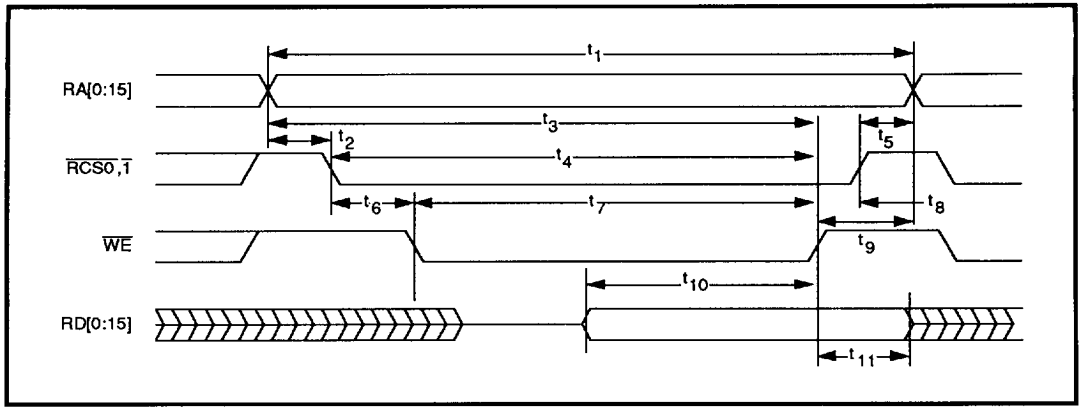

FIGURE 13: SRAM Write Timing

TABLE 10: SRAM Write Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Write Cycle	t_1	RAMSP = 1	95			ns
		RAMSP= 0	145			ns
Address Valid to $\overline{RCS0,1}$ low	t_2		0		5	ns
Address Valid to $\overline{WE}$ high	t_3	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RCS0,1}$ low to $\overline{WE}$ high	t_4	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RCS0,1}$ high to Address Invalid	t_5		0			ns
$\overline{RCS0,1}$ low to $\overline{WE}$ low	t_6		0			ns
$\overline{WE}$ Pulse Width	t_7	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{WE}$ high to $\overline{RCS0,1}$ high	t_8		0			ns
$\overline{WE}$ high to Address Invalid	t_9		20			ns
Data Setup Time	t_{10}		40			ns
Data Hold Time	t_{11}		20			ns

Note: Use SRAM with address access time of 80 ns or less for RAMSP = 1 and 130 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

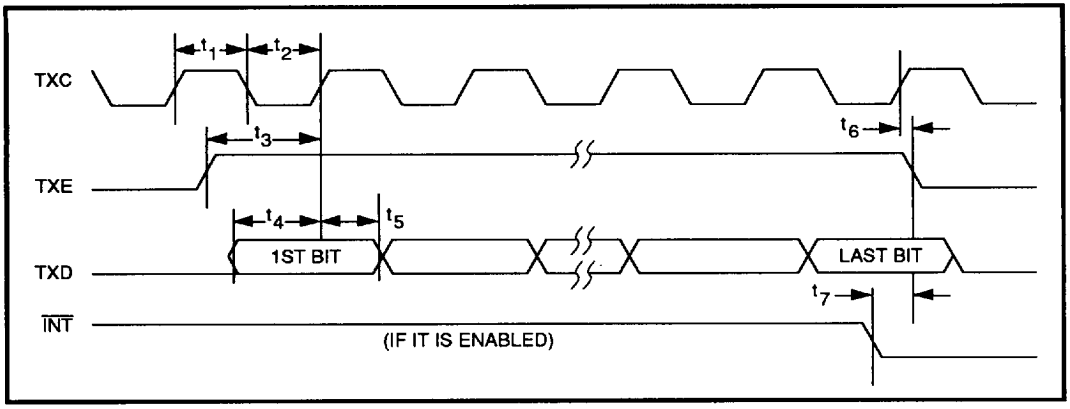

FIGURE 14: Transmit Timing

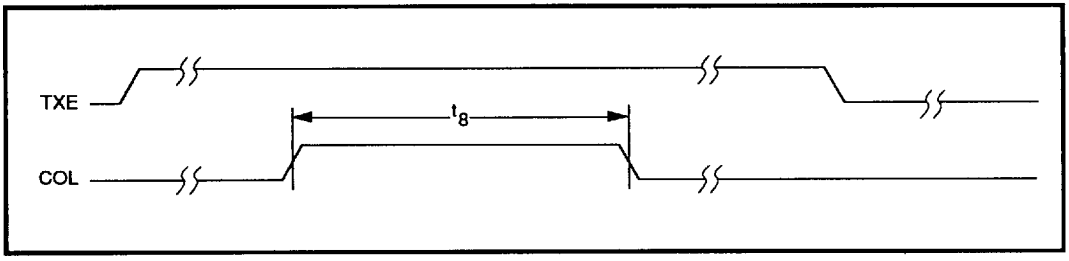

FIGURE 15: Transmit Timing

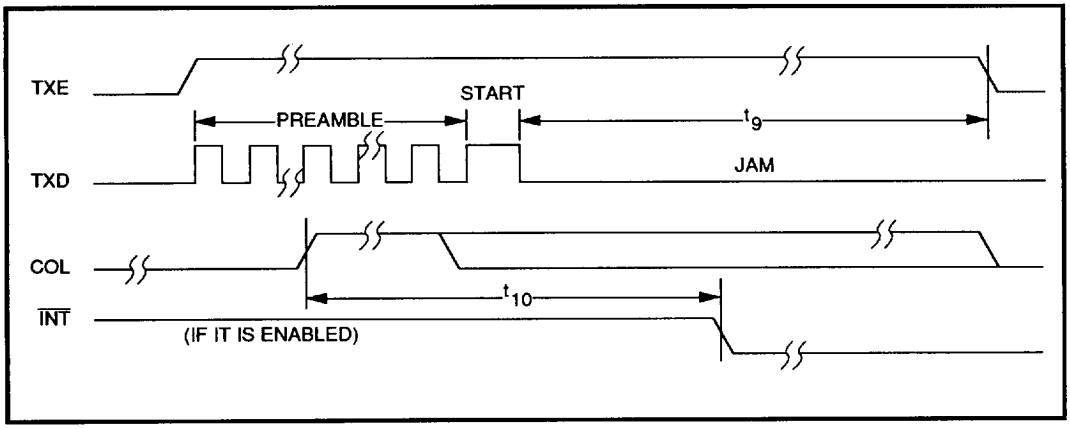

FIGURE 16: Transmit Timing

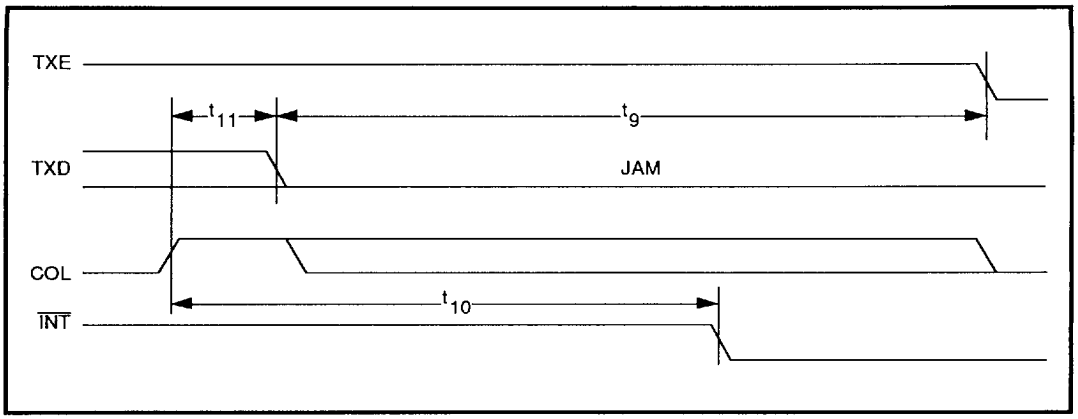

FIGURE 17: Transmit Timing

TABLE 11: Transmit Timing: Figure 14-17 (for external Encoder/Decoder mode)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Transmit clock high width	t_1		45	50	55	ns
Transmit clock low width	t_2		45	50	55	ns
TXE high to TXC high	t_3		65	-	-	ns
Transmit data setup	t_4		55	-	-	ns
Transmit data hold	t_5		5	-	-	ns
TXC high to TXE low	t_6		-	-	35	ns
Transmit interrupt low to transmit enable low	t_7		-	1	-	TXC cycles
Minimum collision length	t_8		200	-	-	ns
Jam period (1)	t_9		-	32	-	TXC cycles
Transmit interrupt from collision	t_{10}		-	-	5	TXC cycles
Collision at data field to first jam bit	t_{11}		-	-	5	TXC cycles

Note: (1) The 32 jam bits consists of all zeroes.

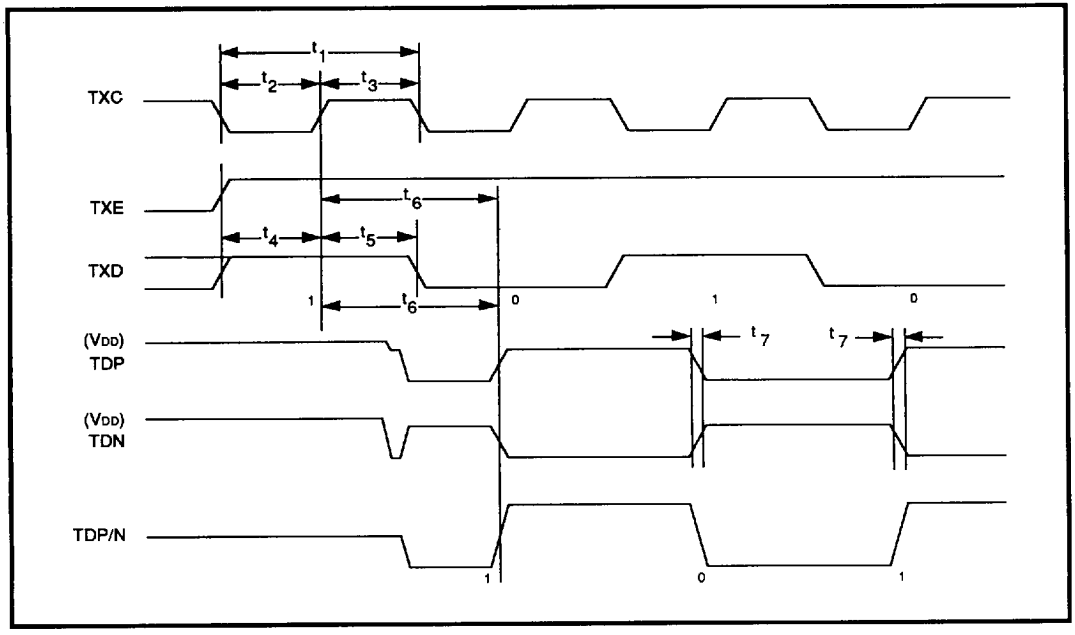

FIGURE 18: Transmit Start Timing

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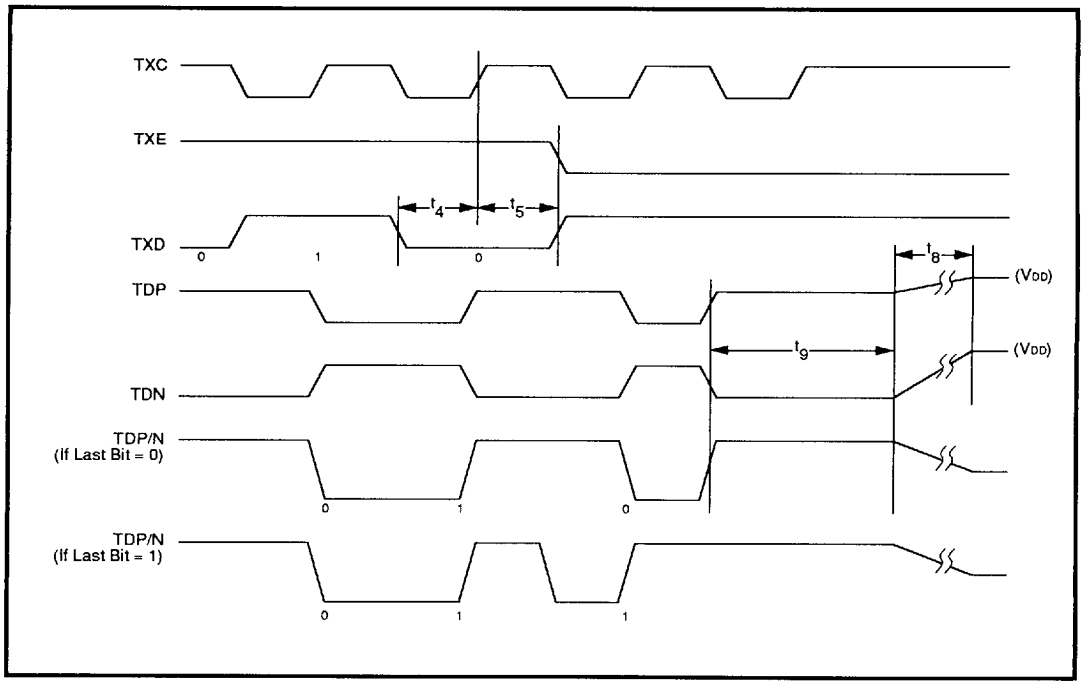

FIGURE 19: Transmit End Timing

TABLE 12: Transmit Start and End Timing: Figure 18-19 (for Encoder/Decoder Test mode)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TXC cycle time	t_1		99.99	100	100.01	ns
TXC high width	t_2		40	50	60	ns
TXC low width	t_3		40	50	60	ns
TXD, TXE setup time to TXC	t_4		-	30	-	ns
TXD, TXE hold time from TXC	t_5		-	20	-	ns
TDP/N encode time	t_6		-	90	-	ns
TDP,N fall/rise time	t_7	20% to 80%, REXT = 20 kΩ, R_T = 78Ω	-	2	-	ns
TDP/N line voltage transition	t_8		-	-	8	µs
TDP/N end-of-packet delimiter	t_9		200	-	-	ns

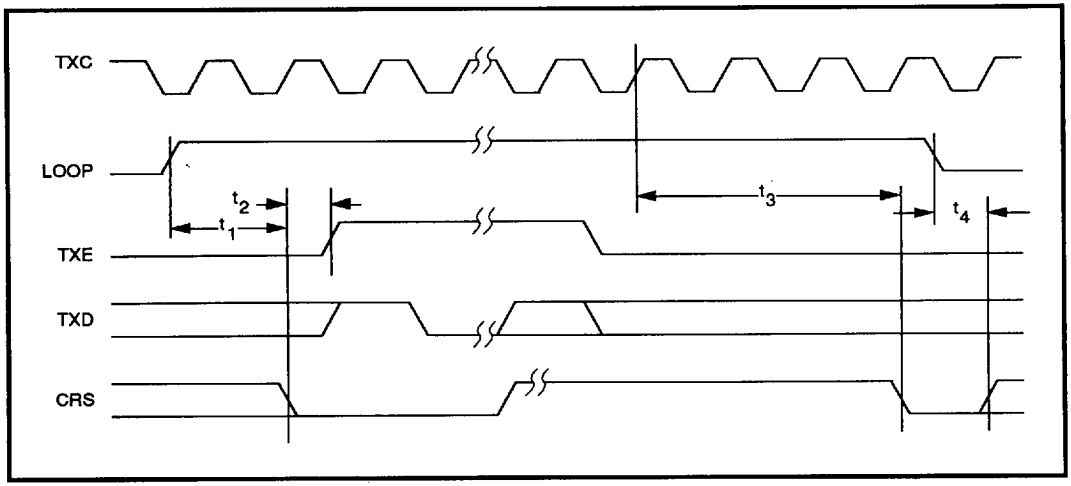

FIGURE 20: Loopback Timing

TABLE 13: Loopback Timing (for Encoder/Decoder test mode)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Loop receiving data purge time t_1		-	180	-	ns
Wait time from CRS low to TXE high t_2		9.6	-	-	µs
Data through time t_3		-	190	-	ns
Loop receiving data accept time t_4		-	30	-	ns

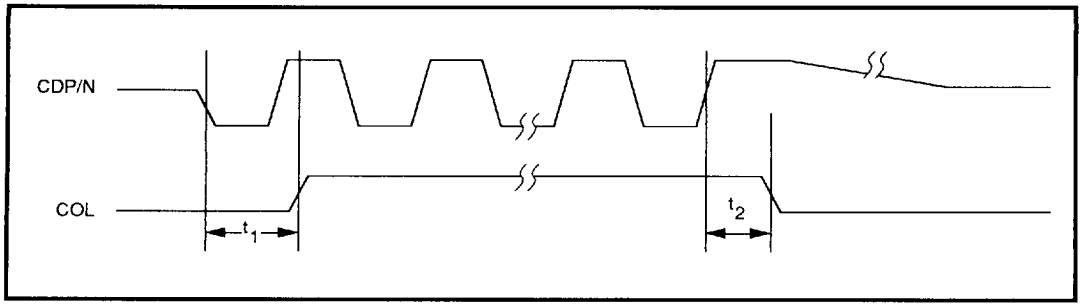

FIGURE 21: Collision Timing

TABLE 14: Collision Timing (for Encoder/Decoder Test mode)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
COL on delay time	t_1		–	40	50	ns
COL off delay time	t_2		–	270	300	ns

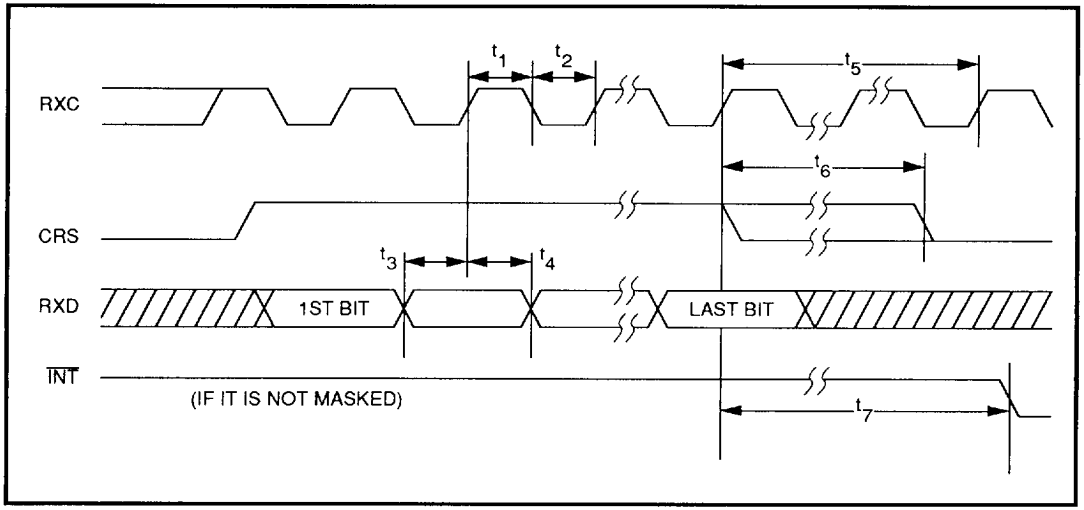

FIGURE 22: Receive Timing

TABLE 15: Receive Timing (for external Encoder/Decoder mode)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Receive clock high width	t_1		40			ns
Receive clock low width	t_2		40			ns
Receive data and carrier sense setup	t_3		20			ns
Receive data and carrier sense hold	t_4		20			ns
Number of RXC cycles after last bit	t_5		1			RXC cycles
Receive carrier sense drop after last bit	t_6				7	RXC cycles
Last bit of packet received to interrupt	t_7	Good packet			8	RXC cycles
		Bad packet			2	RXC cycles

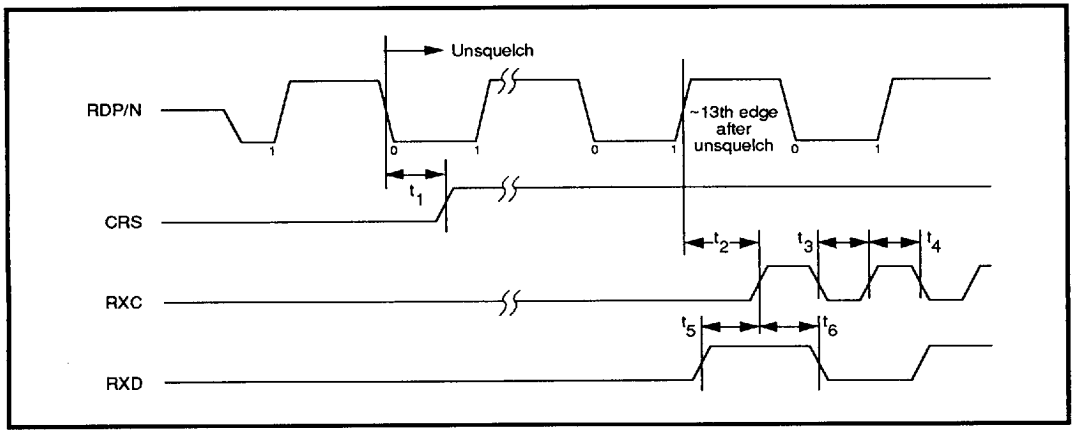

FIGURE 23: Receive Start Timing

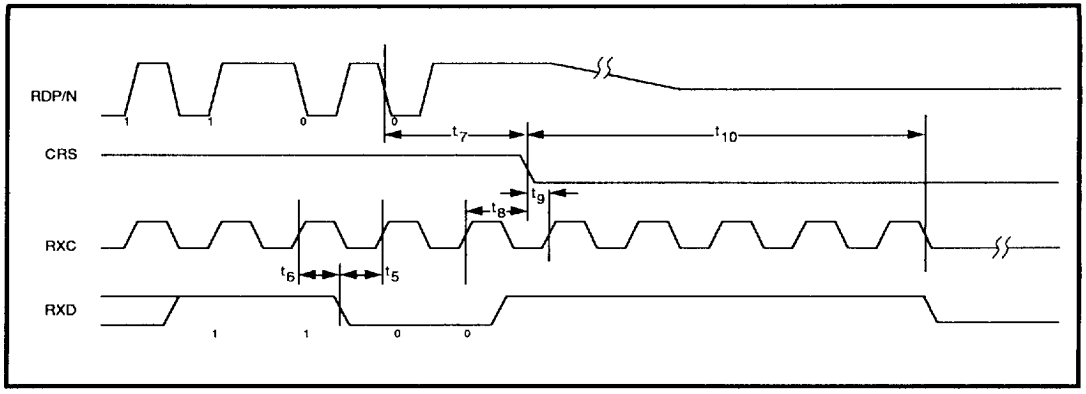

FIGURE 24: Receive End Timing

TABLE 16: Receive Timing: Figure 23-24 (for Encoder/Decoder Test mode)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
CRS on delay time	t_1		-	150	220	ns
RXC delay time	t_2		-	170	-	ns
RXC low time	t_3		35	50	-	ns
RXC high time	t_4		35	50	-	ns
RXD setup time to RXC	t_5		40	50	-	ns
RXD hold time from RXC	t_6		40	50	-	ns
CRS off delay time	t_7		-	220	-	ns
CRS high hold time	t_8		-	50	-	ns
CRS low setup time	t_9		-	50	-	ns
Number of RXC cycles after last bit	t_{10}		5	5	5	cycles

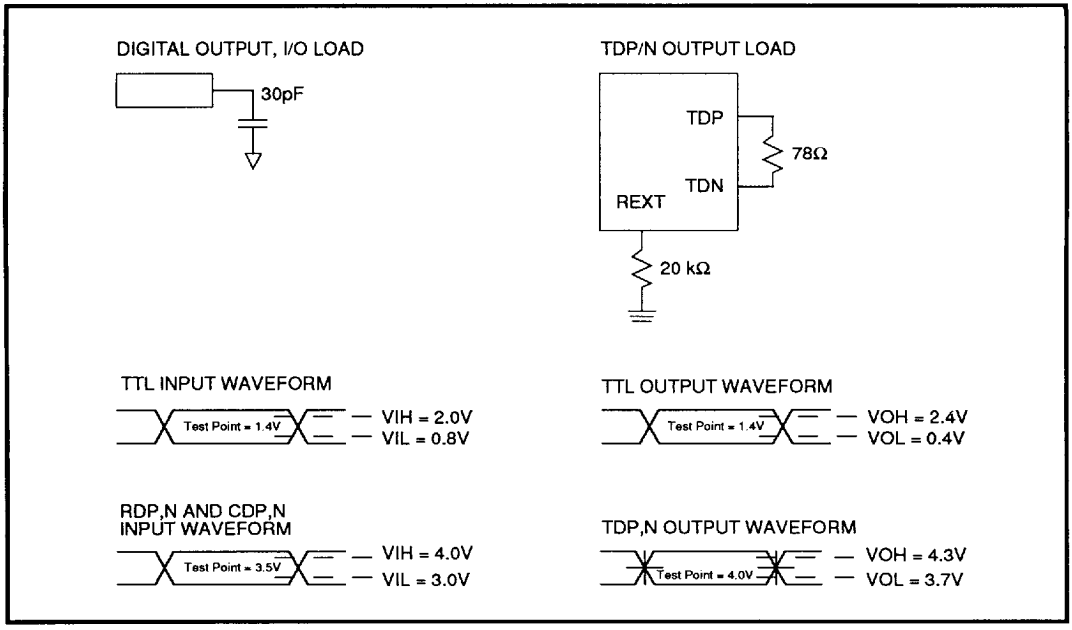

FIGURE 25: Test Conditions

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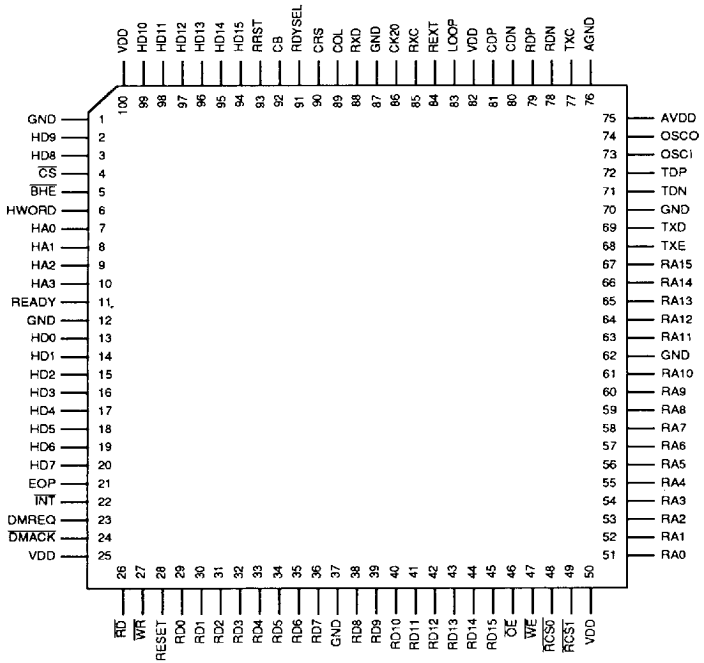
PACKAGE PIN DESIGNATIONS

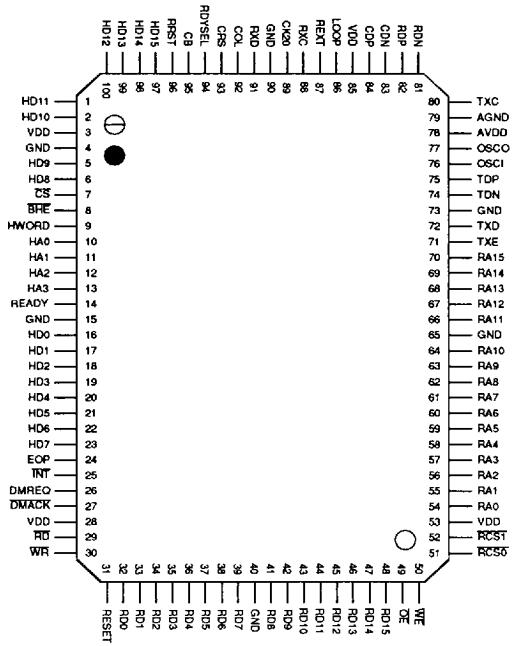
(Top View)



100-Lead TQFP

PACKAGE PIN DESIGNATIONS

(Top View)



100-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 78Q8360 - Ethernet Controller/ ENDEC Combo	100-pin QFP	78Q8360-CG	78Q8360-CG
	100-pin TQFP	78Q8360-CGT	78Q8360-CGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

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