REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
C	Converted to military drawing format. Add vendor CAGE number 50088 as second source. Changed Code Ident. No. to 67268.	7 NOV 87	[illegible signature]

CURRENT CAGE CODE 67268

REV	C	C	C	C
PAGE	24	25	26	27

REV STATUS OF PAGES																								
	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing: 1 August 1984

AMSC N/A

PREPARED BY James E. Jamison

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APPROVED BY [illegible signature]

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, FOUR BIT MICROPROCESSOR SLICE MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	14933	84057

REV C

5962-E631

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

84057	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2901C	Four-bit microprocessor slice

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 9/16" x 2 1/16"), dual-in-line package
Z	See figure 1 (42-lead, 5/8" x 1 1/16"), flat package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc at -12 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	1.6 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q	See MIL-M-38510, appendix C
Case Z	9°C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must witnstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 3.

3.2.3 Block diagram. The block diagram shall be as specified on figure 4.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$			Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage	V_{OH1}	V_{CC} = 4.5 V, V_{IN} = 2.0 V, 0.8 V		I_{OH} = -1.6 mA Y_0, Y_1, Y_2, Y_3	1,2,3	2.4		V
	V_{OH3}			I_{OH} = -1.0 mA, C_{n+4}		2.4		
	V_{OH2}			I_{OH} = -800 µA, OVR, $\overline{P}$		2.4		
	V_{OH4}			I_{OH} = -600 µA, F_3		2.4		
	V_{OH4}			I_{OH} = -600 µA $RAM_{0,3}$, $Q_{0,3}$		2.4		
	V_{OH1}			I_{OH} = -1.6 mA, $\overline{G}$		2.4		
Output leakage current for F = 0 output	I_{CEX}	V_{CC} = 4.5 V, V_{OH} = 5.5 V, V_{IN} = 2.0 V, 0.8 V					250	µA
Low level output voltage	V_{OL1}	V_{CC} = 4.5 V, V_{IN} = 2.0 V, 0.8 V	F = 0	I_{OL} = 16 mA			0.5	V
	V_{OL1}		Y_0, Y_1, Y_2, Y_3	I_{OL} = 16 mA			0.5	
	V_{OL1}		$\overline{G}$	I_{OL} = 16 mA			0.5	
	V_{OL3}		C_{n+4}	I_{OL} = 10 mA			0.5	
	V_{OL2}		OVR, $\overline{P}$	I_{OL} = 8.0 mA			0.5	
	V_{OL4}		F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0 mA			0.5	
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA					-1.5	V

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$			Group A subgroups	Limits Min	Limits Max	Unit
Low level input current	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.5 V		Clock, $\overline{OE}$	1,2,3		-0.36	mA
	I_{IL2}			A_0, A_1, A_2, A_3, Clock			-0.36	
				B_0, B_1, B_2, B_3			-0.36	
	I_{IL3}			D_0, D_1, D_2, D_3			-0.72	
	I_{IL1}			I_0, I_1, I_2, I_6, I_8			-0.36	
	I_{IL4}			I_3, I_4, I_5, I_7			-0.72	
	I_{IL5}			$RAM_{0,3}, Q_{0,3}$ 1/			-0.8	
	I_{IL6}			C_n			-3.6	
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		Clock, $\overline{OE}$			20	µA
				A_0, A_1, A_2, A_3			20	
				B_0, B_1, B_2, B_3			20	
	I_{IH2}			D_0, D_1, D_2, D_3			40	
	I_{IH1}			I_0, I_1, I_2, I_6, I_8			20	
	I_{IH2}			I_3, I_4, I_5, I_7			40	
	I_{IH3}			$RAM_{0,3}, Q_{0,3}$ 1/			100	
	I_{IH4}			C_n			200	
High impedance state output current	I_{ZH1}	V_{CC} = 5.5 V	Y_0, Y_1, Y_2, Y_3	V_O = 2.4 V			50	µA
	I_{ZL1}			V_O = 0.5 V			-50	
	I_{ZH2}		$RAM_{0,3}$ $Q_{0,3}$	V_O = 2.4 V 1/			100	
	I_{ZL2}			V_O = 0.5 V 1/			-800	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$		Group A subgroups	Limits Min	Limits Max	Unit
Output short circuit current 2/	I_{OS}	V_{CC} = 5.5 V, V_O = 0 V	Y_0, Y_1, Y_2 Y_3, $\overline{G}$	1,2,3	-30	-85	mA
			C_{n+4}		-30	-85	
			OVR, $\overline{P}$		-30	-85	
			F_3		-30	-85	
			$RAM_{0,3}$, $Q_{0,3}$		-30	-85	
Power supply current	I_{CC}	V_{CC} = 5.5 V				280	mA
Frequency of operation	f_{MAX}				31		MHz
A_3-A_0 setup time to positive edge of clock	t_{SHL1}	C_L = 50 ±5 pF all outputs (see figure 5)		9,10,11	30		ns
	t_{SLH1}				30		ns
A_3-A_0 setup time to negative edge of clock	t_{SHL2}				15		ns
	t_{SLH2}				15		ns
B_3-B_0 (source) setup time to position edge of clock	t_{SHL3}				30		ns
	t_{SLH3}				30		ns
B_3-B_0 (source) setup time to negative edge of clock	t_{SHL4}				15		ns
	t_{SLH4}				15		ns
B_3-B_0 (DEST) setup time to negative edge of clock	t_{SHL5}				15		ns
	t_{SLH5}				15		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$	Group A subgroups	Limits Min	Limits Max	Unit
D_3-D_0 (arithmetic mode) setup time to positive edge of clock	t_{SHL6}	C_L = 50 ±5 pF all outputs (see figure 5)	9,10,11	25		ns
	t_{SLH6}			25		ns
D_3-D_0 (I = X37) setup time to positive edge of clock	t_{SHL7}			25		ns
	t_{SLH7}			25		ns
C_n setup time to positive edge of clock	t_{SHL8}			20		ns
	t_{SLH8}			20		ns
I_2-I_0 setup time to positive edge of clock	t_{SHL9}			30		ns
	t_{SLH9}			30		ns
I_5-I_3 setup time to positive edge of clock	t_{SHL10}			30		ns
	t_{SLH10}			30		ns
I_8-I_6 setup time to negative edge of clock	t_{SHL11}			10		ns
	t_{SLH11}			10		ns
Q_3,Q_0 setup time to positive edge of clock	t_{SHL12}			12		ns
	t_{SLH12}			12		ns
RAM_3, RAM_0 setup time to positive edge of clock	t_{SHL13}			12		ns
	t_{SLH13}			12		ns
A_3-A_0 hold time from positive edge of clock	t_{HHL1}			2		ns
	t_{HLH1}			2		ns
B_3-B_0 hold time from positive edge of clock	t_{HHL2}			2		ns
	t_{HLH2}			2		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 3/	Group A subgroups	Limits Min	Limits Max	Unit
D_3-D_0 hold time from positive edge of clock	t_{HHL3}	C_L = 50 ±5 pF all outputs (see figure 5)	9,10,11	0		ns
	t_{HLH3}			0		ns
C_n hold time from positive edge of clock	t_{HHL4}			0		ns
	t_{HLH4}			0		ns
I_8-I_0 hold time from positive edge of clock	t_{HHL5}			0		ns
	t_{HLH5}			0		ns
Q_3,Q_0 hold time from positive edge of clock	t_{HHL6}			0		ns
	t_{HLH6}			0		ns
RAM_3,RAM_0 hold time from positive edge of clock	t_{HHL7}			0		ns
	t_{HLH7}			0		ns
Delay from A_3-A_0 to Y_3-Y_0	t_{PHL1}				48	ns
	t_{PLH1}				48	ns
Delay from A_3-A_0 to F_3	t_{PHL2}				48	ns
	t_{PLH2}				48	ns
Delay from A_3-A_0 to C_{n+4}	t_{PHL3}				48	ns
	t_{PLH3}				48	ns
Delay from A_3-A_0 to $\overline{G}$ and $\overline{P}$	t_{PHL4}				44	ns
	t_{PLH4}				44	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 3/	Group A subgroups	Limits Min	Limits Max	Unit
Delay from A_3-A_0 to F = 0	t_{PHL5}	C_L = 50 ±5 pF all outputs (see figure 5)	9,10,11		48	ns
	t_{PLH5}				48	ns
Delay from A_3-A_0 to OVR	t_{PHL6}				48	ns
	t_{PLH6}				48	ns
Delay from A_3-A_0 to RAM_3 and RAM_0	t_{PHL7}				48	ns
	t_{PLH7}				48	ns
Delay from B_3-B_0 to Y_3-Y_0	t_{PHL8}				48	ns
	t_{PLH8}				48	ns
Delay from B_3-B_0 to F_3	t_{PHL9}				48	ns
	t_{PLH9}				48	ns
Delay from B_3-B_0 to C_{n+4}	t_{PHL10}				48	ns
	t_{PLH10}				48	ns
Delay from B_3-B_0 to $\overline{G}$ and $\overline{P}$	t_{PHL11}				44	ns
	t_{PLH11}				44	ns
Delay from B_3-B_0 to F = 0	t_{PHL12}				48	ns
	t_{PLH12}				48	ns
Delay from B_3-B_0 to OVR	t_{PHL13}	R_L = 68Ω, R = 1.5 kΩ, Y_3-Y_0, $\overline{G}$, C_L = 50 ±5 pF all outputs (see figure 5)			48	ns
	t_{PLH13}				48	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 3/	Group A subgroups	Limits Min	Limits Max	Unit
Delay from B_3-B_0 to RAM_3 and RAM_0	t_{PHL14}	C_L = 50 ±5 pF all outputs (see figure 5)	9,10,11		48	ns
	t_{PLH14}				48	ns
Delay from D_3-D_0 (ARITH) to Y_3-Y_0	t_{PHL15}				37	ns
	t_{PLH15}				37	ns
Delay from D_3-D_0 (ARITH) to F_3	t_{PHL16}				37	ns
	t_{PLH16}				37	ns
Delay from D_3-D_0 (ARITH) to C_{n+4}	t_{PHL17}				37	ns
	t_{PLH17}				37	ns
Delay from D_3-D_0 (ARITH) to $\overline{G}$ and $\overline{P}$	t_{PHL18}				34	ns
	t_{PLH18}				34	ns
Delay from D_3-D_0 (ARITH) to F = 0	t_{PHL19}				40	ns
	t_{PLH19}				40	ns
Delay from D_3-D_0 (ARITH) to OVR	t_{PHL20}				37	ns
	t_{PLH20}				37	ns
Delay from D_3-D_0 (ARITH) to RAM_3 and RAM_0	t_{PHL21}				37	ns
	t_{PLH21}				37	ns
Delay from D_3-D_0 (I = X37) to Y_3-Y_0	t_{PHL22}				37	ns
	t_{PLH22}				37	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 3/	Group A subgroups	Limits Min	Limits Max	Unit
Delay from D_3-D_0 (I = X37) to F_3	t_{PHL23}	C_L = 50 ±5 pF all outputs (see figure 5)	9,10,11		37	ns
	t_{PLH23}				37	ns
Delay from D_3-D_0 (I = X37) to F = 0	t_{PHL24}				40	ns
	t_{PLH24}				40	ns
Delay from D_3-D_0 (I = X37) to RAM_3 and RAM_0	t_{PHL25}				37	ns
	t_{PLH25}				37	ns
Delay from C_n to Y_3-Y_0	t_{PHL26}				25	ns
	t_{PLH26}				25	ns
Delay from C_n to F_3	t_{PHL27}				25	ns
	t_{PLH27}				25	ns
Delay from C_n to C_{n+4}	t_{PHL28}				21	ns
	t_{PLH28}				21	ns
Delay from C_n to F = 0	t_{PHL29}				28	ns
	t_{PLH29}				28	ns
Delay from C_n to OVR	t_{PHL30}				25	ns
	t_{PLH30}				25	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 3/	Group A subgroups	Limits Min	Limits Max	Unit
Delay from C_n to RAM_3 and RAM_0	t_{PHL31}	C_L = 50 ±5 pF all outputs (see figure 5)	9,10,11		28	ns
	t_{PLH31}				28	ns
Delay from I_2-I_0 to Y_3-Y_0	t_{PHL32}				40	ns
	t_{PLH32}				40	ns
Delay from I_2-I_0 to F_3	t_{PHL33}				40	ns
	t_{PLH33}				40	ns
Delay from I_2-I_0 to C_{n+4}	t_{PHL34}				40	ns
	t_{PLH34}				40	ns
Delay from I_2-I_0 to $\overline{G}$ and $\overline{P}$	t_{PHL35}				44	ns
	t_{PLH35}				44	ns
Delay from I_2-I_0 to F = 0	t_{PHL36}				44	ns
	t_{PLH36}				44	ns
Delay from I_2-I_0 to OVR	t_{PHL37}				40	ns
	t_{PLH37}				40	ns
Delay from I_2-I_0 to RAM_3 and RAM_0	t_{PHL38}				40	ns
	t_{PLH38}				40	ns
Delay from I_5-I_3 to Y_3-Y_0	t_{PHL39}				40	ns
	t_{PLH39}				40	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 3/	Group A subgroups	Limits Min	Limits Max	Unit
Delay from I_5-I_3 to F_3	t_{PHL40}	C_L = 50 ±5 pF all outputs (see figure 5)	9,10,11		40	ns
	t_{PLH40}				40	ns
Delay from I_5-I_3 to C_{n+4}	t_{PHL41}				40	ns
	t_{PLH41}				40	ns
Delay from I_5-I_3 to $\overline{G}$, $\overline{P}$	t_{PHL42}				40	ns
	t_{PLH42}				40	ns
Delay from I_5-I_3 to F = 0	t_{PHL43}				40	ns
	t_{PLH43}				40	ns
Delay from I_5-I_3 to OVR	t_{PHL44}				40	ns
	t_{PLH44}				40	ns
Delay from I_5-I_3 to RAM_3 and RAM_0	t_{PHL45}				40	ns
	t_{PLH45}				40	ns
Delay from I_8-I_6 to Y_3-Y_0	t_{PHL46}				29	ns
	t_{PLH46}				29	ns
Delay from A_3-A_0 (I = 2XX) to Y_3-Y_0	t_{PHL47}				40	ns
	t_{PLH47}				40	ns
Delay from CP to Y_3-Y_0	t_{PHL48}				40	ns
	t_{PLH48}				40	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 3/	Group A subgroups	Limits Min	Limits Max	Unit
Delay from CP to F_3	t_{PHL49}	C_L = 50 ±5 pF all outputs (see figure 5)	9,10,11		40	ns
	t_{PLH49}				40	ns
Delay from CP to C_{n+4}	t_{PHL50}				40	ns
	t_{PLH50}				40	ns
Delay from CP to $\overline{G}$ and $\overline{P}$	t_{PHL51}				40	ns
	t_{PLH51}				40	ns
Delay from CP to F = 0	t_{PHL52}				40	ns
	t_{PLH52}				40	ns
Delay from CP to OVR	t_{PHL53}				40	ns
	t_{PLH53}				40	ns
Delay from CP to RAM_3 and RAM_0	t_{PHL54}				40	ns
	t_{PLH54}				40	ns
Delay from CP to Q_3 and Q_0	t_{PHL55}				33	ns
	t_{PLH55}				33	ns
Delay from $\overline{OE}$ to Y_3-Y_0	t_{PZL1}	C_L = 50 ±5 pF			25	ns
	t_{PZH1}				25	ns
Delay from I_8 to RAM_3 and RAM_0	t_{PZL2}				29	ns
	t_{PZH2}				29	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

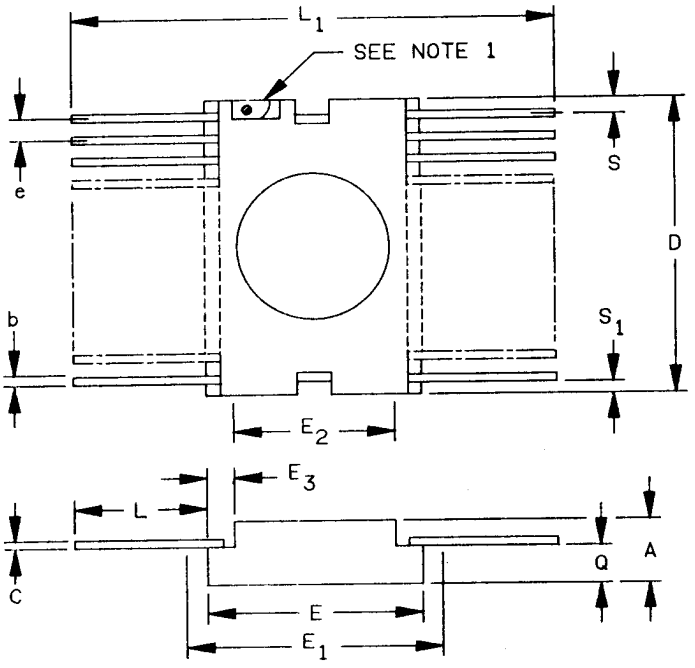
Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 3/	Group A subgroups	Limits Min	Limits Max	Unit
Delay from I_8 to Q_3 and Q_0	t_{PZL3}	C_L = 50 ±5 pF all outputs	9,10,11		29	ns
	t_{PZH3}				29	ns
Delay from $\overline{OE}$ to Y_3-Y_0 float 4/	t_{PLZ1}				25	ns
	t_{PHZ1}				25	ns
Delay from I_8 to RAM_3 and RAM_0 float	t_{PLZ2}				29	ns
	t_{PHZ2}				29	ns
Delay from I_8 to Q_3 and Q_0 float	t_{PLZ3}				29	ns
	t_{PHZ3}				29	ns
Minimum clock low time	t_{PWL}				15	ns
Minimum clock high time	t_{PWH}				15	ns
Minimum clock period	t_{cp}				32	ns

1/ These are three-state outputs internally connected to TTL inputs. The tristate condition must be OFF.

2/ Not more than one output should be shorted at a time. Duration of the short circuit test shall not exceed 1 second.

3/ Refer to figure 6 for output load resistor values and test circuits.

4/ Output disable tests performed with C_L = 5 pF and measured to 0.5 V change of output voltage level.



Ltr	Dimensions			
	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.070	.098	1.78	2.49
b	.017	.023	0.43	0.58
c	.006	.010	0.15	0.25
D	1.050	1.090	26.67	27.69
E	.620	.660	15.75	16.76
E_1	----	.680	----	17.27
E_2	.520	----	13.21	----
E_3	.030	----	0.76	----
e	.045	.055	1.14	1.40
L	.310	.370	7.87	9.40
L_1	1.280	1.360	32.51	34.54
Q	.030	.060	0.76	1.52
S	----	.045	----	1.14
S_1	.005	----	0.13	----

NOTES:
1. Index area: A notch, tab, or pin one identification mark shall be located within the shaded area shown.
2. E_1 allows for Ag-Cu alloy brazed overun.
3. Dimensions b and c increase by 3 mils maximum limit is tinplate/solder dip lead finish is applied.
4. Dimensions are in inches.
5. Metric equivalents are given for general information only.

FIGURE 1. Case outline Z (42-lead, 5/8" x 1-1/16"), flat package.

Device type 01

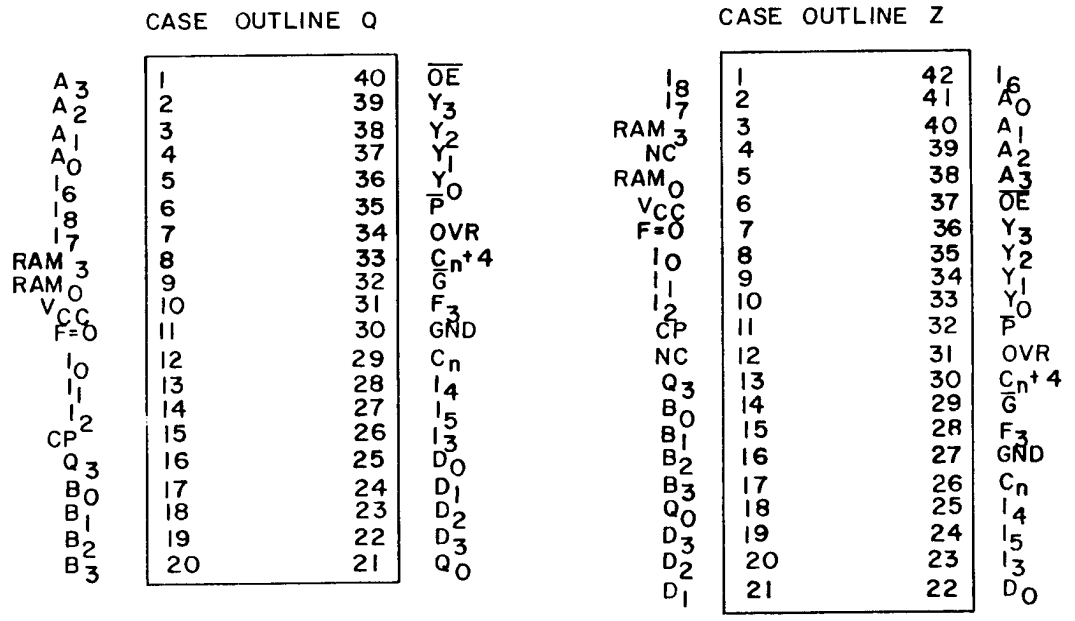


FIGURE 2. Terminal connections.

Device type 01

Micro code			ALU source operands		
I_2	I_1	I_0	Octal code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	0	Q
L	H	H	3	0	B
H	L	L	4	0	A
H	L	H	5	D	A
H	H	L	5	D	Q
H	H	H	7	D	0

ALU sources operand control.

Micro code					
I_5	I_4	I_3	Octal code	ALU function	Symbol
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S - R
L	H	L	2	R Minus S	R - S
L	H	H	3	R OR S	R $\vee$ S
H	L	L	4	R AND S	R $\wedge$ S
H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ $\wedge$ S
H	H	L	6	R EX-OR S	R $\veebar$ S
H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

ALU function control

Micro code				RAM function		Q-REG function		Y Output	RAM Shifter		Q Shifter	
I_8	I_7	I_6	Octal code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	None	None	F → Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F → B	X	None	A	X	X	X	X
L	H	H	3	None	F → B	X	None	F	X	X	X	X
H	L	L	4	Down	F/2 → B	Down	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	Down	F/2 → B	X	None	F	F_0	IN_3	Q_0	X
H	H	L	6	Up	2F → B	Up	2Q → Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	Up	2F → B	X	None	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register addressed by B inputs.
UP is toward MSB; Down is toward LSB.

ALU destination control.

FIGURE 3. Truth tables and logic equations.

Device type 01

Octal I_{543}	ALU Function \ ALU Source I_{210} Octal	0	1	2	3	4	5	6	7
		A,Q	A,B	0,Q	0,B	0,A	D,A	D,Q	D,0
0	C_n = L R Plus S C_n = H	A+Q A+Q+1	A+B A+B+1	Q Q+1	B B+1	A A+1	D+A D+A+1	D+Q D+Q+1	D D+1
1	C_n = L S Minus R C_n = H	Q-A-1 Q-A	B-A-1 B-A	Q-1 Q	B-1 B	A-1 A	A-D-1 A-D	Q-D-1 Q-D	-D-1 -D
2	C_n = L R Minus S C_n = H	A-Q-1 A-Q	A-B-1 A-B	-Q-1 -Q	-B-1 -B	-A-1 -A	D-A-1 D-A	D-Q-1 D-Q	D-1 D
3	R OR S	A∨Q	A∨B	Q	B	A	D∨A	D∨Q	D
4	R AND S	A∧Q	A∧B	0	0	0	D∧A	D∧Q	0
5	$\overline{R}$ AND S	$\overline{A}$∧Q	$\overline{A}$∧B	Q	B	A	$\overline{D}$∧A	$\overline{D}$∧Q	0
6	R EX-OR S	A⊻Q	A⊻B	Q	B	A	D⊻A	D⊻Q	D
7	R EX-NOR S	$\overline{A⊻Q}$	$\overline{A⊻B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D⊻A}$	$\overline{D⊻Q}$	$\overline{D}$

+ = Plus; - = Minus; ∨ = OR; ∧ = AND; ⊻ = EX-OR

Source operand and ALU function matrix.

FIGURE 3. Truth tables and logic equations - Continued.

Device type 01

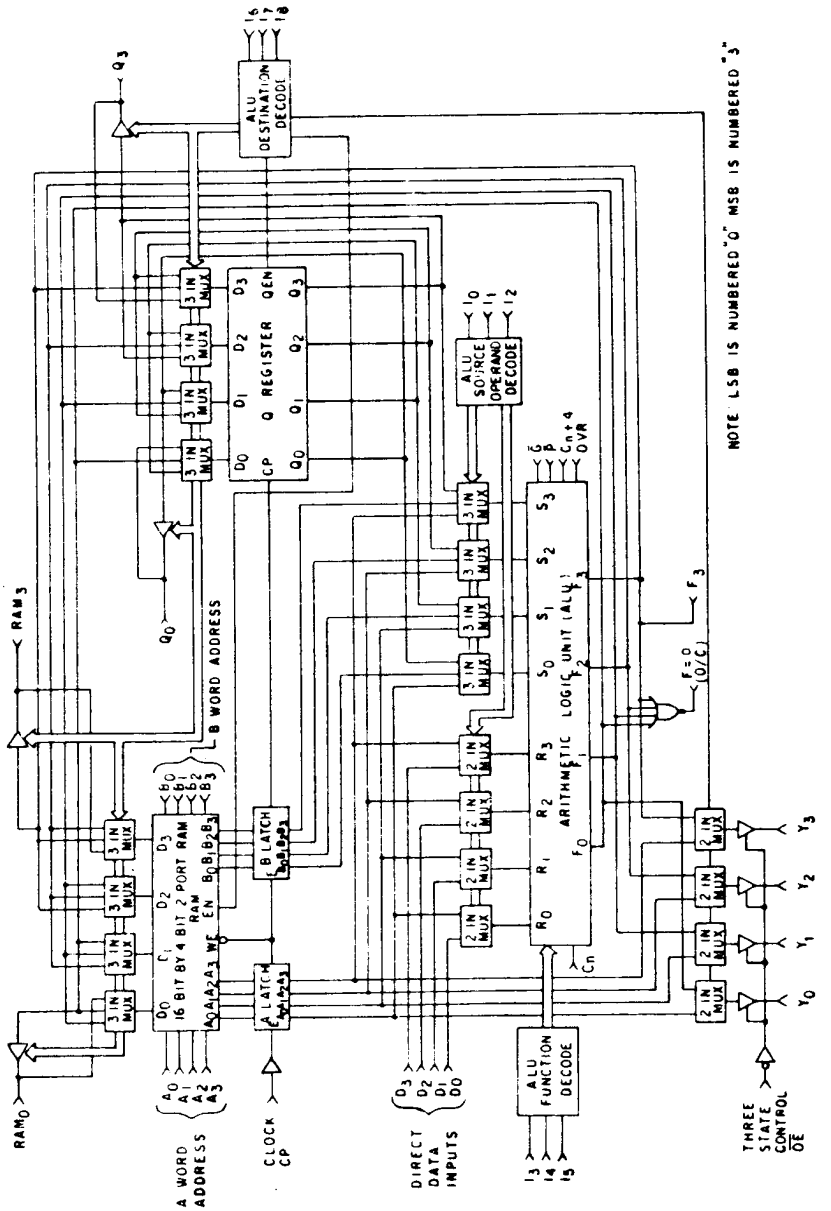
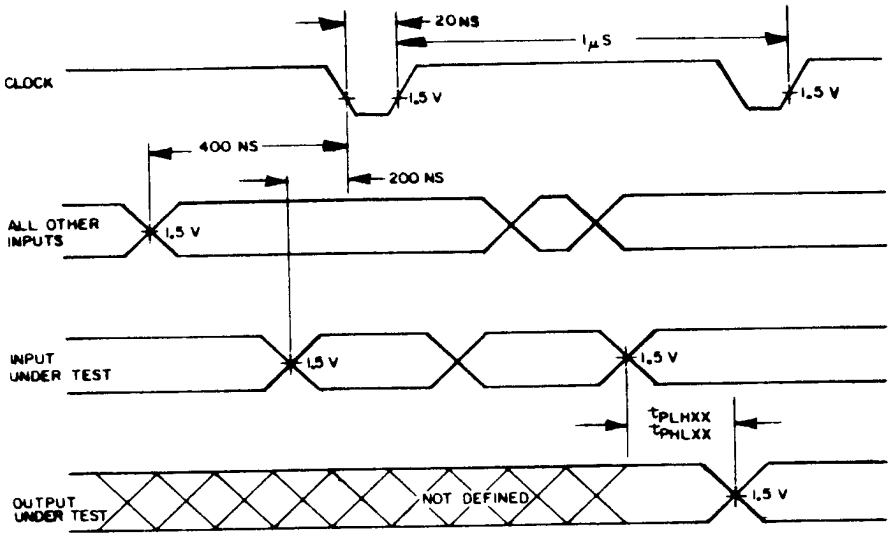
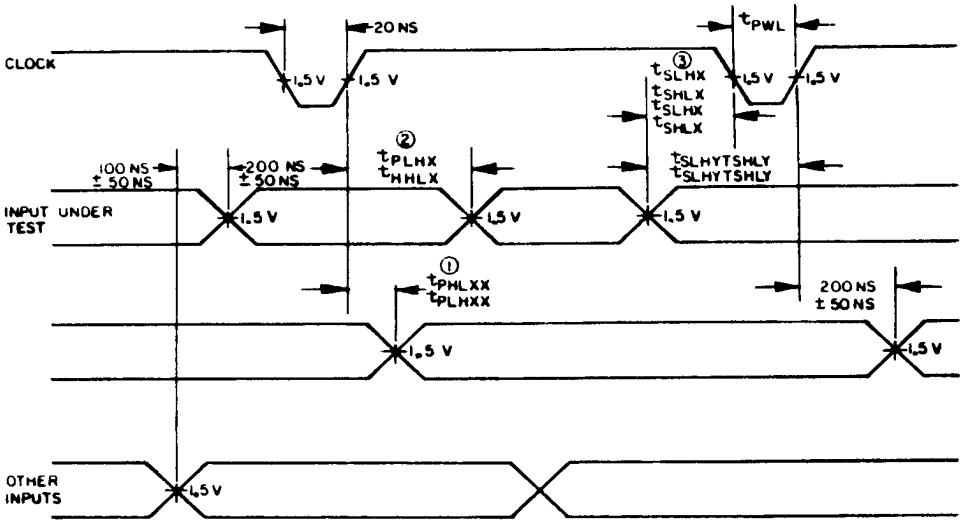


FIGURE 4. Block diagram.



NOTE: For t_{PLHXX}, t_{PHLXX}, XX equals 01 through 47.

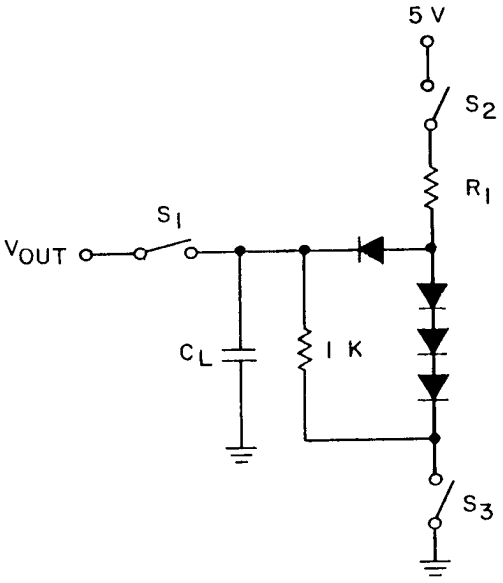
FIGURE 5. Timing waveforms.



NOTES:
1. For t_{PHLXX} and t_{PLHXX}, XX = 48 through 55. See table I for values.
2. For t_{HHLX} and t_{HLHX}, X = 1 through 7. See table I for values.
3. For $t_{SHLX \text{ or } Y}$ and $t_{SLHX \text{ or } Y}$, X = 2, 4, 5; Y = 1, 3, 6, 7, 8, 9, 10, 11, 12, and 13. See table I for values.

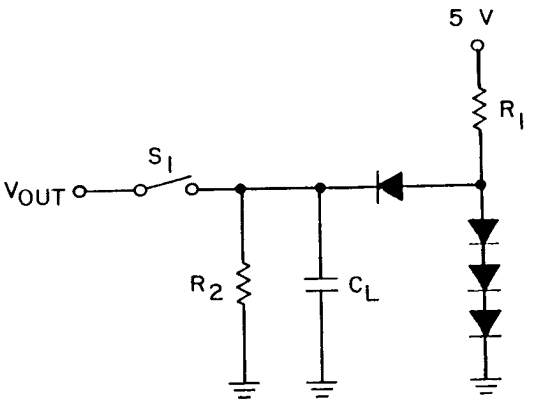
FIGURE 5. Timing waveforms - Continued.

THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL} / 1\,K}$$

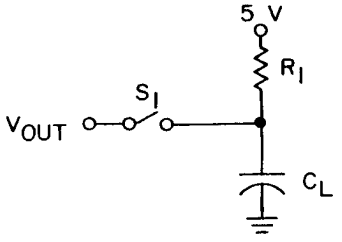
NORMAL OUTPUTS



$$R2 = \frac{2.4\ V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL} / R_2}$$

OPEN-COLLECTOR OUTPUTS



$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

FIGURE 6. Switching time test circuit loads.

MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A		DWG NO 84057
		REV C	PAGE 23

DESC FORM 193A
FEB 86

Functional Pin	Test Circuit	R_1	R_2
RAM_3	A	560	1 K
RAM_0	A	560	1 K
F = 0	C	270	- -
Q_3	A	560	1 K
Q_0	A	560	1 K
F_3	B	620	3.9 K
G	B	220	1.5 K
C_{n+4}	B	360	2.4 K
OVR	B	470	3 K
P	B	470	3 K
Y_{0-3}	A	220	1 K

NOTES:
1. C_L = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3, are closed during function tests and all AC tests except output enable test.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_3 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0 pF for output disable tests.

FIGURE 6. Switching time test circuit loads - Continued.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 functional test shall include verification of programming set.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1, 7, 9
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9**
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9**, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 7
Additional electrical subgroups for for group C periodic inspections	---

*PDA applies to subgroup 1.
**Subgroup 9 is run concurrently with subgroup 7 with a combined LTPD of 5.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
8405701QX	34335 50088 50088	AM2901C/BQA TS2901CMCB/C TS2901CMJB/C
8405701ZX	34335	AM2901C/BYC

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94086
50088	Thompson Components-Mostek Corporation 1310 Electronics Drive Carrollton, TX, 75006

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