Integrated Device Technology, Inc.

# HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

**IDT54/74FCT821AT/BT/CT/DT**
**IDT54/74FCT823AT/BT/CT/DT**
**IDT54/74FCT825AT/BT/CT**
**IDT54/74FCT826AT/BT/CT**

## FEATURES:

- Fastest CMOS logic family available
- A, B, C and D speed grades with 4.2ns tPD
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- IOL = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- True TTL input and output compatibility
  - VOH = 3.3V (typ.)
  - VOL = 0.3V (typ.)
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meet or exceed JEDEC Standard 18 specifications

## DESCRIPTION:

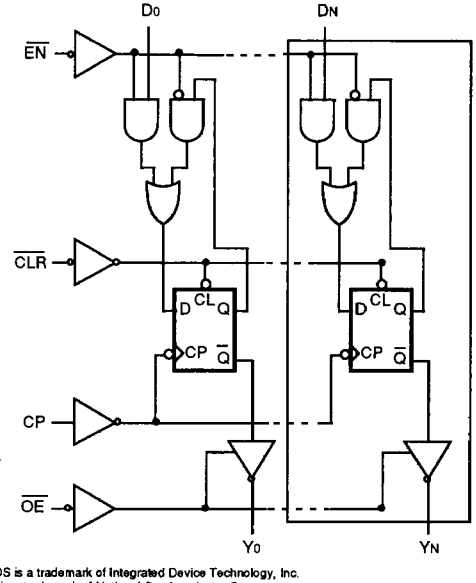
The IDT54/74FCT800 seriesis built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT821AT/BT/CT/DT are buffered, 10-bit wide versions of the popular '374 function. The IDT54/74FCT823AT/BT/CT/DT are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825AT/BT/CT and IDT54/74FCT826AT/BT/CT are 8-bit buffered registers with all the '823 controls plus multiple enables ($\overline{OE1}$, $\overline{OE2}$, $\overline{OE3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high IOL/IOH.

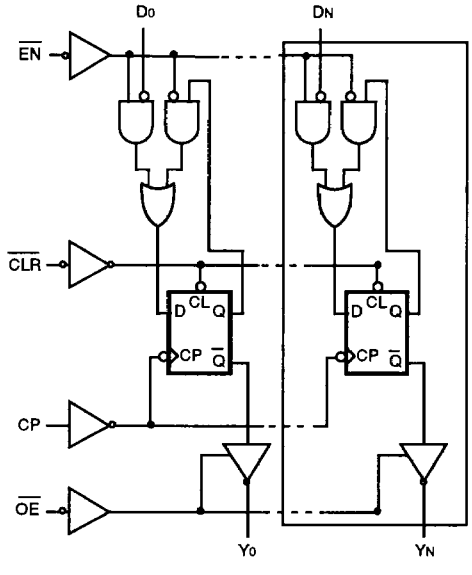
All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

## FUNCTIONAL BLOCK DIAGRAM

**IDT54/74FCT821/823/825T**




**IDT54/74FCT826T**

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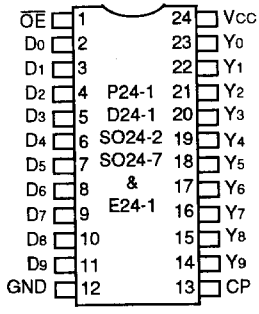
FAST is a trademark of National Semiconductor Co.

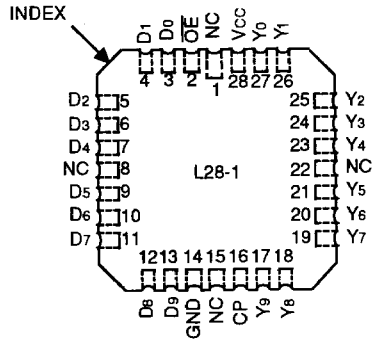
## PIN CONFIGURATIONS

## LOGIC SYMBOLS

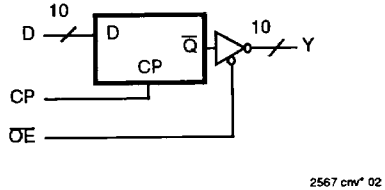
### IDT54/74FCT821T 10-BIT REGISTER




DIP/SOIC/SSOP/CERPACK
TOP VIEW

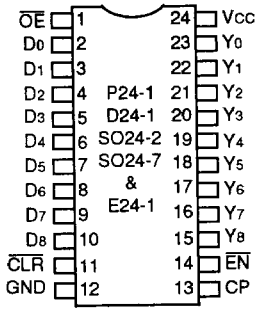



LCC
TOP VIEW

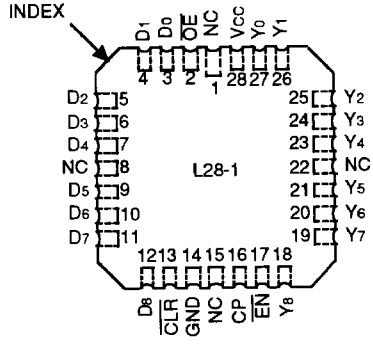



2567 cnv* 02

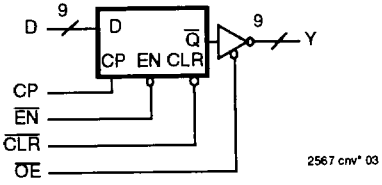
### IDT54/74FCT823T 9-BIT REGISTER




DIP/SOIC/SSOP/CERPACK
TOP VIEW

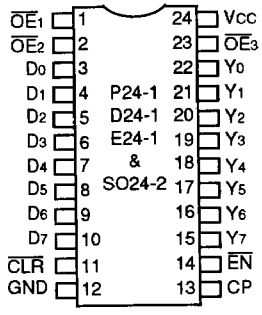



LCC
TOP VIEW

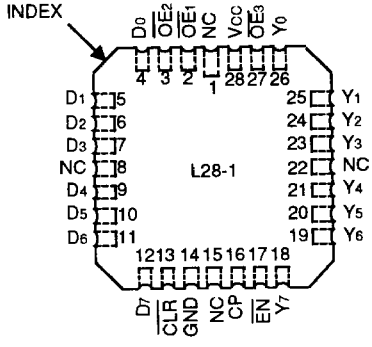



2567 cnv* 03

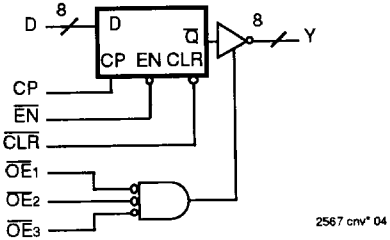
### IDT54/74FCT825/826T 8-BIT REGISTER




DIP/SOIC/CERPACK
TOP VIEW




LCC
TOP VIEW




2567 cnv* 04

## PRODUCT SELECTOR GUIDE

| | Device | | |
|---|---|---|---|
| | 10-Bit | 9-Bit | 8-Bit |
| Non-inverting | FCT821AT/BT/CT/DT | FCT823AT/BT/CT/DT | FCT825AT/BT/CT |
| Inverting | | | FCT826AT/BT/CT |

2567 tbl 01

## PIN DESCRIPTION

| Names | I/O | Description |
|---|---|---|
| $D_I$ | I | The D flip-flop data inputs. |
| $\overline{CLR}$ | I | When the clear input is LOW and $\overline{OE}$ is LOW, the QI outputs are LOW. When the clear input is HIGH, data can be entered into the register. |
| CP | I | Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition. |
| $Y_I$ | O | The register 3-state outputs. |
| $\overline{EN}$ | I | Clock Enable. When the clock enable is LOW, data on the D I input is transferred to the QI output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the QI outputs do not change state, regardless of the data or clock input transitions. |
| $\overline{OE}$ | I | Output Control. When the $\overline{OE}$ input is HIGH, the Y I outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the YI outputs. |

2567 tbl 02

## FUNCTION TABLE[1] IDT54/74FCT821/823/825T

| Inputs | | | | | Internal/ Outputs | | |
|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{CLR}$ | $\overline{EN}$ | $D_I$ | CP | QI | $Y_I$ | Function |
| H | H | L | L | ↑ | L | Z | High Z |
| H | H | L | H | ↑ | H | Z | |
| H | L | X | X | X | L | Z | Clear |
| L | L | X | X | X | L | L | |
| H | H | H | X | X | NC | Z | Hold |
| L | H | H | X | X | NC | NC | |
| H | H | L | L | ↑ | L | Z | Load |
| H | H | L | H | ↑ | H | Z | |
| L | H | L | L | ↑ | L | L | |
| L | H | L | H | ↑ | H | H | |

**NOTE:**
1. H = HIGH
   L = LOW
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition
   Z = High Impedance

2567 tbl 03

## FUNCTION TABLE[1] IDT54/74FCT826T

| Inputs | | | | | Internal/ Outputs | | |
|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{CLR}$ | $\overline{EN}$ | $D_I$ | CP | QI | $Y_I$ | Function |
| H | H | L | L | ↑ | H | Z | High Z |
| H | H | L | H | ↑ | L | Z | |
| H | L | X | X | X | L | Z | Clear |
| L | L | X | X | X | L | L | |
| H | H | H | X | X | NC | Z | Hold |
| L | H | H | X | X | NC | NC | |
| H | H | L | L | ↑ | H | Z | Load |
| H | H | L | H | ↑ | L | Z | |
| L | H | L | L | ↑ | H | H | |
| L | H | L | H | ↑ | L | L | |

**NOTE:**
1. H = HIGH
   L = LOW
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition
   Z = High Impedance

2567 tbl 10

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## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Commercial | Military | Unit |
|---|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | –0.5 to +7.0 | –0.5 to +7.0 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | –0.5 to $V_{CC}$ | –0.5 to $V_{CC}$ | V |
| $T_A$ | Operating Temperature | 0 to +70 | –55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | –65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 0.5 | 0.5 | W |
| $I_{OUT}$ | DC Output Current | 120 | 120 | mA |

**NOTES:** 2567 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 8 | 12 | pF |

**NOTE:** 2567 tbl 05

1. This parameter is measured at characterization but not tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ± 5%; Military: $T_A$ = –55°C to +125°C, $V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Conditions(1) | | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic HIGH Level | | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max. | $V_I$ = 2.7V | — | — | 5 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max. | $V_I$ = 0.5V | — | — | –5 | µA |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = Max. | $V_O$ = 2.7V | — | — | 10 | µA |
| $I_{OZL}$ | | | $V_O$ = 0.5V | — | — | –10 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = Max., $V_I$ = $V_{CC}$ (Max.) | | — | — | 20 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min., $I_N$ = –18mA | | — | –0.7 | –1.2 | V |
| $I_{OS}$ | Short Circuit Current | $V_{CC}$ = Max.(3), $V_O$ = GND | | –60 | –120 | –225 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –6mA MIL. $I_{OH}$ = –8mA COM'L. | 2.4 | 3.3 | — | V |
| | | | $I_{OH}$ = –12mA MIL. $I_{OH}$ = –15mA COM'L. | 2.0 | 3.0 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 32mA MIL. $I_{OL}$ = 48mA COM'L. | — | 0.3 | 0.5 | V |
| $V_H$ | Input Hysteresis | — | | — | 200 | — | mV |
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max. $V_{IN}$ = GND or $V_{CC}$ | | — | 0.2 | 1.5 | mA |

**NOTES:** 2567 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC}$ = Max.<br>$V_{IN}$ = 3.4V[3] | | — | 0.5 | 2.0 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | $V_{CC}$ = Max.<br>Outputs Open<br>$\overline{OE}$ = $\overline{EN}$ = GND<br>One Input Toggling<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 0.15 | 0.25 | mA/<br>MHz |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = Max.<br>Outputs Open<br>$f_{CP}$= 10MHz<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 1.7 | 4.0 | mA |
| | | $\overline{OE}$ = $\overline{EN}$ = GND<br>One Bit Toggling<br>at fi = 5MHz<br>50% Duty Cycle | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 2.2 | 6.0 | |
| | | $V_{CC}$ = Max.<br>Outputs Open<br>$f_{CP}$= 10MHz<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 4.0 | 7.8[5] | |
| | | $\overline{OE}$ = $\overline{EN}$ = GND<br>Eight Bits Toggling<br>at fi = 2.5MHz<br>50% Duty Cycle | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 6.2 | 16.8[5] | |

2567 tbl 07

**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Per TTL driven input ($V_{IN}$ = 3.4V); all other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   $I_{CC}$ = Quiescent Current
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $f_i$ = Input Frequency
   $N_i$ = Number of Inputs at $f_i$
   All currents are in milliamps and all frequencies are in megahertz.

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## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Condition[1] | FCT821AT-826AT | | | | FCT821BT-826BT | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Com'l. | | Mil. | | Com'l. | | Mil. | | |
| | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| tPLH<br>tPHL | Propagation Delay<br>CP to Yi ($\overline{OE}$ = LOW) | CL = 50pF<br>RL = 500Ω | 1.5 | 10.0 | 1.5 | 11.5 | 1.5 | 7.5 | 1.5 | 8.5 | ns |
| | | CL = 300pF[4]<br>RL = 500Ω | 1.5 | 20.0 | 1.5 | 20.0 | 1.5 | 15.0 | 1.5 | 16.0 | |
| tSU | Set-up Time HIGH or LOW<br>Di to CP | CL = 50pF<br>RL = 500Ω | 4.0 | — | 4.0 | — | 3.0 | — | 3.0 | — | ns |
| tH | Hold Time HIGH or LOW<br>Di to CP | | 2.0 | — | 2.0 | — | 1.5 | — | 1.5 | — | ns |
| tSU | Set-up Time HIGH or LOW<br>$\overline{EN}$ to CP | | 4.0 | — | 4.0 | — | 3.0 | — | 3.0 | — | ns |
| tH | Hold Time HIGH or LOW<br>$\overline{EN}$ to CP | | 2.0 | — | 2.0 | — | 0 | — | 0 | — | ns |
| tPHL | Propagation Delay, $\overline{CLR}$ to Yi | | 1.5 | 14.0 | 1.5 | 15.0 | 1.5 | 9.0 | 1.5 | 9.5 | ns |
| tREM | Recovery Time $\overline{CLR}$ to CP | | 6.0 | — | 7.0 | — | 6.0 | — | 6.0 | — | ns |
| tW | Clock Pulse Width<br>HIGH or LOW | | 7.0 | — | 7.0 | — | 6.0 | — | 6.0 | — | ns |
| tW | $\overline{CLR}$ Pulse Width LOW | | 6.0 | — | 7.0 | — | 6.0 | — | 6.0 | — | ns |
| tPZH<br>tPZL | Output Enable Time $\overline{OE}$ to Yi | CL = 50pF<br>RL = 500Ω | 1.5 | 12.0 | 1.5 | 13.0 | 1.5 | 8.0 | 1.5 | 9.0 | ns |
| | | CL = 300pF[4]<br>RL = 500Ω | 1.5 | 23.0 | 1.5 | 25.0 | 1.5 | 15.0 | 1.5 | 16.0 | |
| tPHZ<br>tPLZ | Output Disable Time $\overline{OE}$<br>to Yi | CL = 5pF[4]<br>RL = 500Ω | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 6.5 | 1.5 | 7.0 | ns |
| | | CL = 50pF<br>RL = 500Ω | 1.5 | 8.0 | 1.5 | 9.0 | 1.5 | 7.5 | 1.5 | 8.0 | |

2567 tbl 08

**NOTES:**
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Condition[1] | FCT821CT-826CT | | | | FCT821DT | | FCT823DT | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Com'l. | | Mil. | | Com'l. | | Com'l. | | |
| | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| tPLH<br>tPHL | Propagation Delay<br>CP to Yi ($\overline{OE}$ = LOW) | CL = 50pF<br>RL = 500Ω | 1.5 | 6.0 | 1.5 | 7.0 | 1.5 | 4.2 | 1.5 | 5.0 | ns |
| | | CL = 300pF[4]<br>RL = 500Ω | 1.5 | 12.5 | 1.5 | 13.5 | 1.5 | 8.0 | 1.5 | 8.5 | |
| tSU | Set-up Time HIGH or LOW<br>Di to CP | CL = 50pF<br>RL = 500Ω | 3.0 | — | 3.0 | — | 2.0 | — | 2.0 | — | ns |
| tH | Hold Time HIGH or LOW<br>Di to CP | | 1.5 | — | 1.5 | — | 1.0 | — | 1.0 | — | ns |
| tSU | Set-up Time HIGH or LOW<br>$\overline{EN}$ to CP | | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | ns |
| tH | Hold Time HIGH or LOW<br>$\overline{EN}$ to CP | | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tPHL | Propagation Delay, $\overline{CLR}$ to Yi | | 1.5 | 8.0 | 1.5 | 8.5 | 1.5 | 5.0 | 1.5 | 5.0 | ns |
| tREM | Recovery Time $\overline{CLR}$ to CP | | 6.0 | — | 6.0 | — | 3.0 | — | 3.0 | — | ns |
| tW | Clock Pulse Width<br>HIGH or LOW[3] | | 6.0 | — | 6.0 | — | 3.0 | — | 3.0 | — | ns |
| tW | $\overline{CLR}$ Pulse Width LOW[3] | | 6.0 | — | 6.0 | — | 3.0 | — | 3.0 | — | ns |
| tPZH<br>tPZL | Output Enable Time $\overline{OE}$ to Yi | CL = 50pF<br>RL = 500Ω | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 4.8 | 1.5 | 4.8 | ns |
| | | CL = 300pF[4]<br>RL = 500Ω | 1.5 | 12.5 | 1.5 | 13.5 | 1.5 | 9.0 | 1.5 | 9.0 | |
| tPHZ<br>tPLZ | Output Disable Time $\overline{OE}$<br>to Yi | CL = 5pF[4]<br>RL = 500Ω | 1.5 | 6.0 | 1.5 | 6.0 | 1.5 | 4.0 | 1.5 | 4.0 | ns |
| | | CL = 50pF<br>RL = 500Ω | 1.5 | 6.5 | 1.5 | 6.5 | 1.5 | 4.0 | 1.5 | 4.0 | |

2567 tbl 09

**NOTES:**
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

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